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Characterization of the embedded micromechanical device approach to the monolithic integration of MEMS with CMOS

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ABSTRACT

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MicroElectroMechanical Systems (MEMS) with driving, controlling, and signal processing electronics. This integration promises to improve the performance of micromechanical devices as well as lower the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with a electronic devices in the same manufacturing and packaging process. In order to maintain modularity and overcome some of the manufacturing challenges of the CMOS-first approach to integration, we have developed a MEMS-first process. This process places the micromechanical devices in a shallow trench, planarizes the wafer, and seals the micromechanical devices in the trench. Then, a high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal processing associated with fabrication of the microelectronic processing does not aversely affect the mechanical properties of the polysilicon structures. These wafers with the completed, planarized micromechanical devices are then used as starting material for conventional CMOS processes. The circuit yield for the process has exceeded 98%. A description of the integration technology, the refinements to the technology, and wafer-scale parametric measurements of device characteristics is presented. Additionally, the performance of integrated sensing devices built using this technology is presented.

Keywords: Integration, Micromechanics, CMOS, CMP, Intelligent Micromachines

2. MONOLITHIC INTEGRATION OF MICROELECTRONICS AND MICROMECHANICS

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MicroElectroMechanical Structures (MEMS) with driving, controlling, and signal processing electronics. This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process. For example, Analog Devices has developed and marketed an accelerometer[1] which illustrates the viability and commercial potential of this integration. They accomplished this task by interleaving, combining, and customizing their manufacturing processes which produce the micromechanical devices with the processes that produce the electronics. In another approach, researchers at Berkeley[2] have developed a modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent micromechanical processing. The results of our implementation of the Berkeley CMOS-first approach was presented at this conference last year.[3]

In order to maintain the modularity of the Berkeley approach but overcome some of the manufacturing challenges of their CMOS-first approach, we have developed a MEMS-first process. This process places the micromechanical devices in a shallow trench, planarizes the wafer, and seals the micromechanical devices in the trench. These wafers with the completed, planarized micromechanical devices are then used as starting material for a conventional CMOS process. This technique is equally applicable to other microelectronic device technologies such as bipolar or BiCMOS. In our facility,

both 2 μm and 0.5 μm CMOS technologies on 6 inch wafers are available; the 2 μm process is being used as the development vehicle for the integrated technology. Since this integration approach does not modify the CMOS processing flow, the wafers with the subsurface micromechanical devices can also be sent to a foundry for microelectronic processing. Furthermore, the topology of multiple polysilicon layers does not complicate subsequent photolithography. A high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal budget of the microelectronic processing does not affect the mechanical properties of the polysilicon structures. This anneal can affect the doping profile of commonly used epitaxial starting material; however, this effect can be easily addressed by increasing the epitaxial layer thickness of the starting material.

3. THE EMBEDDED MEMS PROCESS

This process was been described previously in more detail.[4] Figure 1 is a schematic cross-section of the integrated technology. First, alignment marks are etched onto the surface of wafer in order to provide reference locations for subsequent processing. A shallow trench (~ 6 μm for the single-level polysilicon structures described here) is etched in (100) silicon wafers using an anisotropic etchant. The alignment marks from the top surface of the wafer are used as references to generate another set of alignment marks on the bottom surface of the trench.

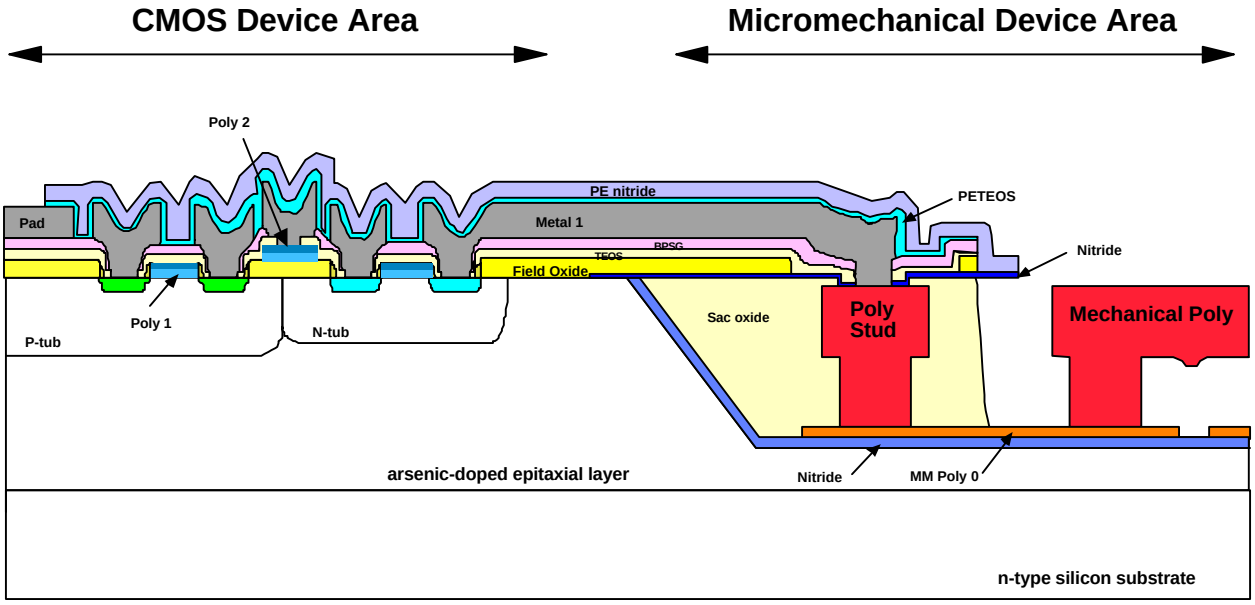

Figure 1. A cross-sectional schematic of the subsurface, embedded MEMS integrated technology.

A silicon nitride film is deposited to form a dielectric layer on the bottom of the trench. Sacrificial oxide and multiple layers of polysilicon are then deposited and patterned in a standard surface micromachining process. Polysilicon studs provide contact between the micromechanical devices and the CMOS; the depth of the trench is sized so that the top of the polysilicon stud lies just below the top of the trench. The shallow trenches are then filled with a series of oxide depositions optimized to eliminate void formation in high-aspect-ratio structures. The wafer is subsequently planarized with chemical-mechanical polishing (CMP). The entire structure is annealed to relieve stress in the structural polysilicon and sealed with a silicon nitride cap. At this point, conventional CMOS processing is performed. The backend of the process requires additional masks to open the nitride cap over the micromechanical layer prior to release of the micromechanical structures.

Photoresist is used as a protection layer over the exposed bond pads during the release process. The slow etching of the undoped, densified glasses used as sacrificial layers and the ability of this photoresist to withstand long, HF-based etches is presently a factor that imposes limits on the design rules used for spacing of release access holes in the structure.

Figure 2 shows a cross-sectional view of an anchor point for the MEMS device within a trench after planarization. The silicon nitride dielectric layer, the ground plane polysilicon, the micromechanical polysilicon and the sacrificial/planarizing layers are easily seen in this Scanning Electron Micrograph (SEM). Completed MEMS next to their controlling CMOS are shown in Figure 3.

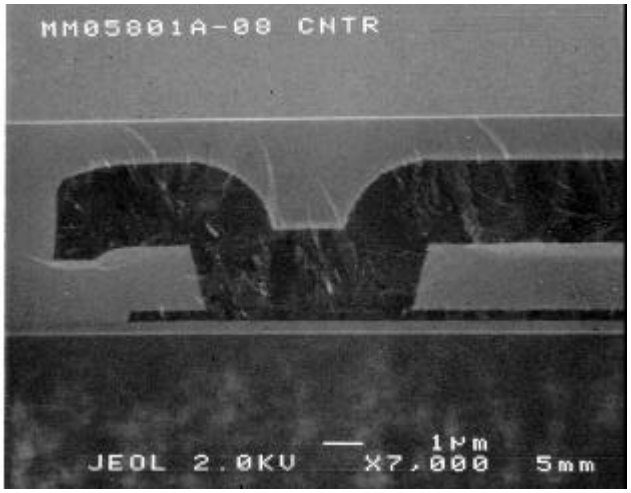

Figure 2. A cross-sectional view of a single-layer polysilicon (with ground plane) structure in a trench. The trench has been refilled with oxide and planarized using chemical-mechanical polishing. This planar structure is ready for standard CMOS processing.

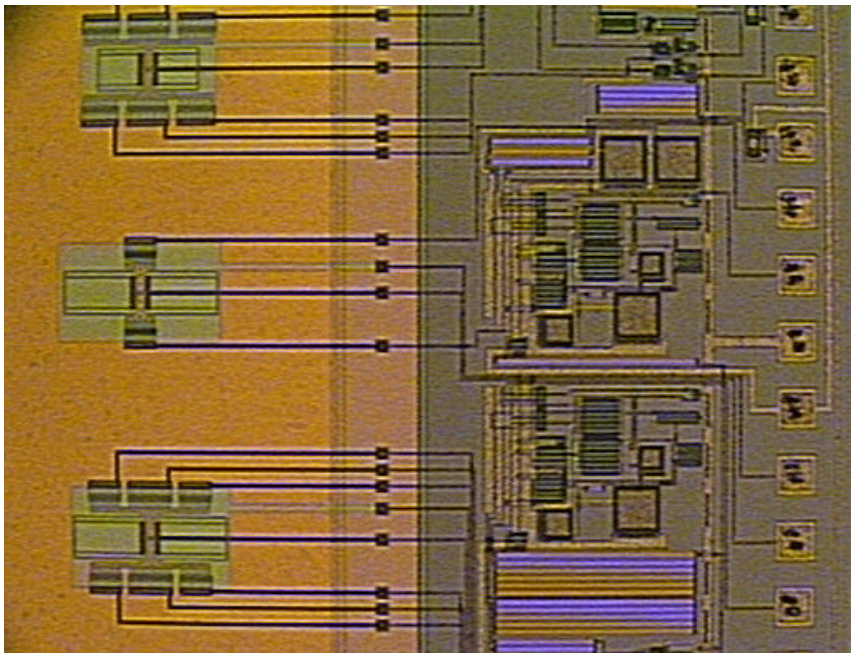

Figure 3. Surface-micromachined polysilicon resonators built in a trench alongside their CMOS sensing electronics. The marks on the bonding pads were caused during wafer-level testing.

This integration process is not limited to the single-level polysilicon process described here. This process can be used with more intricate micromechanical processes such as the three-level polysilicon technology previously developed at Sandia.[5] An example of this technology built in a trench is shown in Figure 4.

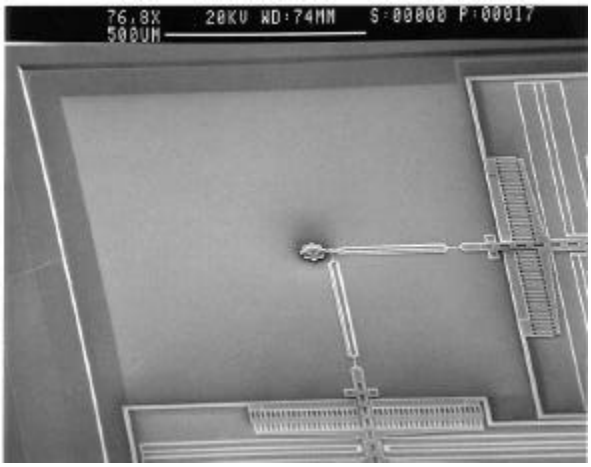

Figure 4. A three-level polysilicon structure (microengine) built in a trench. Here, the trench depth is approximately 12 μm.

4. CHARACTERIZATION

Devices including CMOS diagnostic structures, MEMS diagnostic structures, and combustible gas detectors were fabricated on this wafer. The layout of the completed die is shown in Figure 5. The completed MEMS structures showed no mechanical degradation with respect to MEMS structures which had not seen the CMOS process. This first wafer was tested at the wafer scale for parametric and functional data. The CMOS parametrics agreed within acceptable process control limits with our unmodified 2 μm CMOS process. Due to tester limitations, only the combustible gas sensors were tested at the wafer level from the first run of the technology in a fully-coupled CMOS/MEMS mode. These devices showed a yield of 78% as shown in the wafer map of Figure 6. The combustible gas sensor control circuitry included an op-amp and a set of power MOSFETs. Since then, yields of 98% have been achieved on some runs.

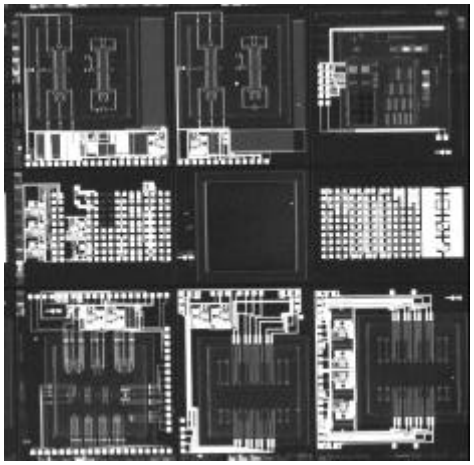

Figure 5. An photograph of the completed integrated MEMS/CMOS die illustrating the layout of the various sensors, resonators, test structures, and electronics.

A set of CMOS parametric test structures was fabricated on each die. These structures are shown in both the left and right center position of the reticle layout pictured in Figure 5. The parametrics collected included transistor threshold voltage data as well as contact resistance data. Wafer maps of this data are given in Figures 7 through 11. The data represented in these figures is essentially unchanged from our standard (non-integrated) CMOS parametric data. The threshold voltages are well-controlled and the contact resistances are reasonably low. In particular, the contact resistance to the p-channel source/drain is 10-20 ohms. This compares favorably with contact resistances previously reported of 100-150 ohms for a CMOS-first process.[3]

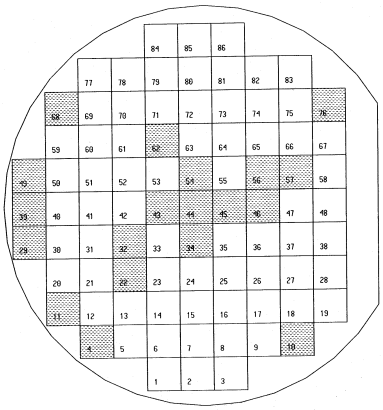

Figure 6. A wafer map from the first run showing functionality of wafer-level tests of combustible gas sensor devices. The unshaded devices are functional.

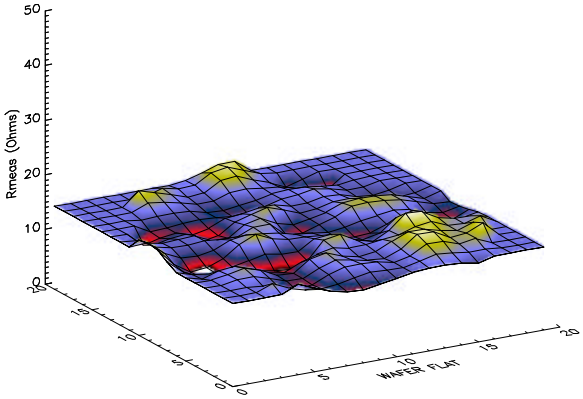

Figure 8. Source/drain contact resistance for 2 μm x 2 μm contacts to p-channel devices.

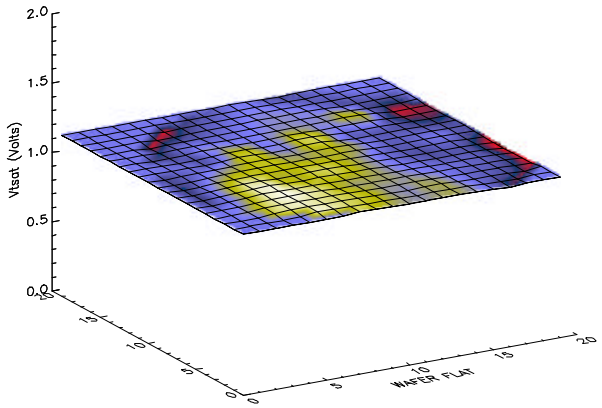

Figure 10. Threshold voltage for 2 μm channel length, n-channel transistors.

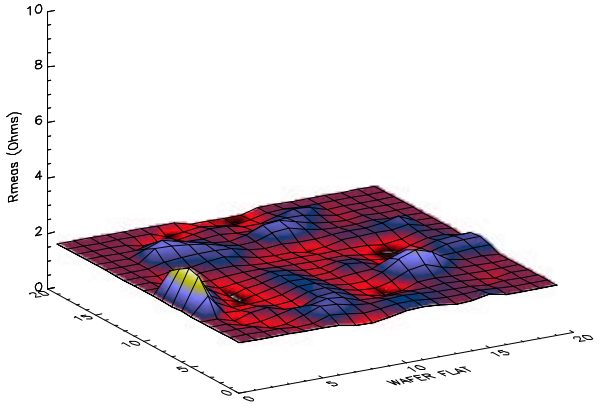

Figure 7. Source/drain contact resistance for 2 μm x 2 μm contacts to n-channel devices.

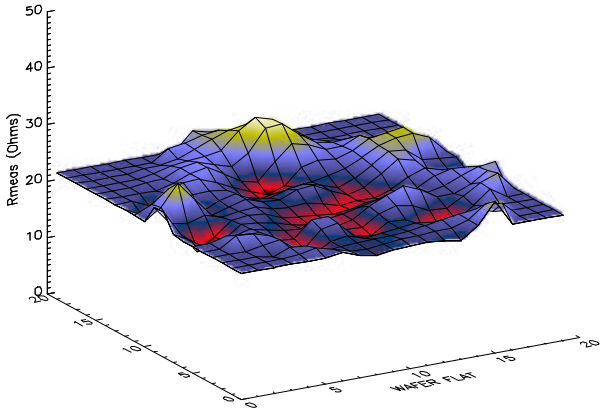

Figure 9. Metal to poly contact resistance.

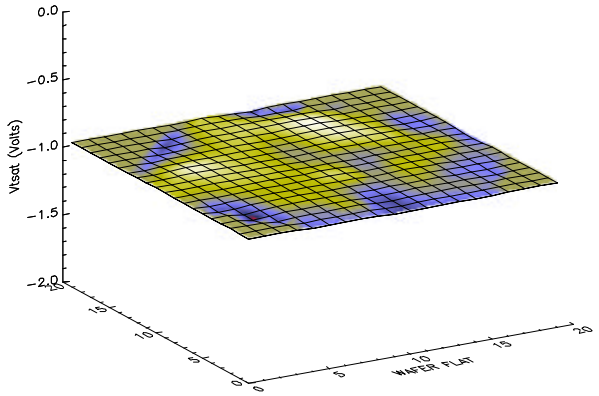

Figure 11. Threshold voltage for 2 μm channel length, p-channel transistors.

5. INTEGRATED MICROFILAMENT SENSORS

The combustible gas sensor (CGS) design presented here is based on a conventional device that operates by the catalytic oxidation of combustible gases. The heat of combustion, ΔH, evolved on a heated catalyst surface is detected by means of a resistance thermometer in proximity with the catalyst.[6-9] In its simplest incarnation a thin, electrically-heated platinum wire serves as catalyst, catalyst heater, and resistance thermometer; the heat of combustion on the hot wire is detected as a resistance variation of the wire.[10,11]

Polysilicon microfilaments, manufactured by now standard microfabrication techniques and coated with Pt by a micro-CVD technique (Figure 12) are well suited to combustible gas detection.[12] Here, ΔH is detected through a resistance variation in the polysilicon microfilament. Because it is thermally isolated from the substrate by a 2 μm air gap, the microfilament reaches maximum temperatures of roughly 500°C with about 100 mW of applied power. Hence, it serves as an efficient heater for the Pt catalyst on its surface.

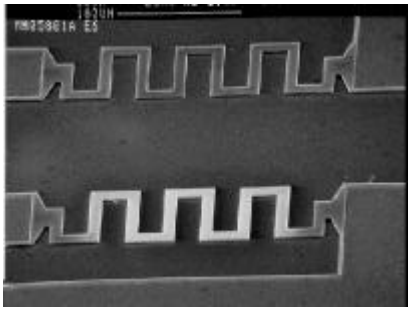

Figure 12. Plan view of two meandered microfilaments. Both filaments are fabricated of polysilicon and are 10 μm wide and 2μm thick. They are elevated above the substrate by a 2μm air gap to provide thermal isolation of the bridge from the substrate. The lower filament is coated with a 0.1 μm thick layer of Pt, deposited by micro-CVD techniques.

Such a MEMS fabricated filament and CMOS circuitry for control and detection were integrated by the Embedded MEMS Process and were tested at a wafer and die level in a fully-coupled CMOS/MEMS mode. A Hewlett-Packard 4156 Parameter Analyzer was used to power the CMOS and to monitor the electrical characteristics of the microfilament and a reference resistor. For ease of testing, a 10-turn potentiometer was used as the reference. The control circuit for the filaments as shown in Figure 13 is similar to a circuit described by Mastrangelo.[13] Examination of Figure 13 shows that as the potentiometer setting is increased, the currents to it and the microfilament are increased by the same amount. The reference resistance is negligibly altered by the slight current changes (~10-15 mA) necessary to affect maximum temperatures in the microfilament. Figure 14 illustrates that microfilament resistance follows the reference under the control of the CMOS circuit. This was the first indication that the MEMS/CMOS integration was successful.

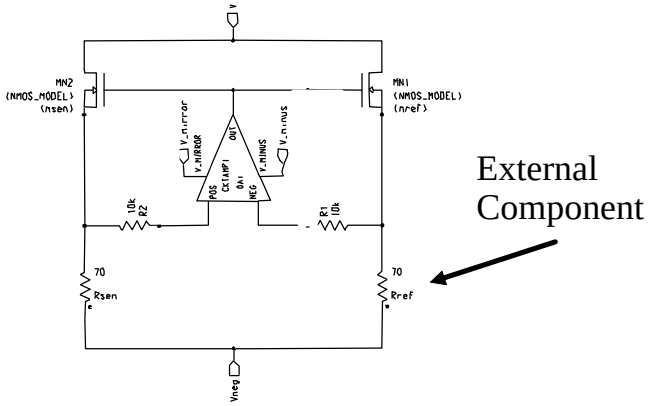

Figure 13. Schematic of the CMOS control circuit integrated with the micromachined sensing filament (labeled Rsen). For the purposes of testing, the micromachined reference resistance was replaced with a 10-turn potentiometer.

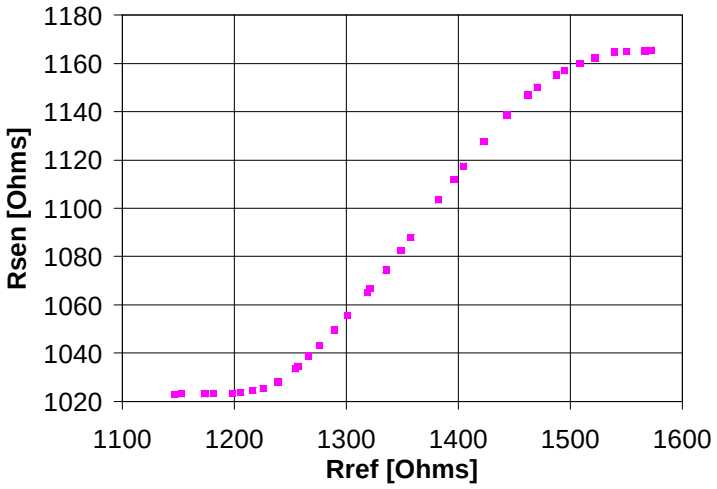

Figure 14. Under the control of the integrated CMOS circuit the micromachined filament resistance follows the reference resistance.

Prior to combustible gas sensing, a second test was performed to verify the success of the integration through the operation of the integrated microfilament as a thermal conductivity sensor. A heated microfilament was subjected to various mixtures of hydrogen in nitrogen in a steady-flow gas test bed. As the hydrogen concentration of a gas mixture increases, so does its thermal conductivity. The power supplied by the on-board CMOS to maintain the temperature of a microfilament subjected to such a mixture increases in response to the increased heat losses with thermal conductivity. This data is shown in Figure 15.

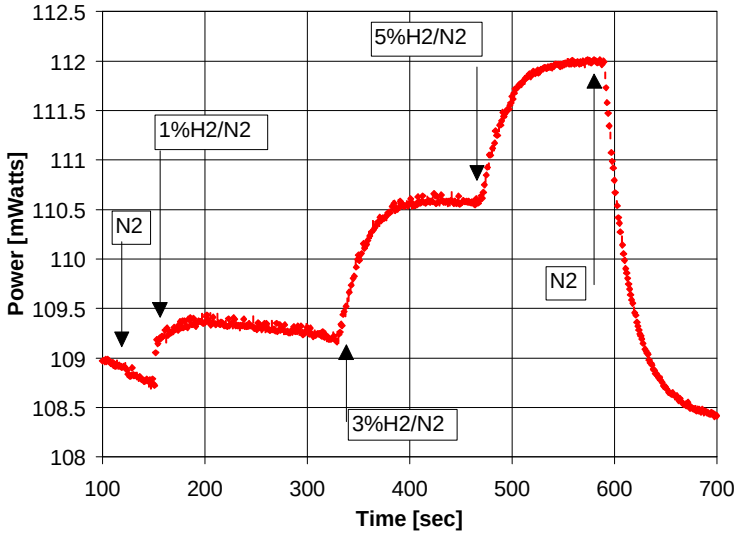

Figure 15. Power provided to the microfilament by the integrated CMOS to maintain its temperature during exposure to various mixtures of hydrogen in oxygen. As the concentration of hydrogen increases, so does the thermal conductivity of the gas mixture and its ability to cool the filament. The power required by the filament to maintain its temperature therefore increases with hydrogen concentration. Throughout the measurement flow was regulated to 1 slm.

Finally, the response of a platinum coated filament to combustible mixtures of hydrogen in 20% oxygen and nitrogen is given in Figure 16. Combustion on the Pt surface adds heat to the filament. In response, the power provided by

the CMOS electronics to maintain filament temperature, plotted on the vertical axis, drops in the presence of the combustible mixture.

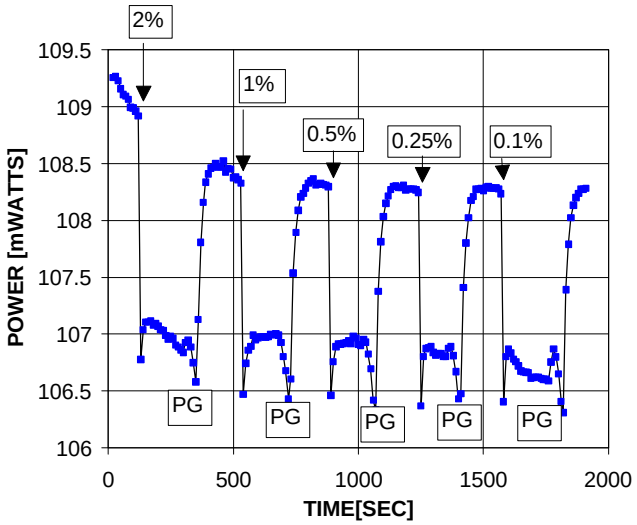

Figure 16. Response of the integrated microfilament to combustible mixtures of hydrogen in oxygen and nitrogen As combustion occurs on the heated, platinum-coated microfilament, the power provided by the control circuit to maintain filament temperature drops. Percentages indicate the amount of hydrogen in 20% oxygen and a balance of nitrogen. PG refers to a purge mixture of 1% hydrogen in a balance of nitrogen. Gas flows were regulated to 1 slm throughout.

6. CONCLUSIONS

The manufacturability of a technology that integrates surface-micromachined polysilicon structures with microelectronics in a modular fashion has been demonstrated. This technology does not impose additional limits on the size, thickness, or number of layers of the micromechanical polysilicon structures. The modularity of the process allows changes to be made to either the micromechanical process or the microelectronic process without affecting the other process. Excellent CMOS parametric data and yield along with the application of the process to a combustible gas sensor system have been demonstrated.

7. ACKNOWLEDGMENTS

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8. REFERENCES

1. W. Kuehnel and S. Sherman, “A surface micromachined silicon accelerometer with on-chip detection circuitry,” *Sensors and Actuators A*, vol. 45, no. 1, pp. 7-16, 1994.
2. W. Yun, R. Howe, and P. Gray, “Surface micromachined, digitally force-balanced accelerometer with integrated CMOS detection circuitry,” *Proc. of the IEEE Solid-State Sensor and Actuator Workshop `92*, p. 126, 1992.
3. J. Smith, S. Montague, and J. Sniegowski, “Material and processing issues for the monolithic integration of microelectronics with surface-micromachined polysilicon sensors and actuators,” *SPIE* vol. 2639, pp. 64-73, 1995.

4. J. Smith, S. Montague, J. Sniegowski, J. Murray, and P. McWhorter, "Embedded micromechanical devices for the monolithic integration of MEMS with CMOS", *Proc. IEDM ' 95*, pp. 609-612, 1995.
5. J. Sniegowski and E. Garcia, "Microfabricated actuators and their application to optics," *SPIE* vol. 2383, pp. 46-64, 1995.
6. A.R. Baker, British Patent #892530, 1962.
7. J.G. Firth, A. Jones, T.A. Jones, "The principles of the detection of flammable atmospheres by catalytic devices", Combustion and Flame, vol. 21,pp. 303-311, 1973.
8. E. Jones, "The pellistor catalytic gas sensor", *Solid State Gas Sensors*, P.T. Moseleyand and B.C. Tofield eds., A. Higler (Bristol and Philadelphia) 1987.
9. J.G. Firth, "Measurement of flammable gases and vapours", *Detection and Measurement of Hazardous Gases*, C.F. Cullis and J.G. Firth eds., Heinemann, London, 1981.
10. A. Chen, R. Luo, T.C. Tan and C.C. Liu, "A thick-film calorimetric sensor for monitoring the concentration of combustible gases", *Sensors and Actuators*, vol. 19, pp. 237-248, 1989.
11. J.J. Eherhardt, L. Colin, A. Accorsi, M. Kazmierczak and I. Zdanevitch, "Catalytic oxidation of methane on platinum thin film", *Sensors and Actuators B*, vol. 7, pp. 656-660, 1992.
12. R. P. Manginell, J. H. Smith, A. J. Ricco, D. J. Moreno, and R. C. Hughes, R. J. Huber, "Pulsed, Selective, CVD of Platinum on Microfilament Gas Sensors", *Tech. Digest 1996 Solid-State Sensor & Actuator Workshop*, pp. 23-27, 1996.
13. C. Mastrangelo, *Thermal Applications of Microbridges*, Ph. D. Thesis, U.C. Berkeley, 1991.