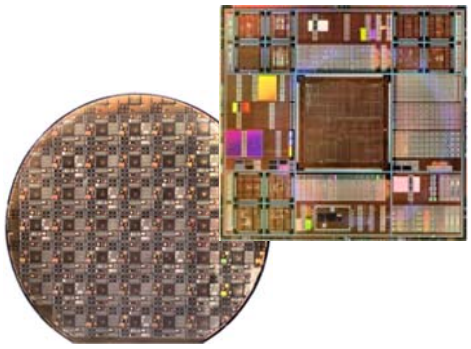
CMOS7 Memory IP

The CMOS7 Memory IP is a collection of rad-hard memories that have been demonstrated on previous products. Each memory package includes the physical layouts, LVS netlists, SPICE netlists, simulation models, and timing libraries that can be used in the design of digital or mixed signal integrated circuits in Sandia National Laboratories 0.35um SOI CMOS7 technology.

The Memory IP available consists of:

- Single port SRAMs
- Dual port SRAMs
- Cache Tag SRAM
- ROMs

These can be modified to generate new memory designs.



Current Offerings:

TYPE	SIZE	DESCRIPTION
SP-SRAM	8Kx8	
	8Kx32	Tacc<40ns @125C
	128Kx8	Tacc=40ns @125C
	128Kx32	Tacc about 40ns @125C
	768x144	Tacc<40ns @85C, without SEU resistors. Will support SEU resistors at slower speeds.
	768x72	Tacc<40ns @85C, without SEU resistors. Will support SEU resistors at slower speeds.
	192x36	Tacc<20ns @85C, without SEU resistors. Will support SEU resistors at slower speeds.
DP-SRAM	128x32	Building block for larger DP-RAMs, Tacc<=20ns @125C
TAG SRAM	256K	
ROM	8Kx32	
	512x32	Building block for larger ROMs, Tacc<=20ns @125C

All device timings are specified at -55C to 125C and with SEU resistors, unless otherwise noted.

Please contact us for more detailed information regarding your radiation and timing requirements.

Future Offerings:

Future offerings will include memory compiler for this technology.

www.sandia.gov/mstc

For more information email snlasic@sandia.gov

U.S. DEPARTMENT OF ENERGY | NNSA National Nuclear Security Administration

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