10 Kw Silicon Carbide (Sic) Based Inverter For Renewable Energy Applications[1]

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I. Introduction

SiC holds the promise of vastly exceeding the capabilities of Si devices by offering higher blocking voltages, lower switching losses and higher operating temperatures. High-voltage (i.e., > 1.2 kV) high-power DC/AC power electronics, such as those used for energy storage applications or used to interface with renewable energy sources, will greatly benefit from the inherent advantages of SiC devices. The utilization of high-power SiC devices is set to revolutionize the power electronics industry and bring the benefit of improved efficiency and improved reliability to the commercial markets while simultaneously benefiting society through improving energy savings on an international scale.

To unlock the full potential of SiC-based power electronics, new electrical and mechanical design approaches are needed that are specifically tailored for SiC devices. Researchers at Arkansas Power Electronics International, Inc. (APEI, Inc.) have performed extensive research in the area of SiC device applications and power packaging, focusing on developing multichip power modules (MCPMs). The MCPM design approach allows for the benefits of SiC at the devices level to be reflected at the system level.

In this paper, the authors present work carried out in the development of a SiC-based fully-functional multi-purpose inverter currently under development at APEI, Inc which uses an MCPM based approach. The paper first presents a short overview of the state of the art of SiC devices (i.e., diodes, JFETs and MOSFETs) that are currently available for these applications as well as an outlook into the near term future of these devices as they become commercially available. Next, the paper focuses on the electrical and mechanical design of a 10 kW SiC based inverter for renewable energy and energy storage applications. Details on the electrical and thermal design approach will be presented. SiC device characterization data is presented and an analysis of performance improvements, including efficiency estimations is presented. Lastly, measured results that were obtained from a similar 4-kW SiC three-phase prototype are discussed.

II. Overview on State of The Art in SiC Power Devices

SiC is a wide bandgap semiconductor material capable of high temperature operation (theoretically up to ~600 °C). When compared to Si-based power devices, SiC power devices have a higher breakdown voltage (~10×), possess lower switching losses, are capable of higher current densities (~3×), and can operate at higher temperatures (~5×) [1-3]. Such power device have the potential to eliminate many of the system design tradeoffs that Si-based systems face today and will yield very efficient and power dense power electronics systems. Figure 1 (left) shows a general comparison of different Si and SiC devices voltage drops. For this comparison, it was assumed that the voltage blocking capability is 1000 V while the bare die area is 1 cm^2. The comparison clearly shows some of the key advantages of SiC devices in term of conduction loss.

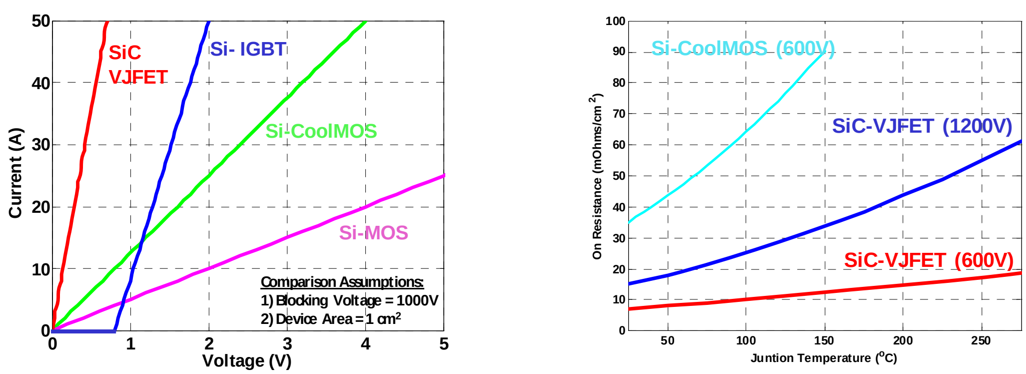

Figure 1. Comparison of several power device voltage drop (left) and comparison of Si and SiC devices on-resistance variation vs. temperature (right).

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Figure 1 (right) shows the variation of on-resistance (per unit of area) of Si and SiC devices. Both technologies exhibit an exponential increase in on-resistance with increasing temperature. However, due to the fact that SiC devices have a smaller on-resistance per unit of area, a 600 V SiC VJFET at 275 °C still has a smaller resistance per unit of area than a 600V Si devices at room temperature [4]. Due to the reduced on-resistance of SiC devices, several design tradeoffs may take place: 1) The device manufacture may choose to design a "smaller area" power device which has similar ratings as an equivalent Si device while saving on material cost. 2) The system designer may choose to use the loss savings (i.e., conduction and switching) to boost system efficiency or. 3) The system designer may choose to utilize the higher switching frequency and high temperature capability aspects of the SiC technology to dramatically increase overall power density. Of course, any combination of the three mentioned scenarios is also possible where the proper mix of the scenarios is determined by economic and performance factors. In any case, the current system design space is greatly increased and design tradeoffs are greatly relaxed by the utilization of SiC technology. Lastly, due to additional advantages of SiC devices such as increased thermal conductivity, increased short-circuit current capability and a square safe operating area, there is great potential for increasing the overall reliability of the power electronic system.

Experimental SiC power devices have been around for over two decades but it was not until 2001 that SiC devices (i.e., Schottky diodes) became commercially available as a standard electronic component. Today several semiconductor manufactures such as Cree, Inc. Infineon, and Microsemi regularly sell SiC Schottky diodes. Presently, several SiC Schottky diodes are available including a 1200V 50A single die diode.

There are no SiC active device commercially available to date. SiC VJFETs can be purchased, however, as engineering samples. 1200V 5mm^2 VJFETs are now available as engineering samples that are nearly commercially quality. The estimated current handling capability of these devices is approximately 30 Amps [4]. Several experimental SiC devices have been demonstrated including normally-on and normally-off VJFETs, SITs, MESFETs, MOSFETs, BJTs and thyristors. Companies like APEI, Inc. have demonstrated the advantages of SiC technology by developing high-performance power electronics demonstration prototypes. Today, the benefits that SiC technology can bring into power electronics systems are clear and device manufactures are aggressively seeking the maturation of manufacturing technologies that will allow them to deliver cost-competitive, high-performance SiC products into the ever-growing power electronics market. SiC semiconductor manufacturers such as Infineon, SemiSouth Labs, Microsemi, Denso and Rohm are presently developing the required commercialization strategies and the first commercial power SiC devices are expected to be released in 2008.

III. 10 kW SiC Inverter Design Approach

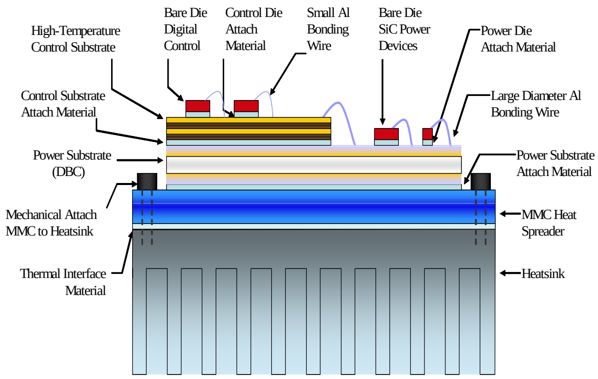
A. Electrical and Mechanical Design Approach

The main design objective of the work presented here is the development of a 10 kW SiC-based fully-functional multi-purpose inverter with improved efficiency (> 96%), large weight and volume reduction (up to 75 %) and similar functionality as commercially available products. Even though the inverter design is multi-purpose (i.e., it can function as a stand-alone inverter, gird-tie inverter or motor drive), a grid-tie solar inverter will be the primary focus of the present development. The output voltage of the inverter is currently being designed for 208 Vrms; the peak power tracking window is selected to be 350 Vdc to 700 Vdc; the maximum ambient temperature is 75 °C. The target weight of the complete system is less than 25 lbs while the target volume is less than 1 cubic foot. Additional ratings include a maximum ac current of approximately 31 Arms, a maximum dc current of approximately 32 A and a total harmonic distortion of the output current of less than 5%.

One of the major contributors to the overall size and weight of a system is the cooling system (i.e., heatsink). The necessary performance of the cooling system can be greatly reduced by increasing the efficiency of the system and/or by increasing the temperature difference between the electronics and the operating environment. As mentioned, SiC can operate at temperature in excess of 500 °C. Unfortunately, the device losses (mostly conduction loss) increases as temperature increases; therefore, there is a tradeoff between system size and efficiency. Based on SiC device characterization and SiC-based inverter prototype measurements, APEI, Inc. has estimated that the efficiency of a SiC-based inverter operating at a junction temperature of 275 °C is at least equivalent to the efficiency of a Si-based inverter operating at a junction temperature of 125 °C. A junction temperature of 275 °C allows for a temperature differential of 215 °C when assuming an ambient temperature of 60 °C (standard design temperature) while the Si-based system allows for only a 65 °C differential. This 3× improvement of the acceptable temperature difference allows for a great reduction of the cooling system.

Another important attribute of SiC devices is higher switching speeds (up to 10×) which greatly minimize switching losses and allow for an increase in system switching frequency. The optimal switching frequency is determined by the tradeoff between switching losses and total harmonic distortion (THD) of output waveforms. Note that THD is generally reduced by the placement of output/input power filters, which dissipate the power of the higher harmonics as heat. To take advantage of the fast switching times offer by SiC devices (i.e., < 20 ns), extremely low parasitic power packaging techniques must be developed that allow for > 1kA/μs and > 50 kV/μs operation. In addition, to minimize signal delays and parasitics the control and gate drive circuitry must be placed as close to the power devices as possible. APEI, Inc. has developed a multi-chip power module (MCPM) packaging concept, presented in Figure 2 (left), which reduces parasitic effects by integrating the controller stage, gate drive stage and power stage of the power system into a single module.

Figure 2 (right) shows a picture of a three-phase 4 kW MCPM prototype built and tested by APEI, Inc. The MCPM utilizes a multiple layer design approach, which separates the power and control circuitry. Note that in order to utilize the potential high-temperature benefits of SiC devices, the MCPM must be designed to operate reliably at high temperatures (i.e., > 150 °C). The MCPM is an advanced packaging approach, which involves several material and processing steps. APEI, Inc. researchers have been working for the past four years in the selection and qualification of packaging materials and processing steps that allow the implementation of high-temperature MCPMs. Present high-temperature MCPM packaging technology allows for the safe operation of power devices at junction temperature in excess of 250+ °C. Detailed descriptions of those packaging technologies can be found in [5-8].



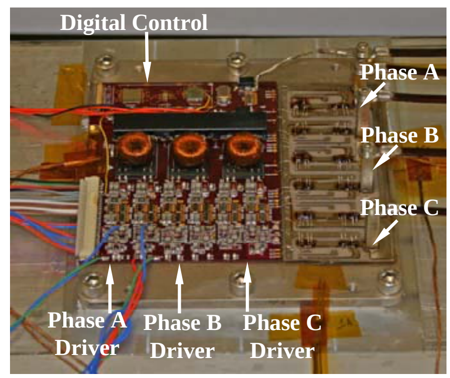


Figure 2. MCPM packaging approach of a SiC-based inverter (left) and picture of 4kW high-temperature MCPM (right).

The electrical design of the 10 kW SiC inverter follows a multi-chip power module (MCPM) approach in which the controller stage and power stage of the inverter are integrated into a single module. This high level of integration allows for the minimization of parasitics. The MCPM inverter is divided into the following blocks:

Control Block: The control block of the inverter generates all control signals. One of the primary factors considered when selecting the components for the control block was the fact that the control block will operate at elevated ambient temperature (up to 150 °C) due to the its close proximity to the power block of the inverter. APEI, Inc. selected the TMS320F2811 DSP from Texas Instruments as the core element for the control block due to its demonstrated rugged operation [5-8]. This DSP family was specifically designed for power electronics applications and, therefore, several on-chip features such as multiple ADC/DACs, PWM units, timers, hardware interrupts, CAN communication, etc. have been included. APEI, Inc. developed its own high-temperature evaluation platform for the TMS320F281x family, which contains most of the elements needed to control a three-phase inverter. APEI, Inc. has performed successful temperature testing of the TMS320F2811 high-temperature evaluation three-phase platform up to 240 °C. Other key components within the control stage such as voltage regulator, were implemented using high-temperature SOI and rated to 250 °C.

Gate Drive Block: The output of the DSP does not have the correct voltage level or current carrying capabilities to drive the gate of a switching position (i.e., up to 7 normally-on SiC VJFET in parallel). Therefore, the proper voltage level and electrical isolation of the signal are provided by the gate drive stage. The DSP outputs are conditioned to deliver the right voltage amplitude, polarity, and current through the gate drive block. High temperature active and passive electronics make up an amplifier circuit that provides the correct voltages to the power devices. The gate signals are then isolated via pulse transformers. Pulse transformers were selected over gate driver ICs (i.e., boost-strap or level-shift methods) due to the improved reliability at high temperatures (i.e., 150 °C).

Power Block: Three single-phase legs (half-bridges) make up the power block. Each switching position is composed of up to four paralleled 10-A, 1200-V SiC Schottky diodes manufactured by Cree and seven 1200V SiC JFETs manufactured by SiCED. The SiC power switches used here are experimental devices, available only as engineering samples, and no current rating was provided by the manufacturer. Based on internal testing discussed below, a current rating of 6 Amps was determined.

B. Testing of SiCED's 1200V 3 mm^2 SiC VJFETs

APEI, Inc. packaged and tested several 1200V 3 mm^2 VJFETs manufactured by SiCED. First several static measurements (i.e., on-state curves, voltage breakdown, on-resistances, etc.) were taken utilizing a Tektronix 371B power curve tracer from room temperature up to 275 °C. Figure 3 shows the on-state plots of the device at room temperature and 275 °C. Note that the maximum junction temperature of the power devices in this inverter may never reach such a high temperature; the final temperature of operation will be determined during the optimization process when investigating the tradeoff between system size, maximum switching frequency and system efficiency. However, to ensure adequate information for this tradeoff analysis, the high temperature characteristics of the SiC devices were also investigated. From the on-state curves it was concluded that the device may carry a maximum current of 6 Amps (or 200 A/cm2) which at 275 °C produces a voltage drop of approximately 11 V.

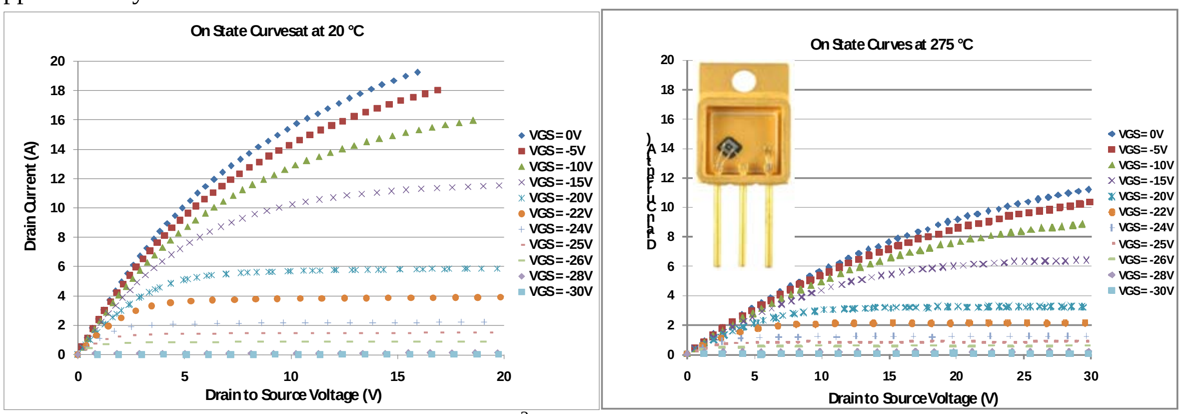


Figure 3. On-state curves of 1200 V 3mm^2 VJFETs at room temperature (left) and 275 °C (right).

In addition to the described static measurements, several dynamic measurements were also performed using a clamped inductor test circuit. These measurements were carried out at room temperature. The particular focus of the measurements was switching loss characterization for different voltages, currents and gate resistances. Figure 4 shows the voltage, current and power at turn-on and turn-off of the 1200V 3 mm^2 VJFETs for a gate resistance of 5 Ohms, load current of 6 A and a drain to source voltage of 300 V. Under these operating conditions, it is estimated that the turn-on loss is approximately 20 µJ while the turn off loss is approximately 25 µJ. Figure 5 (left) shows the total switching energy of the SiC VJFET versus drain current for different gate resistances and a constant drain to source voltage of 300 V while Figure 5 (right) shows the switching energy of the device for different drain to source voltages for a gate resistance of 20 Ω and a constant load current of 6 A. Using the devices data presented in the previous section to estimate switching losses and well-known conduction loss equations for inverters, the efficiency of the inverter can be estimated [9-10]. To carry out this estimation, the following assumptions were made: 1) The housekeeping power supply utilized to power the DSP-based controller circuit, sensing circuitry and portion of the gate driver draws less than 25 W of power. 2) Efficiency is estimated at 150°C junction temperature. 3) The gate resistance is 20 Ω. 4) Switching losses were estimated using linear interpolation of measured data. 5) Switching frequency was set at 25 kHz. 6) Each switch position is composed of seven 1200V 3mm^2 VJFET and four 1200V 10 A Schottky diodes. Under these conditions, the inverter efficiency is greater than 98% at full power and for a dc link voltage of 350 V. The inverter full power efficiency at 700 Vdc exceeds 97%.

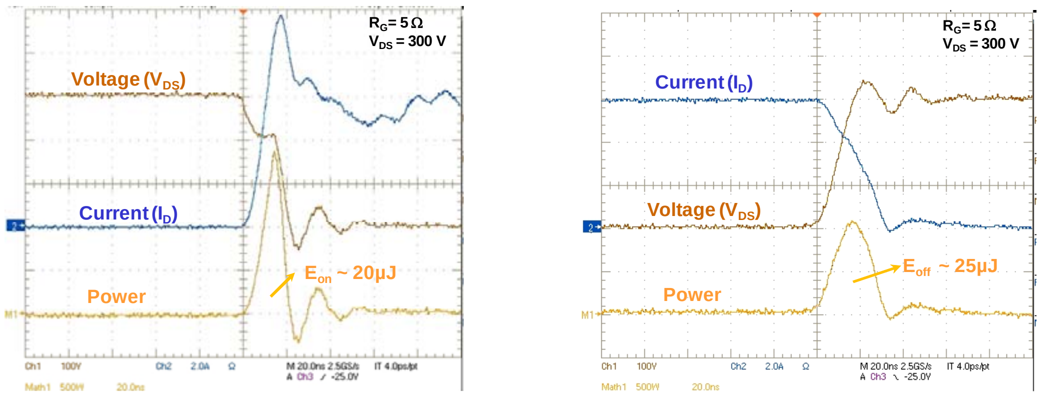


Figure 4. Turn on (left) and turn off (right) waveforms of the 1200V SiC VJFETs (R_G= 5 Ω and V_{DS} = 300 V) (right).

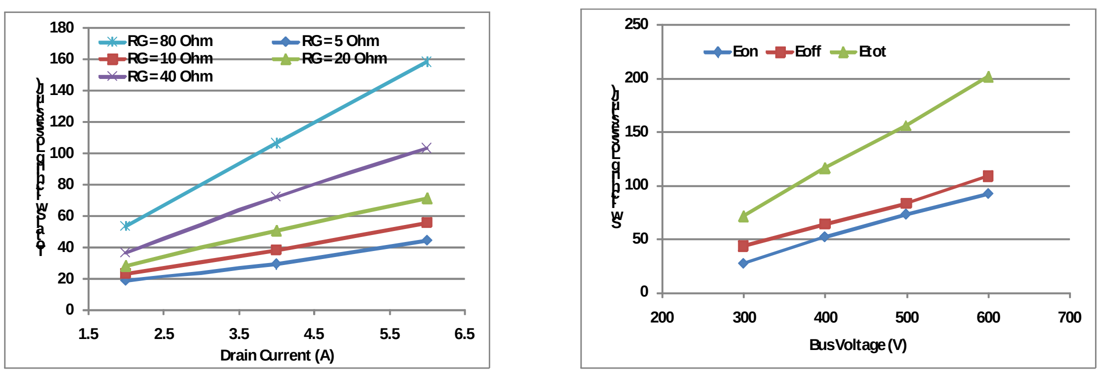


Figure 5. Switching energy vs. drain current (V_{DS} = 300V) for different gate resistances (left) and switching energy vs. drain to source voltages for a R_G= 20 Ω and Id = 6A (right).

IV. Testing of a Three-Phase 4kW Inverter Prototype

APEI, Inc. built and tested a three-phase 4 kW SiC-based inverter MCPM following the previously described electrical and mechanical design approaches (See Figure 2 (right)). The module utilizes two 1200V 3mm^2 VJFETs and two 1200V Schottky diodes per switch position. The module was tested at different power levels and from room temperature to 250 °C measured at the baseplate. The output of the inverter was low-pass filtered using a Y-connected LC filter. The filtered three-phase output was then fed to an RL load with high power factor (>0.98). The following measurements were obtained while operating at full power and with a baseplate temperature of 250 °C (or ~ 300 °C junction temperature of the power devices). The input voltage was 600 Vdc and the switching frequency was 25 kHz.

Figure 6 (left) displays the three-phase line to neutral load voltages measured after the LC filter (Ch. 1-blue, Ch. 2-cyan, Ch. 3-magenta) and the DC bus voltage (Ch. 4-green) supplied to the module. The measured line to neutral voltages translates into over 230 Vrms line to line. Figure 6 (right) shows the three phase currents supplied to the resistive-inductive load following the LC filter (Ch. 1-blue, Ch. 2-cyan, Ch. 3-magenta) as well as the unfiltered DC link input current (Ch. 4-green). A Hioki power meter was used to accurately measure the input and output power of the MCPM including the filter to determine the efficiency at full power. Minor adjustments to the control software were made to increase the amplitude of output voltages relative to what is shown in Figure 6. This was done in order to achieve full 4 kW operation. During this test, the input measured 4.02 kW while the power dissipated by the resistive load (i.e., after LC power filter) was measured at 3.77 kW. This results in an overall system efficiency of 93.8%. Based on thermal measurements and loss calculations previously described, the efficiency of the three-phase inverter operating at an ambient temperature of 250 °C (or ~ 300 °C junction temperature of the power devices) and 600 Vdc bus was in excess of 96 %. The efficiency of the three-phase LC power filter stage was estimated at approximately 97.7 % (or ~ 90 Watts of loss). Conduction loss of the LC filter at full power was estimated to be less than 10 W while the rest of losses were dissipated high-frequency harmonics.

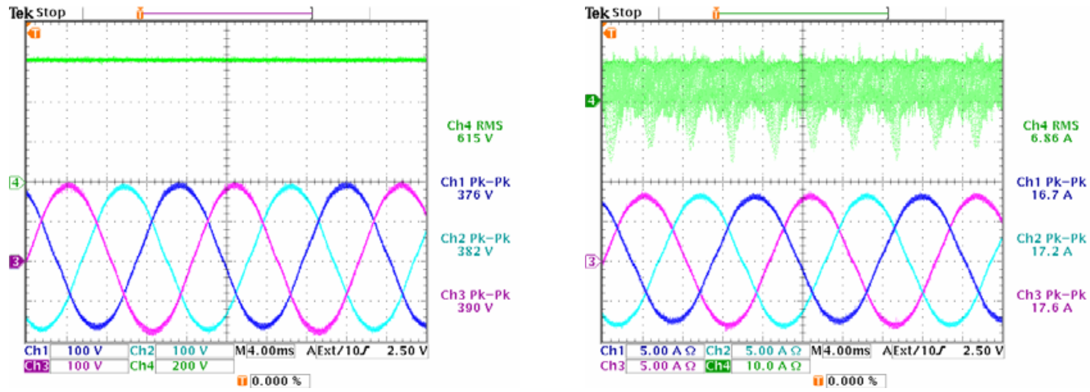


Figure 6. Filtered three-phase line to neutral voltages and DC bus voltage (left), and three-phase filtered load currents (blue, cyan, magenta) and unfiltered DC input current at 250 °C baseplate (right).

V. Summary

In this paper the authors presented work carried out during the development of a SiC-based fully-functional multi-purpose inverter MCPM. The paper first presented the advantages of SiC devices and their implications at the system level. Next, APEI, Inc.'s design approach was presented and discussed. Then, measured static and dynamic characteristics of the SiC devices utilized for the inverter were presented. Based on those measured results, estimated efficiency figures were discussed. Measured results obtained by testing a similar 4-kW SiC three-phase prototype were discussed.

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