High Power Silicon Carbide Inverter Design – 100kW Griud Connect Building Block[1]

Leo Casey (SatCon Technology Corporation; Boston, Massachusetts, USA); leo.casey@satcon.com
Bogdan Borowy and Gregg Davis (SatCon)

Acknowledgements: This paper describes work being sponsored by the DOE and supervised by Dr. Imre Gyuk of the DOE Energy Storage Program and Stan Atcitty of Sandia National Laboratories.[2] The authors also need to acknowledge Northrop Grumman, Cree, SemiSouth, ONR, AFRL, ARL, DARPA, DOE, SANDIA and TARDEC for either providing financial support for work on SiC or for providing device samples or data which this project either utilizes or builds on.

Overview: In an age of increasing electrification the ability to implement the electronics in a smaller, lighter and more robust package is very important and this is certainly true for Energy Storage applications with round-trip efficiency and system reliability benefiting directly. Wide Band Gap semiconductor devices, such as Silicon Carbide (SiC), potentially enable higher frequency operation, lower the power dissipation and offer higher temperature operation than today's Silicon based power conversion technology. The increase in frequency promises a dramatic reduction in volume and weight of the power converter. The higher temperature operation allows for more efficient heat transfer, smaller heatsinks, and the operation of systems with high temperature coolants (>100°C). These are critical features for all power conversion applications with the potential of improved performance, reduced size and weight, and more rugged and reliable systems. This paper addresses the utilization of SiC technology for grid-connected electronics for energy storage applications and uses a modular inverter design as the example. The beauty of a standard building block module is, of course, that it can be integrated into many different systems and so economies of scale can be readily achieved.

This is a large topic as there are many technical issues, well beyond those of materials and devices, to be solved before full SiC systems, taking full advantage of the technology, can become a reality. This paper describes these issues and some of the solutions but proceeds under the assumption that these challenges can and will be overcome. This leads to a discussion of the benefits of both hybrid Si/SiC and full SiC power conversion technology for Utility scale Energy Storage Systems, including a discussion based on projections of the economics of SiC power conversion technology.

Silicon Carbide Potential as Power Semiconductor: The key materials advantages of SiC are factor of 10 higher breakdown field, higher thermal conductivity and wider bandgap. The higher bandgap is what permits semiconductor devices with higher activation energies and so higher temperature and radiation environments. The higher field strength permits proportionally smaller drift regions, with SiC devices achieving greater than 100 V/µm vs. the 10 V/µm of Si. At the same time the high gradient in field strength allows the drift (so called intrinsic) region to be much higher doped than in Si. The overall advantage is approximately two orders of magnitude reduction in the resistance of the drift region of the Power device. The third significant point is the superior heat conductivity of the material. Whatever heat is produced is easier to get out. For power devices where the heat is typically produced several 100 microns below the surface this is quite significant. A final advantage of SiC is dramatically lower minority carrier lifetime which permits minority carrier devices, such as bipolar junction transistors with very fast switching times.

Potential Silicon Carbide Impact on Grid: An area of electrical technology that is still largely electromechanical is that of relaying, particularly at high voltages where solid state solutions are both difficult and inefficient. SiC, power, solid-state-relays would be very attractive with almost instantaneous switching when compared to 6-10 cycle breakers. Solid state High Voltage relays could be used for isolation, protection, fault clearing and fault limiting. The natural current limiting nature of a FET structure would have tremendous impact limiting currents during faults or re-energization of faulted lines.

---

[1] Funded by the Energy Storage Systems Program of the U.S. Department Of Energy (DOE/ESS) through the Small Business Innovation Research (SBIR) program, and managed by Sandia National Laboratories (SNL).

[2] Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Meanwhile in the existing arena of Medium Voltage and High Voltage Transmission Electronics, large power conversion devices such as flexible ac transmission systems (FACTS) reactive power generators (SVAR, DVAR), dynamic voltage restorers (DVR) and static transfer switches (STS) all have to use stacked combinations of switching "valves" today. This would be greatly simplified and performance enhanced with high voltage SiC devices. Using high-frequency isolated links to avoid the volume and weight of line frequency transformers is routine at utilization voltage levels, SiC could well make this an option at transmission and distribution voltages as well. Turning to grid electronics for applications such as storage, renewables and power quality, SiC technology promises advantages in volume, weight, efficiency, reliability, total cost, overload capability and the available voltage and power range. Another application might well be in surge and spike suppression, taking advantage of the speed, ruggedness and thermal properties of the material. This would use the device across the line as opposed to in series. A good surge suppressor needs to absorb energy and SiC would seem to be ideal. It also raises the possibility that SiC power devices in a power converter, with adequate sensing and drive, could be self protecting eliminating the need for MOVs which are a reliability problem. Silicon Carbide Rapidly Maturing: [1] While Silicon Carbide does not occur naturally it is well known to us as the Industrial abrasive carborundum. As an electronic material there are particular challenges stemming from two major points:

1) SiC has no liquid state. This means that most Si processing techniques from crystal pulling, zone refinement, to Rapid Thermal Processing have little application to SiC. SiC must be grown by CVD or sublimation. SiC is ideally doped as it is grown, as ion implantation requires very high energies and so elevated temperatures to minimize crystal damage.
2) SiC has approximately 200 Xtal structures, or polytypes. Growing large SiC wafers of a single crystal structure is very difficult, and the wafer is likely to have defects such as micropipes, screw dislocations and basel plane defects.

There are still materials issues to be solved but nevertheless, in the last 5 years the advances in processing and materials have been truly dramatic. Fueled by the demand for high-quality 4 inch SiC wafers as substrates for Gallium Nitride LEDs, the Industry, in the primary manifestation of Cree, has developed high-quality wafers and now has more than three suppliers of commercial SiC Schottky diode die (Cree, SiCed, Rockwell).

SiC Power Device Summary: A summary of the state of the art in SiC devices is shown below in Table 1. This table is based on characterization of devices or data obtained from Cree, SICED and SemiSouth. This is not a "best-of" or "hero" list but a list of devices that can be obtained with reasonably consistent parameters. The only commercially available devices at this time are the power Schottky devices, although SiC RF devices are commercially available. A Cascode configuration of a SiC JFET and a Si MOSFET has been promised for some time by SICED, and should be the first commercially available, controllable, SiC power device. Cree's 1200V, 50A Schottky device is just now becoming available commercially and a larger 6.4mm x 6.4mm die, with 75A capability, is now being sampled.

Device	Voltage (V)	Current (A)	Demonstrated Switching times
Schottky	600 1200	150 75	ns
PIN	20,000	20	~10ns
Bipolar	1200	20	~100ns, β ~30
MOSFET	1200	10	~100ns
JFET	10,000 1,200	1 20	~100ns

Table 1: State-of-the-Art SiC Devices

The JFET is a very attractive device, and is a close relative of the HEMTs and MESFETs used in RF amplifiers. As a power device it has the difficulty of being normally-on which requires a paradigm shift for the typical power electronics designer (normally-off devices have been fabricated but with 1/3 of the current capability of the normally-on devices). There are also compromise devices that are either partially on or have reduced blocking voltage which can then be enhanced with bias. These devices can be a good fit with dc/dc converter applications as the switching voltage stress is typically a factor or two or more greater than the static off-state voltage. The cascode connection of the JFET power device with a low-voltage device is growing in popularity. SiC bipolar devices are maturing and are serious candidates for commercial application with their fast switching characteristics, but there are remaining issues with forward voltage and β drift with temperature. Meanwhile, the SiC MOSFET, which is targeting high-temperature automotive applications, is rapidly improving but the quality of the oxides is still suspect and IGBTs are still quite a way off due to inability to form highly doped P type SiC material.

An exciting new device is the all SiC Cascoded JFET, which has just been described by Northrop[2]. This device combines the low losses and high current density of the JFET and with the cascoded configuration achieves the normally-off style of power switch control that Power Electronics engineers are familiar with. The device today combines separate high-voltage and low-voltage devices in a hybrid package but there are plans to fully integrate the device.

Silicon Carbide Inverter Design: This SiC inverter design builds on previous work with SiC devices and with the major SiC manufacturers. As the devices have matured they have been characterized, modeled, packaged and applied, with the most recent work culminating in the 7.5kW all SiC inverter[3] shown in Figure 2. This inverter uses paralelled SiC bipolar transistors and Schottky diodes, paralleling four SiC devices with excellent current sharing as shown in Figure 1. This inverter was developed for an automotive application and uses 600V devices with a 400V dc bus. The 100kW grid connected inverter by contrast requires 1200 V minimum devices for a 750—800 V dc bus. The Silicon Inverter module that we are using as a benchmark is shown in Figure 3. It is a three-phase voltage sourced inverter, it operates at a switching frequency of 5.7 kHz with hard switched pulse width modulation, at 1 per unit (pu) it delivers 100kW at 480V, 120Arms. The inverter uses IGBT modules with fast recovery epitaxial diodes.

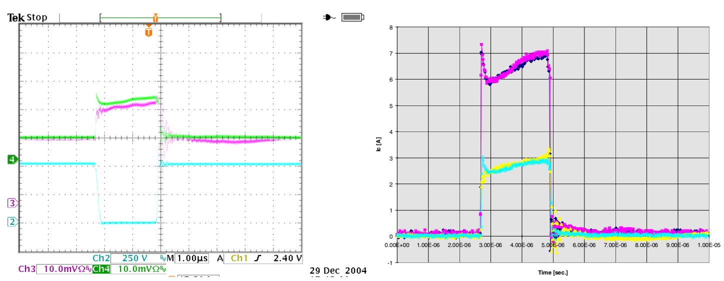

Figure 1: Dynamic Paralleling of SiC Bipolar Devices

To understand the impact of superior Power Semiconductor devices on a design it is important to understand the design process. A converter/inverter design begins by establishing performance criteria which then determines device ratings, features such as overload requirements need to be identified at this point as it impacts active, passive and thermal components (if the magnetics saturate at 1 pu current then you have a 1 pu design regardless of the capability of the power devices). Within the performance criteria is a target efficiency which is key to device selection. The combination of devices and efficiency dictates switching frequency, hence switching loss, and conduction loss. That in turn, with suitable power quality targets, such as IEEE 519, dictates the values of L and C for the main filter elements, although there is some latitude in trading off L for C with the corner frequency of the filter being the critical parameter. The design then moves to thermal design, gate drives, controls, sensing, protection, packaging, software and the like. As we have said we must take care that these related design elements do not become limitations on the design. It is essential to realize that SiC power devices are not drop-in replacements for Silicon switches so circuit topology, control, thermal design, advanced passives and integrated packaging are all critical elements of a Systems driven design to fully realize the potential of the technology. For SiC we must ask ourselves can we package it? can we get the heat out? can we drive it adequately? can we sense it? can we control it? Are the passives adequate? If the SiC power circuit is operating at 10 times the frequency of Si power circuits these answers are not necessarily trivial.

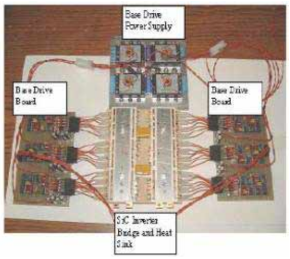

Figure 2: 7.5kW SiC BJT Inverter

Figure 4: 100kW Inverter Module

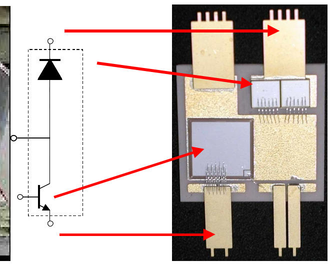

Figure 3: Hybrid Si/SiC Module

If we can use an advanced semiconductor technology, with much faster switching times than Si, we have a choice as to whether to save energy (increase efficiency) or whether instead to save volume and weight of the filter components. If we are looking for improved system dynamics we need to push in the direction of reduced filter elements. Generally, the sum of the switching transition times ($t_{on} + t_{off}$) sets f_{sw}, as the losses go approximately as V.I.($t_{on} + t_{off}$)/2. For Si IGBTs with transition times of 1μs 1% of switching loss would dictate a switching frequency of 10kHz. Now, for a SiC cascoded JFET with transition times better than 100ns the switching frequency could be 100kHz for 1% switching loss. We have gone beyond the device characterization to develop device and system models which have allowed us to carry this SiC design study through. The system results are summarized below in Table 2. The filter elements have been reduced by an order of magnitude so the entire system volume and weight is expected to be 30% of the benchmark, alternatively the conduction and switching losses can be reduced by approximately 80% in the full SiC design. Hybrid Si/SiC Design: Above we discussed the switching losses with no mention of the rectifier losses. In fact today approximately 1/3 of the losses are in the rectifier due to its slow recovery and some of the IGBT losses, particularly at turn-on are due to the rectifier. Our experiments and simulations indicate that approximately half of the switching loss can be saved by replacing the Si fast recovery diode with a SiC Schottky diode. This is a critical step along the path to SiC adoption and will serve to validate some important aspects of the technology, particularly the metallization and interconnect of the SiC die themselves. For our existing Si Inverter module, where the total swiching loss is appoximately 2% this change should improve the efficiency by 1%, or reduce the losses by 25%. Figure 3 shows a hybrid Si/SiC switch module that is under development.

	Silicon SOA	Full SiC Design
Size/Density/Efficiency	10 -- 100 W/ In³ (16 for module)	50 -- 500 W / In³ (80 for module) (25% Vol., 20%P)
Cooling	80ºC max. liquid or 25 ºC Air	>100ºC liquid or 40-50 ºC Air
Response Time	10 ms for 5.6 kHz with V and I loops	50 µS for 100kHz with dead-beat control
High Temperature Design	Si limits entire system to < 110ºC	Partial High-Temperature design then eventually complete High-Temperature design if needed (analog degradtion)
Overload Capability	100-500 ms	10+ seconds
Robustness	10-20,000 hr. MTBF	50-100,000 hr. MTBF

Table 2: Si vs SiC Inverter Design

Systems Approach: Operating electronic devices at higher switching frequencies and/or at higher device temperatures does not necessarily imply reduction in filter elements and shrinking the associated heat sinks. To achieve the full benefit of SiC electronics it is essential to increase/improve the performance of the overall system in all areas. An example is that if the control bandwidth is not improved proportionally to the increase in switching frequency then the total Bulk energy storage requirement is not actually reduced. A true systems approach is therefore necessary with some pertinent points shown in Table 3, along with the anticipated impact on a SiC inverter.

	APPROACH	IMPACT
1	SiC power devices	Higher frequency, higher temperature, lower loss → smaller, lighter, more robust
2	High frequency enables minimization of filter inductors and capacitors and Bulk Capacitors	Reliable and robust Lower line harmonics and input ripple Reduction of common mode on line
3	Dead-Beat Control	Faster inverter response
4	Feed-Forward control from source and line	Minimize storage and response times
5	Wide frequency range	Non-linear control techniques, faster control, faster source and line response with reduced sensitivity
6	Cascode topology	Logic + Normally-on = Normally off power
7	CSI (Current Sourced Inverter)	More Compatible with Normally-On devices
8	Integrated "smart" Gate Drivers	Enhanced noise immunity at higher switching frequencies. Increased reliability (temperature/current equalization)

Table 3: Systems Approach to SiC Inverter

There are many other areas to address from passives, packaging, heat removal, thermal expansion, metallizations, electromigration, Gate Drives (basic and advanced), controls (particularly non-linear) signal electronics and high-temperature electronics. Space restricts our comments to a few areas but these are all topics that power electronic system engineers have a thorough grasp of and are adapting that knowledge to SiC applications.

Signal Electronics for Sensing, Control and Drives: Some environments, such as downhole or inside Reactors, demand all high-temperature electronics and components. Failing this the non-high-temperature parts need to be cooled below the surrounding ambient and this type of thermally segmented and actively cooled system is necessarily complex. The ideal is for the signal electronics to have the same high-temperature capability as the power electronics, whether for normal operation or sustained overload capability. Non-operating, or non-energized, Silicon does not degrade at temperatures as high as 300°C[4] as the solid-state diffusion coefficients are still low in this temperature range. The reason that today's Silicon circuits can not operate above 175°C or so is that the reverse biased junctions become leaky, which leads to thermal runaway with local hotspots and elevated temperatures which do allow solid-state diffusion and so permanent degradation. The leakage current is an exponential function of temperature so there is a hard limit placed on operating temperature.

The only high-temperature Control technology today that can be used reliably at 300°C is the thin-film Silicon SOI from Honeywell or Peregrine.[6] The weakest link in the packaging to date has been the aluminum interconnect and particularly the effects of electromigration. Honeywell's approach has been to operate with incredibly low current densities. Peregrine have been experimenting with copper which seems very promising.

Packaging: The mortal enemies of reliable electronics are elevated temperature (T), temperature cycling (ΔT) and thermal shock (dT/dt). These are the drivers for all of the failure mechanisms that lead to device and system failure. At the same time there are compelling reasons to operate at elevated temperature, specifically:

1) High Temperature ambient environments, such as for downhole instrumentation, require electronics to operate well in excess of 200°C.
2) Minimization of Power Electronics or RF system size and weight by reducing the heat sinking requirements.
3) Increasing the Ruggedness of electronic systems by allowing for surges in power and so occasional excursions to higher than normal operating temperatures.

Silicon Carbide (SiC) and other Wide Band gap (WBG) semiconductor materials permit significantly higher temperature than the 150-175°C junction temperature range of today's Silicon (Si) power devices. To be able to operate at these temperatures for sustained periods of time and to be able to cycle in temperature between the ambient temperature and the elevated operating temperature the packaging must be designed to accommodate this. The key elements of this high-temperature packaging solution are minimal number of layers, good thermal transfer and extremely good matching of thermal coefficients of expansion.

Economics of SiC Adoption: Silicon Carbide is a comparatively expensive technology and liable to remain so even as it becomes more mature. It is not just that Silicon is a dominant, well developed technology but the fact that the processing temperatures and energies of SiC are considerably higher and so inherently costlier in terms of time, energy and ultimately money. How much costlier is of great interest of course and will be critical to allowing us to evaluate the costs against the benefits for many future applications. Some applications for WBG semiconductors are not particularly cost sensitive of course as the high-temperature, or high-radiation or even high-voltage capability is the enabling feature for the application. Many other power conversion applications can benefit from savings in volume or weight or improved performance in the form of dynamic response or efficiency or overload capability. The best estimates are that SiC could eventually approach to a factor of 3 the cost of Silicon when compared on an equal current rating basis. We will use this 3x multiplier to evaluate the potential cost effectiveness of SiC technology using the hybrid Si/SiC module as a basis.

Using the 100kW grid connected inverter example we find that today approximately 4% of the cost of the system is actually in the power semiconductors, while 11% of the cost is in the main filter components. If we consider a hybrid Si/SiC design where the cost of the SiC diodes is twice that of the equivalent current rating of the Si epitaxial diodes, which are themselves 1/3 of the cost of the semiconductors, then the savings in the magnetics (and capacitors) more than compensates for the increase in cost of the semiconductors. This might at first seem surprising but the fact is that copper and iron have been increasingly dramatically in price, particularly copper, over the last several years while the semiconductor industry has been in the doldrums. The first case uses the doubling in switching frequency to halve all of the energy storage components, in the second case we disproportionately reduce the magnetics while keeping the capacitance the same. This keeps the filter corner frequency the same but changes the characteristic impedance of the filter, which translates into higher ripple currents.

There is an altogether different calculation that we could perform based on approximately 1% increase in operating efficiency, or approximately 2% improvement in round-trip efficiency. For the 100kW Inverter, feeding a 200kWHr battery, with a once per day charging cycle such as those used for the transmission feeder power smoothing application we could then claim a 2kWHr saving of off-peak energy, which we will ignore and then an additional daily availability of 2KWHr of peak electrical energy. The value of the peak energy is somewhat controversial but if we were to use the German feed in tariff for PV as an indicator (~55 c€/kWh) we could argue that the 1% of efficiency is worth US $1/day, or with a 20% return on investment approximately $1,800. Without being too specific this is on the order of 10% of the parts cost of the inverter and so the increase in cost of the semiconductors in moving to a hybrid Si/SiC IGBT module is easily justified in savings due to improved efficiency. Similarly, we could argue that organizations such as the CEC have put a monetary value on KW capability of up to $3.50/watt and so the 1% efficiency improvement would have a direct monetary value in a subsidy situation of up to $3,500. Given the realistic nature of the subsidy calculations today based on averaged efficiencies for PV and Fuel Cell inverters it is quite likely that a round trip efficiency number would be used. Also, consider that we are dealing here with a single stage Inverter discussion, whereas in the energy storage system there will likely be two stages of conversion.

	Today's Si Design	Hybrid Si/SiC-1	Hybrid Si/SiC-2
Semiconductors	4.11	6.81	6.81
Magnetics	9.83	4.91	2.455
Filter Caps	1.7	0.85	1.7
Heatsinks + Hardware	2.4	1.2	1.2
Fans	1	1	1
Sum (% of total parts cost)	19.04	14.77	13.165

Table 4: Percentage Costs for Si/SiC Inverter

A full evaluation would be very interesting. As the size and weight come down many of the mechanical components including the main cabinet will shrink. EMI/RFI should be less of an issue. The conduction losses in the magnetics will be reduced. The tradeoffs are complex and non linear.

Summary: Silicon Carbide technology is rapidly maturing and will impact all Power Conversion applications including grid connect electronics for energy storage. Design and analysis of 100kW Inverter applications indicates that a full SiC system will occupy approximately 30% of the volume and weight of today's system or alternatively could save 80% of the conduction and switching loss in the same volume. Similarly, hybrid Si/SiC technology available today can save approximately 30% of either the volume or weight or 25% of the energy being dissipated (half of the switching loss). This provides the designer with choices and trade-offs. The economics look as though they will be more than reasonable once Silicon Carbide costs come down to some reasonable multiplier of Silicon. This is in large part driven by the relatively small cost of the Silicon semiconductors in today's inverters, only 4% for the power devices in the inverter we have been examining. There are many further tasks and challenges to be addressed before full SiC power conversion systems become a reality but the allure exists and the system tradeoffs provide a good context for examining and evaluating the various benefits.

References:

[1] "SiC Microwave Power Technologies", R. Clarke and J. Palmour, Proceedings IEEE, Vol. 90, No. 6, June 2002.

[2] "Silicon Carbide JFET Cascode Switch for Power Conditioning Applications", T. McNutt, V. Veliadis, E. Stewart, H. Hearne, J. Reichl, P. Oda, S. Van Campen, J. Ostop, R.C. Clarke, IEEE Vehicle Power and Propulsion Conference, September 2005

[3] "Issues and Solutions in the Realization of a 5 HP Silicon-Carbide Motor Drive for Military Vehicle Applications", B. Borowy, L. Casey, E. Wagner, T. Burke, G. Khalil, AECV 2005

[4] "Fully-depleted SOI-CMOS technology for high temperature IC applications", B. Gentinne, J.-P. Eggermont, D. Flandre and J.-P. Colinge, Materials Science and Engineering, B46, pp. 1-7.

[5] "High-Temperature Electronics-A Role for Wide Bandgap Semiconductors?", P. Neudeck, R. Okojie and L. Chen", Proceedings IEEE, Vol. 90, NO. 6, June 2002

[6] "High Temperature SOI CMOS Electronics Development - The Deep Trek Project", E. Mallison, John Rogers and Bruce Ohme, Honeywell: Defense and Space Electronics Systems and United States Department of Energy, September 2005.