# Feasibility Analysis and Testing of a Utility Grade Advanced Power Inverter (API)

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***Abstract*- Increased electricity demand amid infrastructure development restrictions continues to foster innovation for distributed generation. However, advances in power converter efficiency, power density, and flexibility are required to enable competitive distributed generation methods to be realized. Wide Band Gap (WBG) semiconductors offer benefits of increased efficiency, higher power density, and simplified thermal management at utility power levels. We aim to use these emerging devices to improve the value proposition of energy storage based distributed generation by increasing power density and eliminating 60 Hz magnetics as well as liquid cooling. Creare is developing a full-scale, containerized grid tie energy storage system with greater than twice the power density over existing converters. This technology will find immediate commercial application to distributed electrical power generation equipment. Elimination of 60 Hz magnetics and liquid cooling provide benefits of reduced cost, greater revenue potential, increased source flexibility, and improved efficiency.**

***Keywords*- silicon carbide, energy storage, utility**

## I. Introduction/Background

Energy storage units that provide distributed power generation are becoming desirable for grid stabilization and revenue growth [1]. However, large equipment size, high capitalization cost, and unacceptable reliability have created an opportunity to develop an innovative solution to satisfy market needs. The goal of this project is to develop an innovative Advanced Power Inverter (API) that enables penetration into these markets. The API technology (Fig. 1) addresses one of the largest needs in grid-tied energy storage units: incorporation of a smaller, lower cost, higher reliability inverter to improve their value proposition. Fig. 1 illustrates the approach for developing the API inverter, which is a combination full-bridge DC-DC converter and Three-Level Neutral-Point-Clamped (3LNPC) inverter using emerging high-voltage SiC MOSFETs [2, 3, 4, 5]. Our product is an SiC MOSFET-based API that we will incorporate into an existing grid tied energy storage container product line aimed at the utility industry. While existing power inverters use traditional silicon semiconductors such as IGBTs, our inverter utilizes Wide Band Gap (WBG) SiC MOSFETs that can operate at higher voltage, temperature, and frequency. These attributes will enable direct connection between the inverter and grid interface, and reduce overall cost and size of the inverter. Fig. 2 shows a computer model of the electronics module as well as a concept for how the electronics module is integrated with other components to form the API. The API is only 1.75 $m^3$ in size, and achieves substantial size reductions when compared with existing products by replacing the liquid cooling with forced air convection cooling and the large 60 Hz transformer with a high frequency transformer having one-tenth the size.

Table 1 compares API size with commercially available inverters. In addition, existing inverters have 480 V or 208 V outputs that require an additional transformer, such as the Temco medium voltage transformer (480:12.47 kV, three-phase 500 KVA, 5.3 $m^3$, $32,000) to achieve 12.47 kV. This roughly doubles the required size and substantially increases cost.

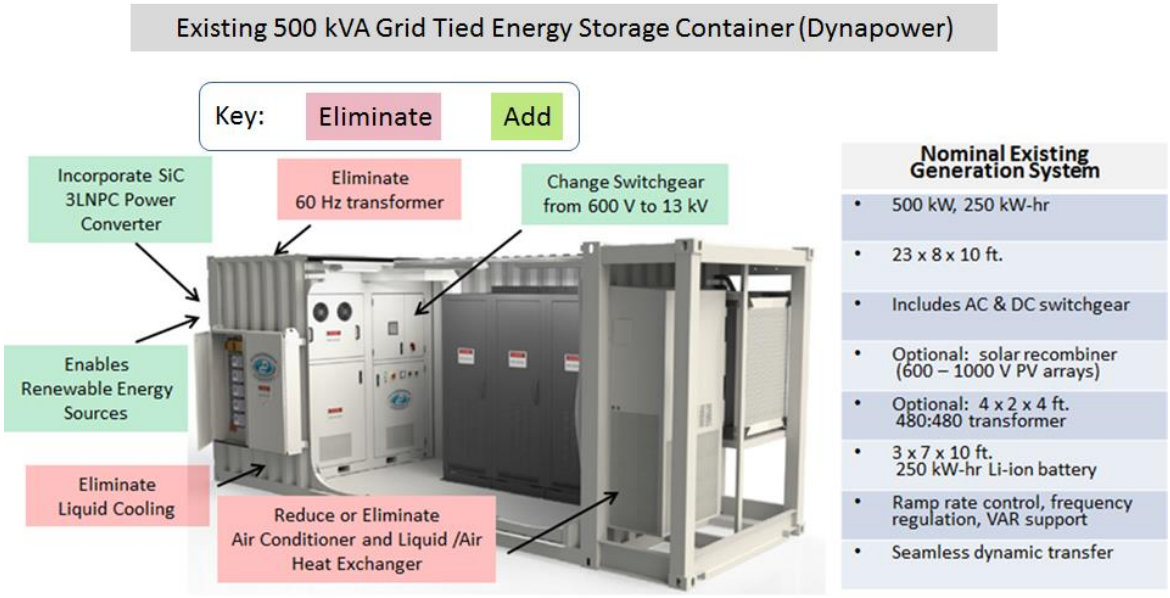



Fig. 1. A transformerless medium voltage grid-tied inverter uses a novel power conversion architecture and SiC semiconductors to eliminate the 60 Hz transformer and liquid cooling.

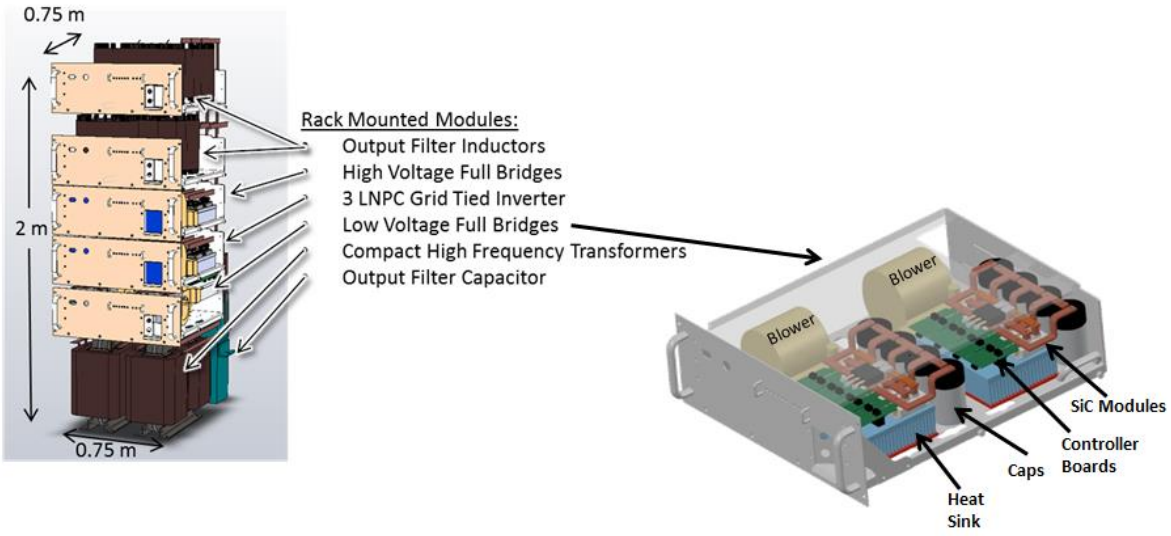



Fig. 2 Creare's API – Packaging details. Substantial size reduction is achieved by elimination of liquid cooling and transformer.

TABLE I
INVERTER SIZE
COMPARISON

| Manufacturer | Size ($m^3$) | Voltage | Power (kW) |
|---|---|---|---|
| Creare | 1.75 | 12.47kV | 500 |
| Dynapower | 4.6 | 480V | 500 |
| Advanced Energy AE500NX | 4.8 | 480V | 500 |
| Solectria SGI500 | 5.9 | 208V | 500 |
| SMA America 500 | 7.0 | 480V | 500 |
| Satcon Tech. PVS500 | 9.4 | 480V | 500 |

## II. RELATED WORK

Six important aspects establish a sound basis for this work. First, the U.S. Department of Energy (DOE) and others have presented data that show the markets for containerized energy storage inverter systems are expanding, and availability of power dense and cost effective power converters will assist these market expansions [1]. The cited report points out that to be cost effective in the near term, system capital cost must be less than $250/kWh, levelized cost must be under 20 ¢/kWh/cycle, system efficiency must be better than 75%, cycle life must exceed 4,000 cycles, and capital costs must be less than $1,750/kW. We believe the API will meet or exceed all of these objectives. Second, data from several researchers have demonstrated that SiC MOSFETs outperform Si IGBTs for medium grid-tie applications [5]. Data indicate that SiC MOSFETs achieve higher frequencies (reducing magnetics size), greater power density, and less loss than series connected Si devices. Third, 10 – 15 kV SiC MOSFETs are available for this work, and we have received and successfully tested 10 kV MOSFETs [5, 6]. Fourth, prior work has successfully demonstrated the use of high-voltage SiC MOSFETs for transformerless grid-tie inverters [7] using bridge-type inverters and boost-type converters. Fifth, using a 3LNPC inverter and novel control algorithms can achieve better harmonic and efficiency performance than a traditional two-level inverter [4]. Finally, while some companies already offer medium-voltage utility interfaces using Si IGBTs, there is no complete system available that incorporates high-voltage SiC power conversion to improve power density, efficiency, and cost [2,3,8]. Taken as a whole, prior work by our team and others establishes a sound basis for the proposed work.

## III. CREARE'S API

### *A. Conventional Utility Inverter Architecture*

A schematic of a conventional grid-tied inverter is shown in Fig. 3 where a two-level, three-phase inverter converts 1 kV DC to 480 V AC output voltage. A low-voltage to high-voltage 60 Hz transformer is then used to interface to the 12.47 kV AC electric grid. A primary goal in this work was to take advantage of the high-voltage capability, fast switching speed, and high temperature operation of SiC semiconductors to eliminate the 60 Hz transformer and the liquid cooling system.

The packaging strategy is modeled on the Dynapower Powerskid system, which is widely marketed. This is a 1 MW+, 12.47 kV AC standalone inverter in a separate enclosure from the battery system. Power levels of 500 kW to 1 MW+ are appropriate for the 12.47 kV interconnect, so this approach is believed to be broadly marketable. Since the inverter and the battery are separable, the inverter can be truly "battery agnostic," which also improves marketability. There is already a proven market for these container systems, since Dynapower has built and sold 12.47 kV AC systems at this power level using 60 Hz interconnect transformers. Choosing this approach enables concentration on demonstrating the benefits of SiC to make the most compact grid-tied inverter that is compatible with any battery system.

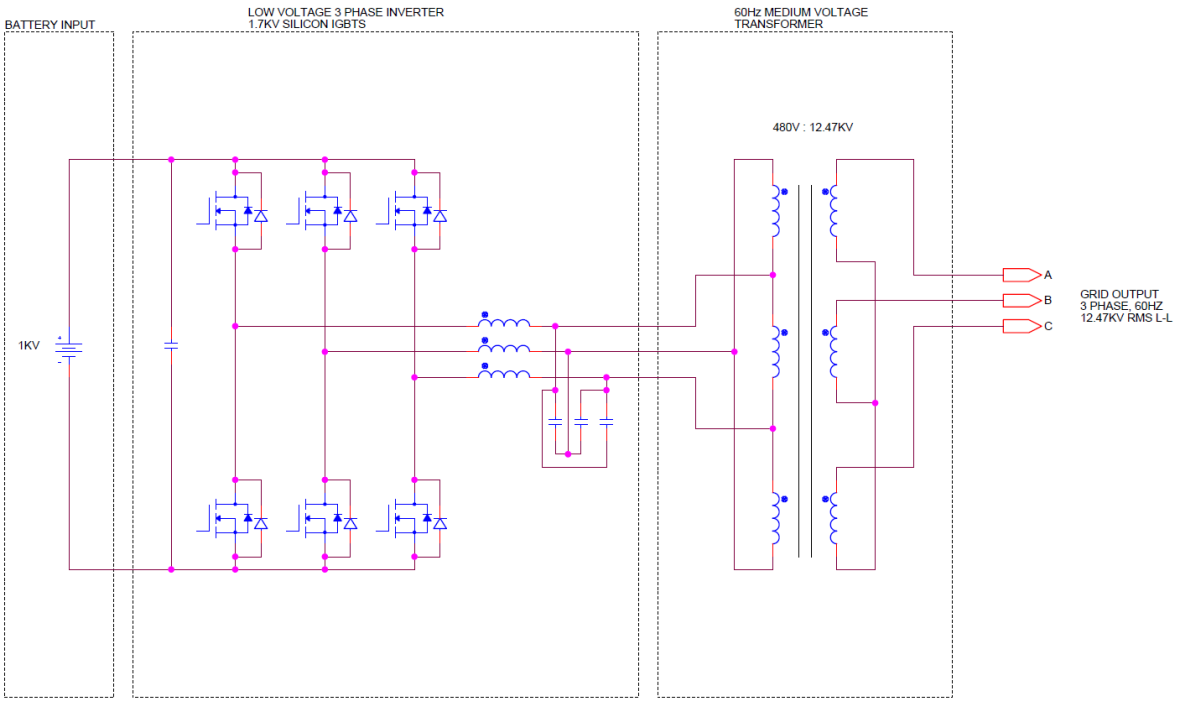



Fig. 3. Conventional two-level three-phase inverter commonly used for utility inverters

*B. Advantages of SiC MOSFETS*

Currently available semiconductor technologies have required most battery storage systems in the U.S. for utility applications in the 100 kVA to several MVA power range to use batteries with a nominal voltage near 1000 VDC even though the ultimate goal is to achieve medium voltage levels of 13 kV AC. This approach is necessary due to the limited voltage capability using 1700V Si IGBTs. This allows easy interface to a 3-phase 480 VAC electric grid and the use of commercially available ancillary components that have been tested and certified for DC applications. However, while this approach allows use of lower voltage semiconductors, use of a 60 Hz step-up transformer is still required. This incurs substantial cost and space, and the 60 Hz transformer may be on the same order of size as the battery bank itself.

Further restricting the design of existing containerized energy storage systems is the relatively low efficiency and low frequency restrictions of existing high-voltage IGBTs (Figure 4). The literature shows the clear advantage of high-voltage SiC MOSFETs over existing Si IGBTs by comparing maximum system power as a function of switching frequency for Si IGBTs and 10 kV and 15 kV SiC MOSFETs [5]. This advantage of SiC MOSFETs over Si IGBTs exists because (1) high-voltage commercial Si IGBTs are limited in blocking voltage range to about 6.5 kV, which mandates series connected devices to achieve higher grid compatible voltages; (2) IGBTs are inherently less capable of high switching frequency; and (3) SiC power MOSFETs have almost a 30x reduction in switching loss compared to the Si IGBTs. Taken as a whole, SiC MOSFETs enable greater power throughput, better efficiency, and smaller size than equivalent Si IGBTs.

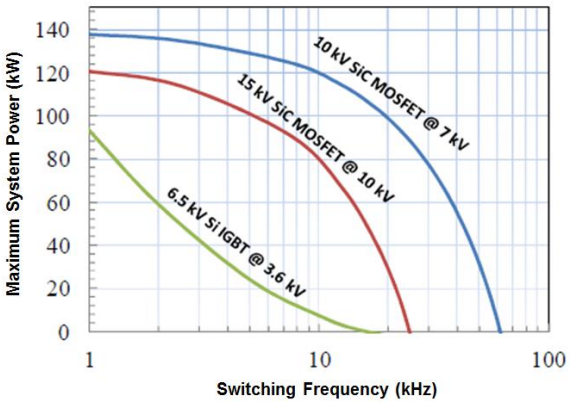



Fig. 4. Comparison of maximum system power as a function of switching frequency for Silicon IGBTs and SiC MOSFETs [5].

*C. Design Approach*

Creare's API takes advantage of the improved characteristics of SiC semiconductors to enable use of a novel transformerless topology while decreasing the total footprint of a battery energy storage system that directly connects to the 12.47 kV AC grid. A system will be designed with the goal of incorporating the inverter at power levels above 500 kW.

*D. Creare's API Architecture*

Creare's architecture relies on a Dual Active Bridge (DAB) to boost the battery voltage to a suitable DC link voltage, and a 3LNPC to create the three phase output voltage from the

DC link voltage. This architecture was chosen to take advantage of the high-voltage SiC MOSFETs currently available from a number of manufacturers.

A benefit of the 3LNPC topology is that since the 3LNPC can create three voltage levels at the grid interface (+VDC, -VDC, 0V) instead of two voltage levels, as in the standard two-level converter, this topology also creates fewer current harmonics (roughly half) for the same switching frequency [4]. This enables the use of less semiconductor area and a smaller LC filter, and resulting in better efficiency.

One of the complexities of a 3LNPC topology is that the DC link voltage must remain equally balanced around the "clamp-point." This can be achieved with switching strategies or by topology variations, as described below. To create this maximum 20 kV DC voltage, a number of options were considered. Our preferred option for converting the battery voltage (roughly 1 kV) to a larger DC link voltage (roughly 20 kV) is a two-phase DAB, as shown in Fig. 5. The bridges on the low-voltage side are wired in parallel to share current. The bridges on the high-voltage side are wired in series and operated to ensure the 20 kV DC bus remains balanced around the neutral point. The benefit of this topology is that each transformer has half the total power, so the low-voltage windings have reduced current and the high-voltage windings have reduced voltage. The two DAB pairs can generally be operated independently.

The API architecture relies upon modular subsections to achieve the DC-DC conversion and DC-AC inversion necessary. This topology has the advantage that each MOSFET only blocks half the DC link voltage and exhibits reduced current harmonics leading to smaller grid side filters. Also, this architecture lends itself well to modular testing, which enables subsystem verification and integration toward a fully functional API system.

*E. Computer Simulations and Analysis*

A computer-based simulation was developed to evaluate performance of the power electronics and controls. This provided a basis for evaluation of the voltage and current waveforms of the semiconductors to calculate losses. The simulation results also provided basis for specifying the values of the DC link capacitors and output filter components. The simulation was developed in the software tool, PSIM. The high level block diagram is shown in Fig. 6. The main components are two DAB blocks and one 3LNPC inverter block. The input is a DC voltage source, the output is a three-phase AC voltage source, and a power meter is wired to the output.

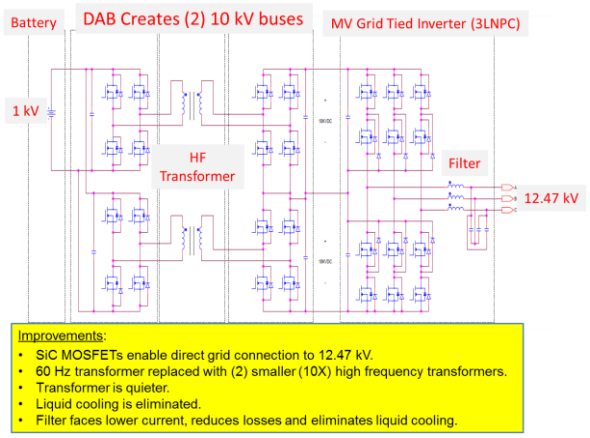



Fig. 5. Creare's API architecture based on a Dual Active Bridge Three-Level Neutral-Point-Clamp.

Fig. 7 shows the details of the DAB blocks. The main components are the MOSFET half-bridge circuits, the high-frequency transformer with winding ratio 1:15, and the 30 µF DC link capacitor on the high-voltage side. The DC link capacitor is sized to maintain reasonable ripple voltage and transient voltage during load changes. Figure 8 shows the details of the inverter block. The main components are the 3LNPC semiconductors and the grid tied output LCL filter. The output filter is designed to maintain current harmonics within the limits defined by IEEE 519/IEEE 1547.

Each DAB operates near 50% duty cycle with a 20 kHz switching frequency. This frequency is higher than possible with IGBTs, substantially reducing audible noise. Power flow from one side of the transformer to the other is controlled by phase-shifting the high and low side drive waveforms with respect to each other. Each DAB is controlled to maintain 10 kV DC across its high-side bus. This creates the balanced 20 kV DC bus required for the 3LNPC output inverter.

The three-phase 3LNPC grid inverter is controlled using conventional carrier-based techniques with the modulating signal controlled in the dq0 reference frame using Park transformations. The grid voltage is sensed to synchronize the output waveform to the grid, and the output current is controlled to create a sinusoidal waveform at the desired power factor. The 3LNPC inverter also switches at 20 kHz.

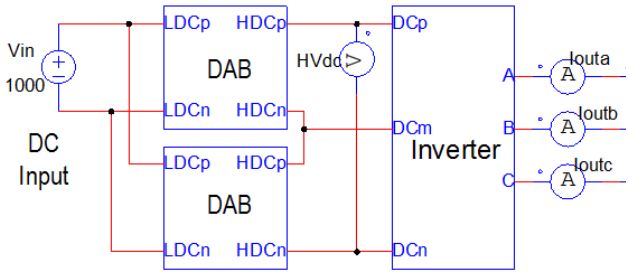



Fig. 6. Computer-based simulation model used to design and analyze the inverter.

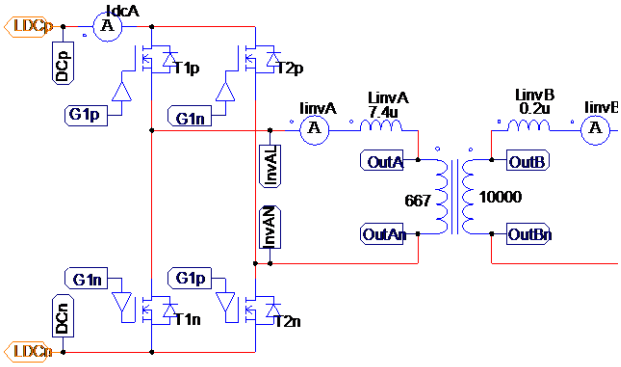



Fig. 7. Dual-Active Bridge block details.

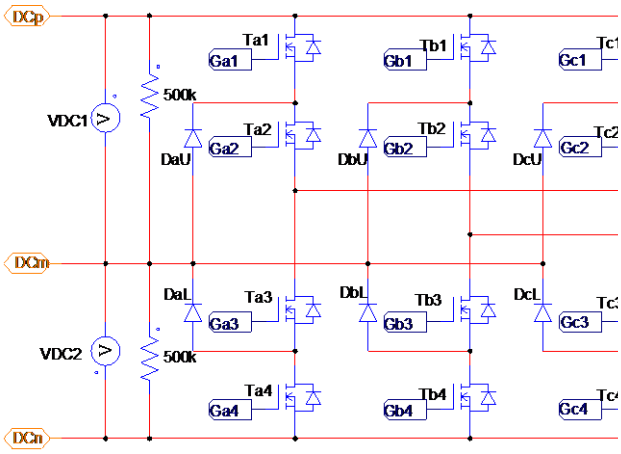



Fig. 8. Inverter block details.

Fig. 9 shows example simulation results that demonstrate system performance. The waveform labelled “HVdc” in the top panel shows that the DC link voltage only changes by 0.1% (± 200 V) with full power step changes, showing good voltage transient suppression. The red waveform labelled “OutP” in the next lower panel is the total output power of the inverter. The power increases to + 500 kW (exporting power to the grid), then decreases to - 500 kW (absorbing power from the grid), then returns to 500 kW, then drops to 0 kW. The waveforms labeled “Iouta,” “Ioutb,” and “Ioutc” show the output currents at the grid connection. They show that the grid currents rapidly respond to changes in power command and reactas expected, even with full power step transitions. The bottom panel shows the three-phase output voltage, which is 12.47 kV line-to-line. These computer simulations were validated with laboratory prototype tests. Fig. 10 shows the harmonic distortion of the output current, displayed as a percentage of the peak value. These harmonics are well below the requirements defined by IEEE 519/IEEE 1547. For example, the 5th harmonic at 300 Hz is roughly 0.7%, where the maximum allowed is 4%. The 11th harmonic at 660 Hz is roughly 0.6%, where the maximum allowed is 2%. The THD is below 1.5%, where the maximum allowed is 5%.

### *F. Efficiency Analysis*

*1) Low Voltage Section*: Fig. 11 shows an example current waveform from the PSIM simulation for one of the low-voltage MOSFETs while the system is exporting 500 kW to the grid. In this waveform, the switching frequency is 20 kHz and the RMS current in the low-voltage side MOSFETs is roughly 300 A. Analysis using these simulation results shows that two half-bridge devices are needed in parallel to operate reliably at full power (250 kW per DAB). With two MOSFETs in parallel, there is a loss of 300 W per MOSFET, for a total of 300 W * 8 * 2 = 4.8 kW, roughly 1% of the output power.

*2) High Voltage DAB:* Fig. 12 shows an example current waveform for one of the high-voltage MOSFETs while the system is exporting 500 kW to the grid. In this waveform the time scale is 0.2 ms/division and the RMS current in the high-voltage side MOSFETs is roughly 20 A. Analysis using the simulations shows that a single MOSFET can be used reliably in each location on the high-voltage side (250 kW per DAB). With this configuration, there is roughly 300 W of loss per MOSFET, for a total of 300 W * 8 = 2.4 kW. This is roughly 0.5% of the output power.

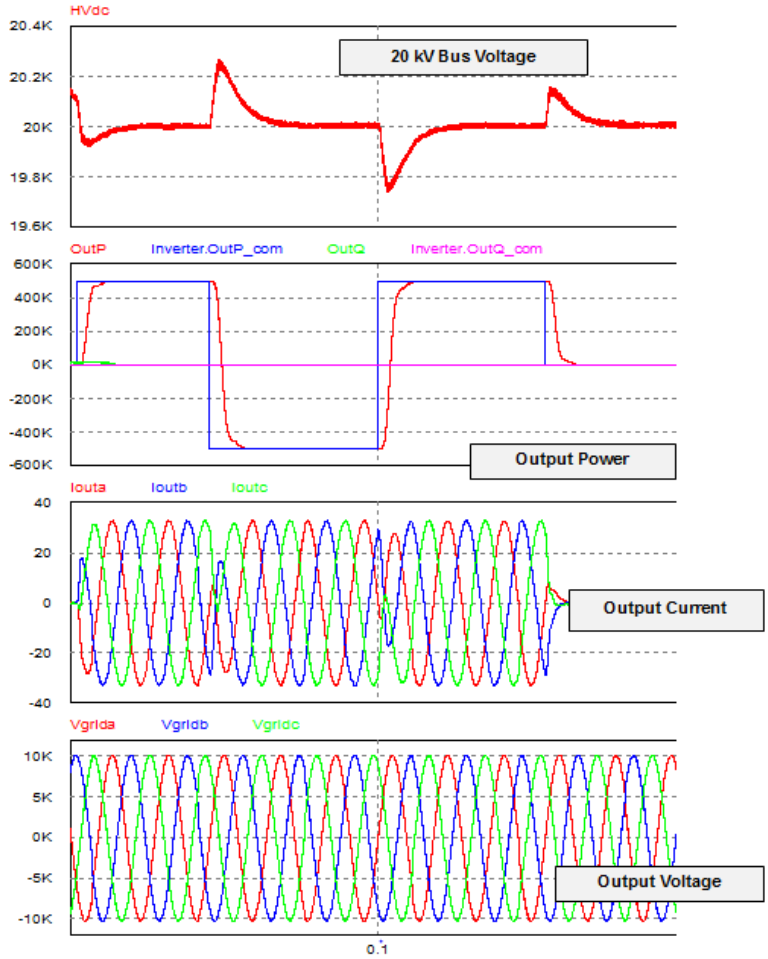



Fig. 9. Simulation results. As output power varies from +500 kW to -500 kW, the DC bus voltage, output current, and output voltage are all well behaved.

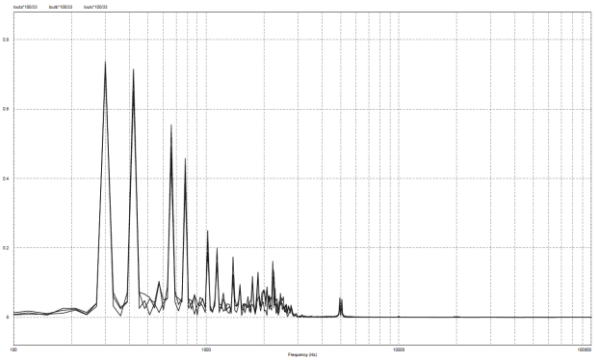


Fig. 10. Total Harmonic Distortion Simulation Results. The THD is below 1.5%, where the maximum allowed is 5%.

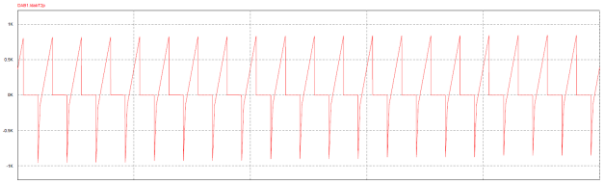


Fig. 11. Low-Voltage MOSFET Current. Total power dissipation in the low-voltage MOSFETs represents roughly 1% of the total output power.

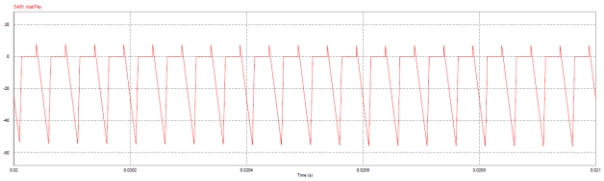


Fig. 12. High-Voltage Dual-Active Bridge MOSFET Current. Total power dissipation in the high-voltage MOSFETs represents roughly 0.5% of the total output power.

*3) 3LNPC Inverter*: Fig. 13 shows example current waveforms for the high-voltage 3LNPC MOSFETs and diodes while the system is exporting 500 kW to the grid. This waveform shows three cycles of 60 Hz current and the timescale is 10 ms/division. The red waveform shows the current in one of the clamp diodes (DaU), the blue waveform shows the current in one of the outer transistors (Ta1), and the green waveform shows the current in one of the inner transistors (Ta2). Fig. 14 shows the results for a longer duration where the power flow varies in both direction and power factor. Note the distribution of current among these devices varies strongly with power factor. The image shows the same waveforms while the power output varies from +

500 kW (exporting) to - 500 kW (absorbing) to + 500 kVAR to - 500 kVAR. In

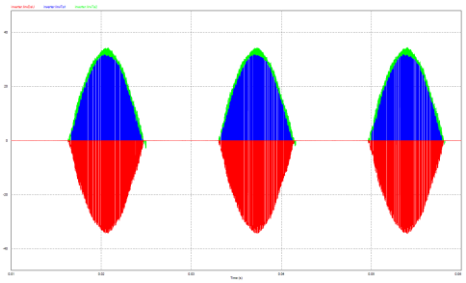


Fig. 13. High-Voltage MOSFET Current. The red waveform shows the current in one of the clamp diodes (DaU), the blue waveform shows the current in one of the outer transistors (Ta1), and the green waveform shows the current in one of the inner transistors (Ta2).

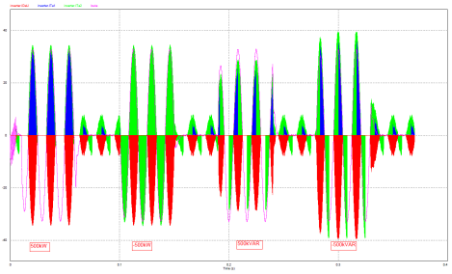


Fig. 14. High-Voltage MOSFET Current. Plot shows the effect of power flow direction and power factor on current split between the clamp diodes and transistors.

this waveform, the pink trace is the grid output current. Depending on power factor, the RMS current in the worst case high-voltage side MOSFET is 15 A. Analysis using the simulations shows that a single MOSFET can be used reliably in each location of the 3LNPC topology. With this configuration, there is roughly 300 W maximum loss in each MOSFET, with a total loss of roughly 3.6 kW. This is roughly 0.7% of the output power.

*4) Overall Efficiency*: Using the computer simulations, we examined efficiency and losses at a typical output power condition of 500 kW. Semiconductor losses total 10.2 kW, or 2% of total output power. Transformer losses are estimated to be 1% and filter losses are estimated to be 1%. Thus, overall efficiency is estimated to be roughly 96%. This is a significant achievement and enables elimination of the liquid cooling system. Table II summarizes the losses and efficiency.

TABLE II
POWER LOSS AND EFFICIENCY SUMMARY. THE SUMMARY IS BASED ON 500 KW OUTPUT POWER.

| Component | Loss |
|---|---|
| Low-Voltage DAB | 4.8 kW (1%) |
| High-Voltage DAB | 2.4 kW (0.5%) |
| 3LNPC | 3.6 kW (0.7%) |
| Transformer | 5 kW (1%) |
| Filters | 5 kW (1%) |
| TOTAL LOSS | 21 kW |
| Output Power | 500 kW |
| Efficiency | 96% |

## IV. PERFORMANCE EXPERIMENTS

### *A. Low Voltage Architecture Testing*

Subsystem hardware testing, to date, includes the DAB modules, and to evaluate the DC-DC conversion performance, these modules were tested in the benchtop test facility shown in Fig. 15. Fig. 16 shows input and output waveforms during testing for a DAB module. During this test effort, we successfully demonstrated the DAB at frequencies up to 20 kHz at subscale voltages.

### *B. DAB/3LNPC Controller Testing*

A combined DAB/3LNPC controller was also successfully tested using a surrogate 6 kHz silicon IGBT prototype while the SiC hardware is being developed. The following figures illustrate laboratory test results intended to validate the previously described computer simulations. Fig. 17 shows a block diagram of the controller, and Fig. 18 shows a photograph of the test facility. The controller was developed to enable configuration as a 20 kHz controller for testing with SiC components, once completed. The implemented control firmware functionality currently includes control for all modules in the API architecture and includes features to operate in a standalone (UF) mode or a grid-tied (PQ) mode. Both hardware and software were successfully demonstrated in UF and PQ modes, and Fig. 19 shows the results for the PQ grid-tied mode at 10 kW.

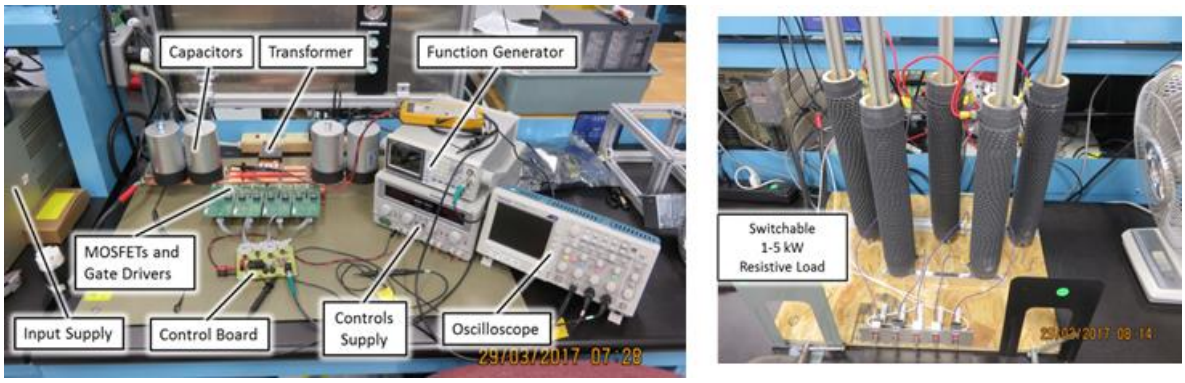



Fig. 15. Low Voltage section of the DAB.

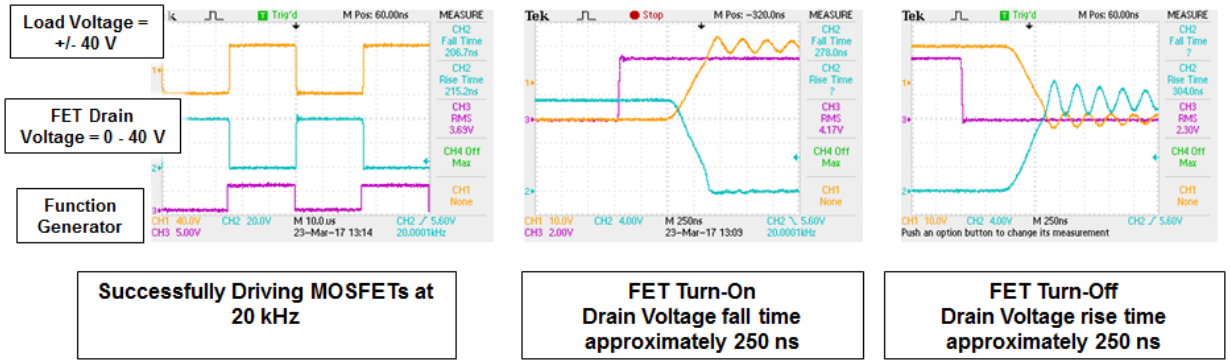



Fig. 16. Low Voltage section test results.

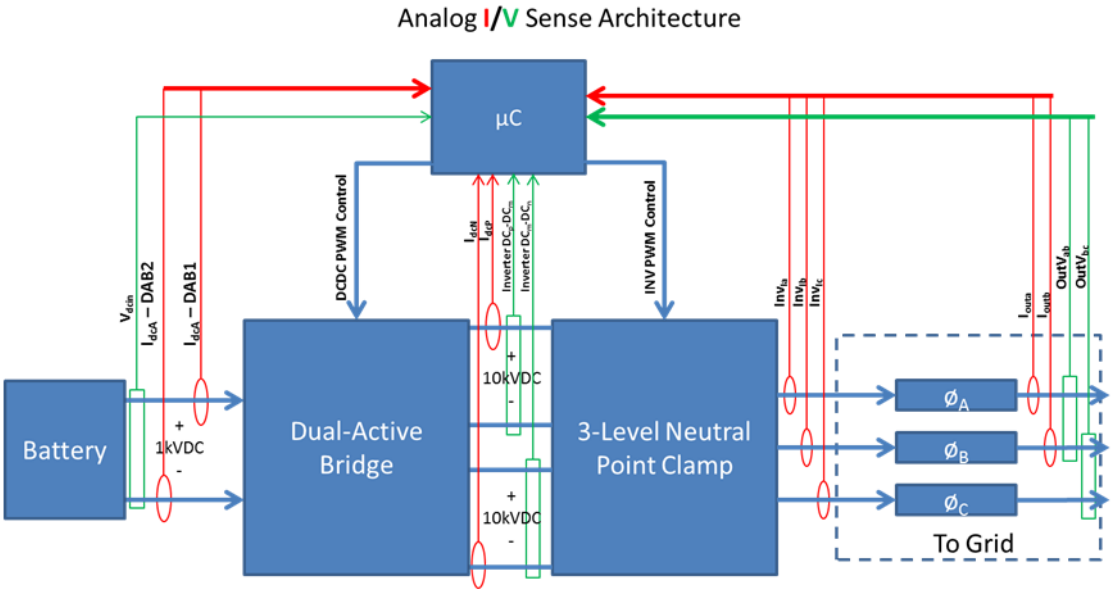



Fig. 17. Controller architecture.

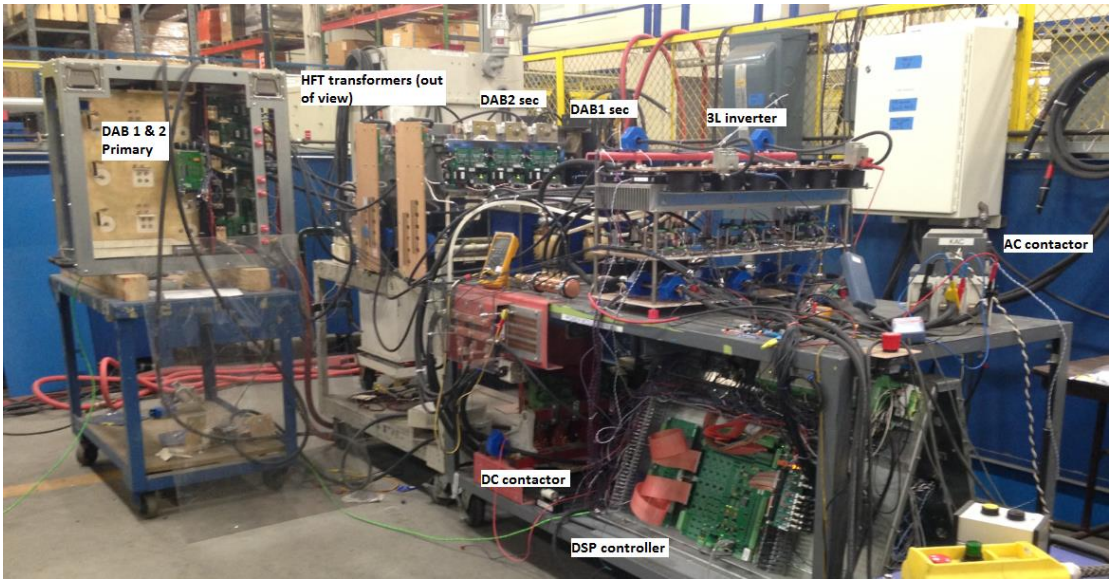



Fig. 18. Photograph of the controller, DAB, and 3LNPC hardware.

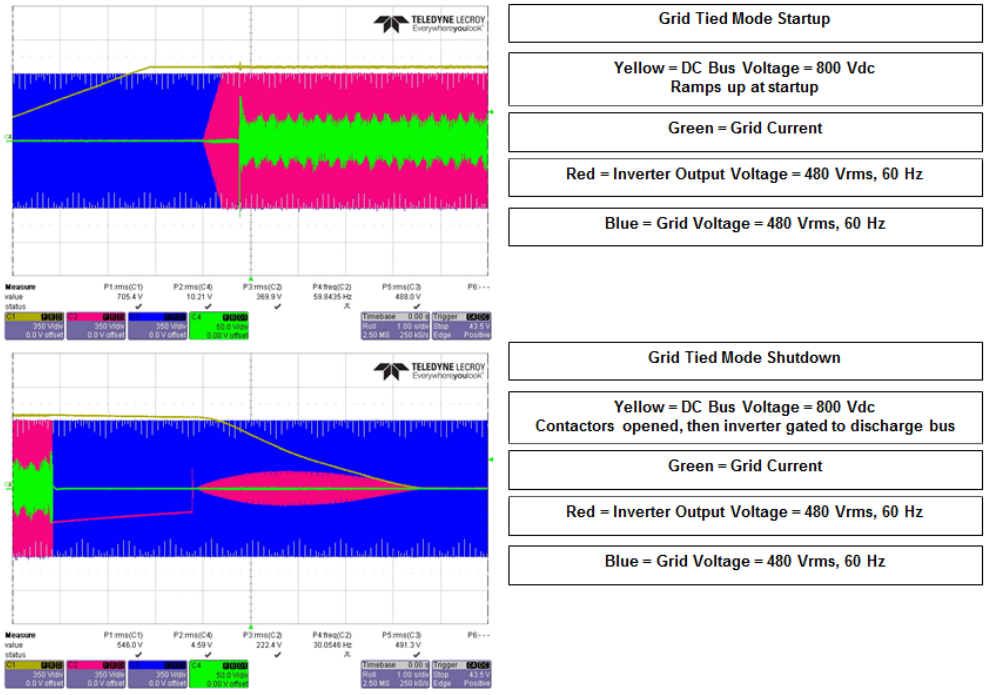
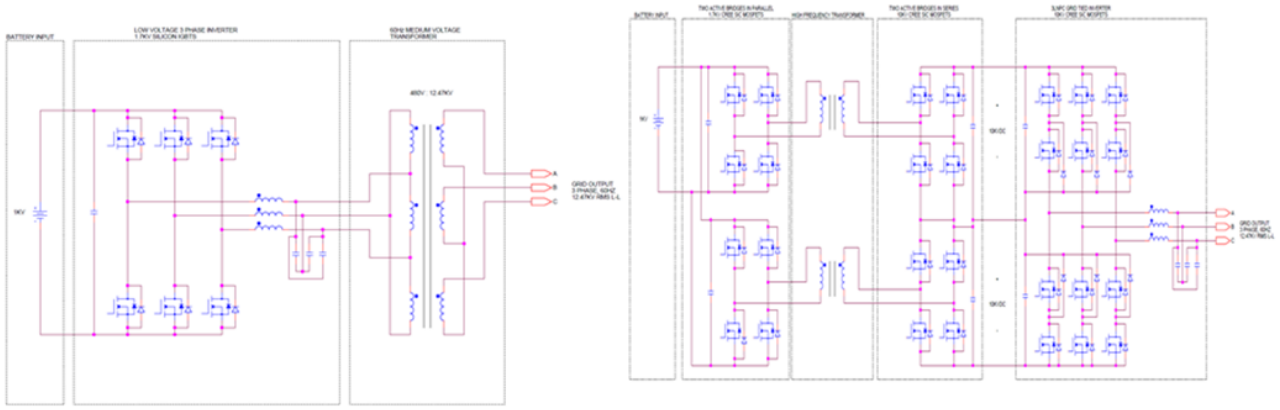



Fig. 19. PQ Grid-Tied mode test results.

## V. Discussion

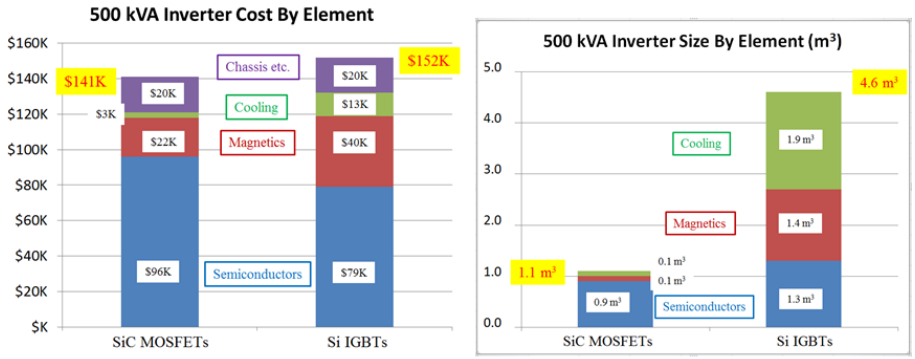
Fig. 20 compares a conventional inverter with Creare's DAB 3LNPC inverter. Benefits of Creare's API include elimination of the 60 Hz transformer and liquid cooling, increased power density, and reduced audible noise. Fig. 21 illustrates the cost and power density comparison between SiC MOSFETs and Si IGBTs. Overall, we expect the cost to be about the same, and the power density to be improved by at least two times when compared with the silicon inverter.



Limitations of this design:
- Requires 480 : 12.47 kV transformer for grid connect.
- Silicon MOSFETs or IGBTs require liquid cooling (~ 50 °C).
- Filter is large and also requires liquid cooling.
- 60 Hz transformer emits acoustic noise.

Improvements:
- SiC MOSFETs enable direct grid connection to 12.47 kV.
- 60 Hz transformer replaced with (2) smaller (10X) high frequency transformers.
- Transformer is quieter.
- Liquid cooling is eliminated.
- Filter faces lower current, reduces losses and eliminates liquid cooling.

Fig. 20. Comparison of conventional inverter with Creare's DAB 3LNPC Inverter.




Per unit material costs are comparable ($141K vs. $152K). New design: SiC costs are higher, but magnetics and cooling costs are lower. **SiC costs are likely to reduce.**

Size of the inverter which uses SiC MOSFETs is much smaller, with 4.3X power density.

Fig. 21. Cost and power density comparison.

## VI. Conclusions

Our work, thus far, has successfully proven the feasibility of deploying this high-performance inverter. Specifically:

- SiC MOSFETs are superior to silicon IGBTs because (1) high-voltage commercial silicon IGBTs are limited in blocking voltage; (2) IGBTs are limited to lower switching frequency; and (3) SiC power MOSFETs have lower loss.
- SiC MOSFETs will eliminate the need for a liquid-cooled system and 60 Hz transformer. Overall power density is expected to be at least two times greater with SiC MOSFETs than for silicon IGBTs.
- SiC MOSFETs are available to accomplish these goals. Testing of low and high voltage SiC MOSFETs has demonstrated adequate switching times to enable use of a high-frequency transformer.

## VII. Recommendation

Based on these positive feasibility demonstrations, Creare plans to continue to develop this API technology. Key future accomplishments are expected to include: (1) fabrication of a fully functional prototype based on this design; (2) initial laboratory testing to verify design expectations; and (3) application of the prototype for initial energy storage applications.

## VIII. Future Work

The project began in 2015 as a Phase I SBIR project. Thus far, the year long Phase I project and the first of 2 years of the Phase II project have been completed. The project is roughly two-thirds complete. During the next year of the program, we plan to fabricate and test the fully functional API prototype. We will review and refine the control firmware used during prior testing and acquire critical system components such as the high-voltage SiC devices. We will fabricate subsystem sections individually, then integrate them to form the entire system. Final versions of the high-frequency transformer and inductor will be fabricated. Controller testing will be completed, and the controller will be integrated with the hardware for testing.

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