All-SiC Phase Leg Power Modules with MIDSJT Devices

Ranbir Singh, Siddarth Sundaresan and Stan Atcitty*
GeneSiC Semiconductor Inc.
*Sandia National Laboratories
ranbir.singh@genesicsemi.com +1 703 996 8200
43670 Trade Center Pl #155; Dulles VA 20166

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Phase Leg forms fundamental building block for AC/DC AND DC/AC Conversion

Each switch and diode must be capable of bus voltage
Novel Single-chip Monolithic Integrated Diode Super Junction Transistor (MIDSJT)

- If achieved it will be the first time a high voltage integrated circuit is demonstrated
- Universal applicability towards all grid-connected power electronics
Many Energy storage opportunities require power electronics that can be made efficient

Silicon Carbide high voltage devices will play a pivotal role
Goals for this Project: Phase Leg using Single Chip MIDSJT

Phase I (6/14-12/14)
• Demonstrate Integrated SJT/Diode chip at 600 V

Phase II (1/15-12/15)
• Develop SPICE Models for Integrated Device
• Quantify benefits of Integrated MIDSJT vs discrete

Phase III (1/16-12/16)
• 1200 V Integrated SJT/Diodes
• >20 A
• Optimized Packaging
### Why SiC Power Devices at Medium Voltages?

<table>
<thead>
<tr>
<th>Properties SiC vs Si</th>
<th>Performance of SiC Devices</th>
<th>Impact on Power Circuits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown Field ((10X))</td>
<td>Lower On-state Voltage drop ((2-3X))</td>
<td>Higher Efficiency of circuits</td>
</tr>
<tr>
<td>Smaller Epitaxial Layers ((10-20X))</td>
<td>Faster Switching speeds ((100-1000X))</td>
<td>Compact circuits</td>
</tr>
<tr>
<td>Higher Thermal Conductivity ((3.3-4.5 \text{ W/cmK vs } 1.5 \text{ W/cmK}))</td>
<td>Higher Chip Temperatures ((250-300^\circ\text{C instead of } 125^\circ\text{C}))</td>
<td>Higher pulsed power Higher continuous current densities,</td>
</tr>
<tr>
<td>Melting Point ((2X))</td>
<td>High Temperature Operation ((3X))</td>
<td>Simple Heat Sink</td>
</tr>
<tr>
<td>Bandgap ((3X)) ((10^{16}X \text{ smaller } n_i))</td>
<td>High Intrinsic Adiabatic Pulsed Current Level ((3-10X))</td>
<td>Higher Current Capability</td>
</tr>
</tbody>
</table>
## SiC Switch Comparisons

<table>
<thead>
<tr>
<th></th>
<th>MOSFET</th>
<th>JFET-ON</th>
<th>JFET-OFF</th>
<th>BJT</th>
<th>SJT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gate Control</strong></td>
<td>+20V/0V No Current</td>
<td>+0V/-20V Low Current</td>
<td>+3/0V Current Gain</td>
<td>+3V/0V Current Gain</td>
<td>+3V/0V Current Gain</td>
</tr>
<tr>
<td><strong>Current Gain</strong></td>
<td>Infinite</td>
<td>&gt;1000</td>
<td>~50 (at rated current)</td>
<td>~30 (at rated current)</td>
<td>&gt;100 (Target at rated current)</td>
</tr>
<tr>
<td><strong>Current Rating</strong></td>
<td>Very low</td>
<td>High</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td><strong>Fabrication Cost</strong></td>
<td>Very High</td>
<td>Medium</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Switching Speed</strong></td>
<td>Medium (Gate Cap)</td>
<td>High</td>
<td>Low/Medium (Gate-Source Cap)</td>
<td>Very low (Minority injection)</td>
<td>High (Low cap, No Minority)</td>
</tr>
<tr>
<td><strong>High Temperature</strong></td>
<td>Very Poor</td>
<td>Very Good</td>
<td>Medium</td>
<td>Very Good</td>
<td>Very Good</td>
</tr>
</tbody>
</table>
1200 V/20 mOhm SiC Junction Transistor (SJT) – Output Characteristics

- $R_{on,sp} = 2.3 \text{ m} \Omega \cdot \text{cm}^2$
- $V_{CE,sat} = 1.1 \text{ V (50 A)}$

- $R_{on,sp} = 4.5 \text{ m} \Omega \cdot \text{cm}^2$
- $V_{CE,sat} = 2.0 \text{ V (50 A)}$
SJT Switching at 1200 V and 175°C

Turn-On Transient

Turn-Off Transient

\[ t_{fv} = 45 \text{ ns} \]

\[ t_{fr} = 25 \text{ ns} \]
GeneSiC SJT has Highest Efficiency

Source: Virginia Tech
# 1200 V (60-80 mΩ) SiC Transistors

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SiC SJT</th>
<th>SiC MOSFET#1</th>
<th>SiC MOSFET#2</th>
<th>SiC JFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{on}$ (25° C)(mΩ-cm²)</td>
<td>2.2</td>
<td>8*</td>
<td>7*</td>
<td>3.2</td>
</tr>
<tr>
<td>$R_{on}$ (175° C)(mΩ-cm²)</td>
<td>3.8</td>
<td>16.6*</td>
<td>16.2*</td>
<td>8</td>
</tr>
<tr>
<td>$V_{ds, on}$ (25° C, 20 A)(V)</td>
<td>1.2</td>
<td>1.8</td>
<td>1.75</td>
<td>1.3</td>
</tr>
<tr>
<td>$V_{ds, on}$ (175° C, 20 A)(V)</td>
<td>2.2</td>
<td>3.7</td>
<td>3.5</td>
<td>4.0</td>
</tr>
<tr>
<td>$C_{iss}$ @ $V_d=1$ V (pF)</td>
<td>3160</td>
<td>1500</td>
<td>3000</td>
<td>1000</td>
</tr>
<tr>
<td>$C_{oss}$ @ $V_d=1$ V (pF)</td>
<td>800</td>
<td>1500</td>
<td>1500</td>
<td>380</td>
</tr>
<tr>
<td>$C_{rss}$ @ $V_d=1$ V (pF)</td>
<td>800</td>
<td>650</td>
<td>1200</td>
<td>380</td>
</tr>
<tr>
<td>$R_{th}$ (° C/W)</td>
<td>1.16</td>
<td>0.60</td>
<td>0.52</td>
<td>1.1</td>
</tr>
<tr>
<td>$t_{F,V}$ (ns)-Ind. Load</td>
<td>25</td>
<td>20</td>
<td>22</td>
<td>26</td>
</tr>
<tr>
<td>$t_{R,V}$ (ns)-Ind. Load</td>
<td>19</td>
<td>15</td>
<td>36</td>
<td>33</td>
</tr>
<tr>
<td>$E_{on}$ (µJ)-Ind. Load</td>
<td>175</td>
<td>170</td>
<td>174</td>
<td>180</td>
</tr>
<tr>
<td>$E_{off}$ (µJ)-Ind. Load</td>
<td>38</td>
<td>35</td>
<td>40</td>
<td>185</td>
</tr>
</tbody>
</table>

* The low transconductance in SiC MOSFETs causes the transition from triode (ohmic) to the saturation (constant current region to be spread over a wide range of drain current. The $R_{on}$ of these parts increases from 92 mΩ at 20 A to > 100 mΩ at the rated 32 A.
### 1200 V/60-80 mΩ SiC Transistors – Switching Figures of Merit

<table>
<thead>
<tr>
<th>Category</th>
<th>FOM</th>
<th>$T_J$</th>
<th>SiC SJT</th>
<th>SiC MOSFET#1</th>
<th>SiC MOSFET#2</th>
<th>SiC JFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft Switching (ZVS) [1]</td>
<td>$\frac{I}{R_{on,sp}C_{oss,sp}}$</td>
<td>150° C</td>
<td>11.4</td>
<td>4.2</td>
<td>5.6</td>
<td>10.5</td>
</tr>
<tr>
<td>Hard Switching</td>
<td>$\frac{T_J - T_C - R_{on}I_C^2D}{R_{th} E_{on} + E_{off}}$</td>
<td>150° C</td>
<td>592</td>
<td>601</td>
<td>567</td>
<td>380</td>
</tr>
</tbody>
</table>

- In ZVS, the power transistor is turned on with zero voltage across it. Therefore, ZVS is insensitive to the Miller (cross-over) power losses, and only depends on $Q_{OSS}$, since the output capacitance needs to be fully discharged before the start of the next switching cycle.
Short Circuit Ruggedness

- Simultaneous application of operating voltage and full, rated current
- >10 µsec short circuit testing successful
SPICE Models Developed and Published

* MODEL OF GeneSiC Semiconductor Inc.
* $Revision: 1.0 $
* $Date: 29-MAY-2015 $
* GeneSiC Semiconductor Inc.
* 43670 Trade Center Place Ste. 155
* Dulles, VA 20166
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* ALL RIGHTS RESERVED
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
* Start of GA10SICP12-247 SPICE Model
.SUBCKT GA10SICP12 DRAIN GATE SOURCE
Q1 DRAIN GATE SOURCE GA10SICP12_Q
D1 SOURCE DRAIN GA10SICP12_D1
D2 SOURCE DRAIN GA10SICP12_D2
*
.model GA10SICP12_Q NPN
+ IS  9.833E-48 ISE  1.073E-26 EG   3.23
+ BF  113 BR    0.55 IKF 5000
+ NF  1 NE    2 RB   4.67
+ RE  0.005 RC   0.083 CJC 427E-12
+ VJC 3.1004 MJC 0.4752 CJJE 1373E-12
+ VJE 10.644 MJJE 0.21376 XTI  3
+ XTB -1.35 TRC1 7.0E-03 MFG GeneSiC_Semi
+ IRB 0.001 RMB  0.16
.model GA10SICP12_D1 D
+ IS  4.556E-15 RS   0.0736 N   1
+ IKF 1000 EG   1.2 XTI -2
+ TRS1 0.0054347826 TRS2 2.71739E-05 CJO 6.40E-10
+ VJ  0.469 M    1.508 FC  0.5
+ TT  1.00E-10 BV  1200 IBV 1.00E-03
+ VPK 1200 IAVE 10
.model GA10SICP12_D2 D
+ IS  1.54E-22 RS  0.19  TRS1 -0.004
+ N   3.941 EG  3.23 IKF  19
+ XTI 0 FC   0.5 TT 0
+ BV  1200 IBV 1.00E-03 VPK 1200
.ENDS
* End of GA10SICP12-247 SPICE Model
GeneSiC’s commercial Phase Leg Packaging
Module Configuration

- Gate Return Terminal (Anode Potential)
- Gate Terminal
- Plastic Case (PPS Ryton R-4)
- Baseplate
- Anode Power Terminal (Top of Chip)
- SiC Chip on DBC AlN
- Cathode Power Terminals (Bottom of Chip)
Status and Future Efforts

• **Current Status**
  - SPICE Models for 1200 V and 600 V SiC MIDSJT Developed
  - Demonstration of 600 V MIDSJT Completed
  - Conduction and Switching losses calculated using analytical models
  - Commercial Release of DISCRETE SJT+Diodes Completed

• **Future Efforts in Phase II**
  - Undergoing H-Bridge Circuit Level simulation for Dual-Active Bridge in Energy Storage relevant 400 kW System
  - Circuit Efficiencies to be compared between Monolithically Integrated SJT-Diodes with DISCRETE SJT+Diodes
Grant Details

- Principal Investigator: Dr. Siddarth Sundaresan
- Program Manager: Dr. Ranbir Singh
- Grantee:
  GeneSiC Semiconductor Inc.
  43670 Trade Center Place
  Suite 155
  Dulles VA 20166
  +1 703 996 8200 (ph)
  ranbir.singh@genesicsemi.com