



All-SiC Phase Leg Power Modules with MIDSJT Devices

Ranbir Singh, Siddarth Sundaresan and
Stan Atcitty*

GeneSiC Semiconductor Inc.

*Sandia National Laboratories

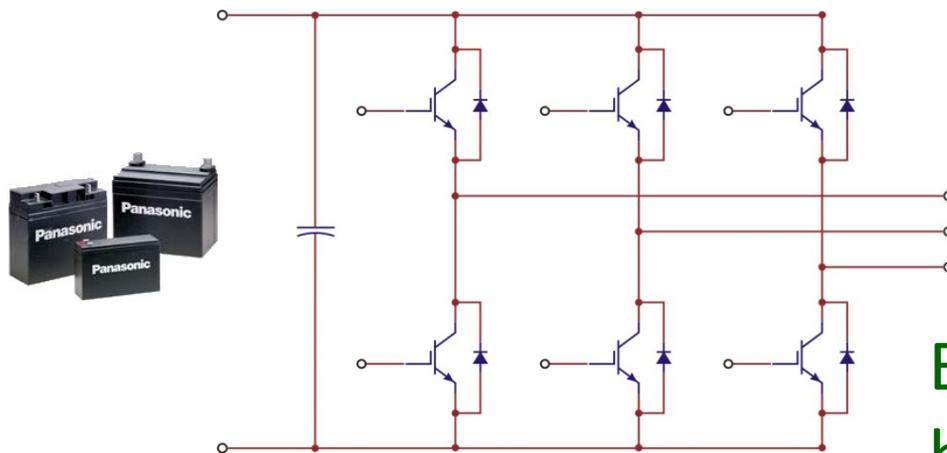
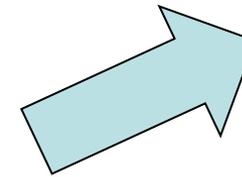
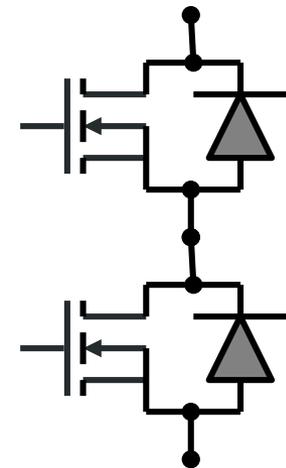
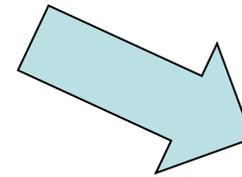
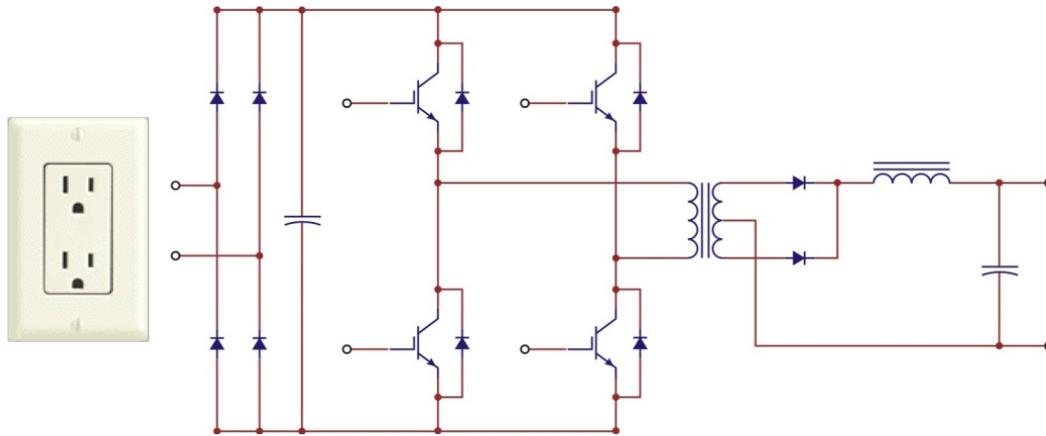
ranbir.singh@genesicsemi.com +1 703 996 8200

43670 Trade Center Pl #155; Dulles VA 20166

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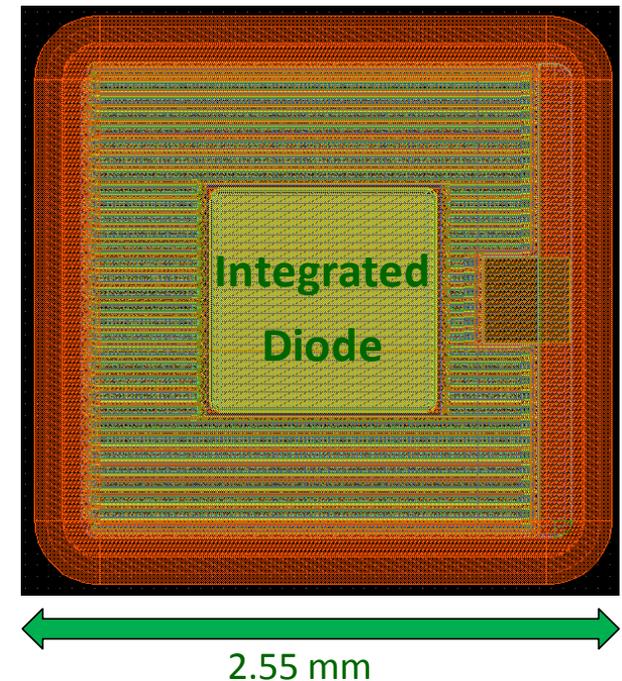
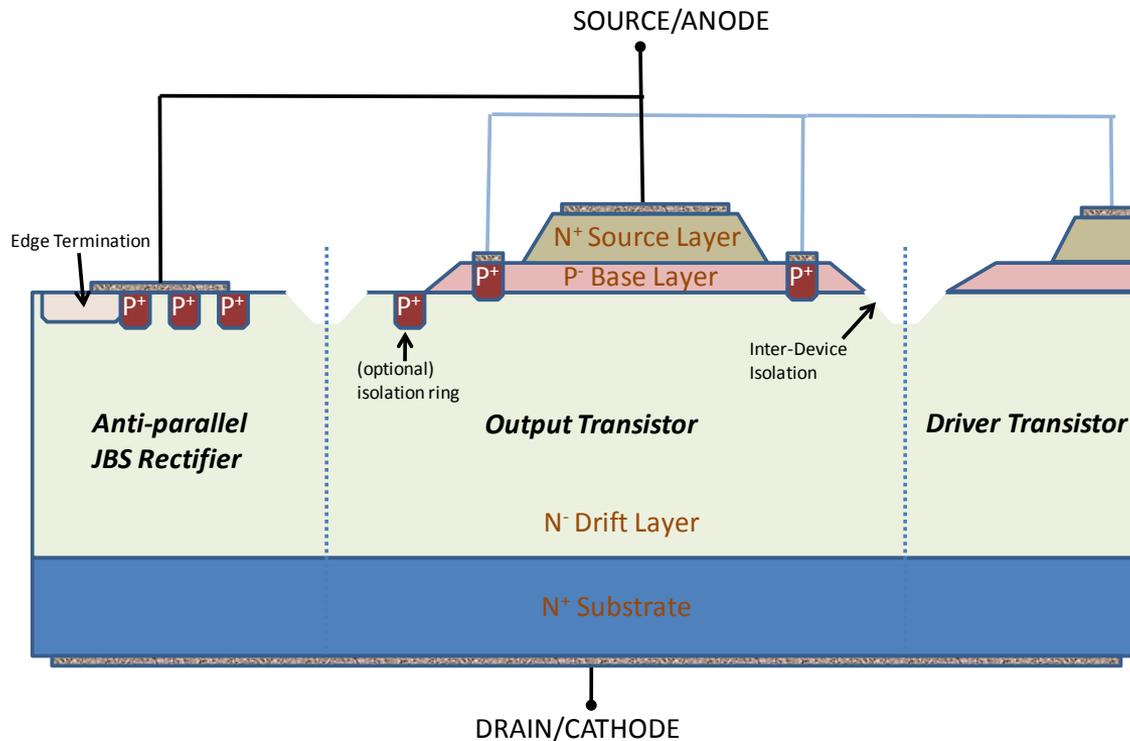
GeneSiC
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Phase Leg forms fundamental building block for AC/DC AND DC/AC Conversion



Each switch and diode must be capable of bus voltage

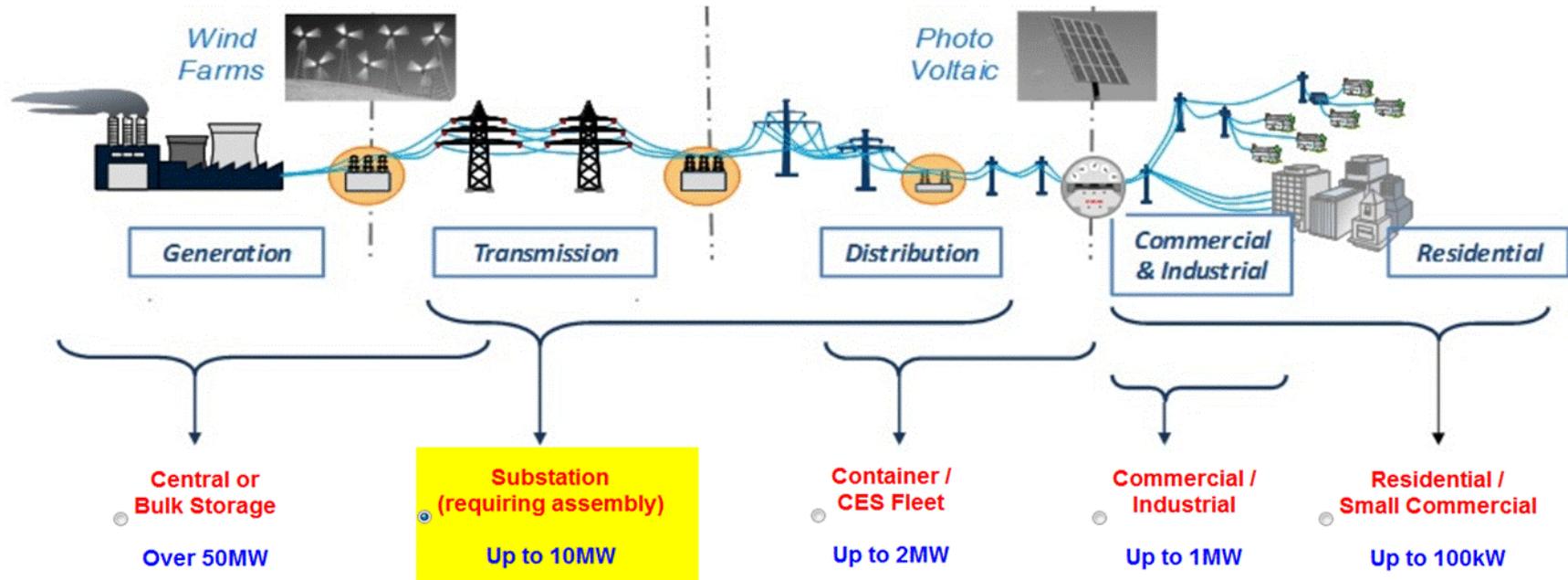
Novel Single-chip Monolithic Integrated Diode Super Junction Transistor (MIDSJT)



- If achieved it will be the first time a high voltage integrated circuit is demonstrated
- Universal applicability towards all grid-connected power electronics

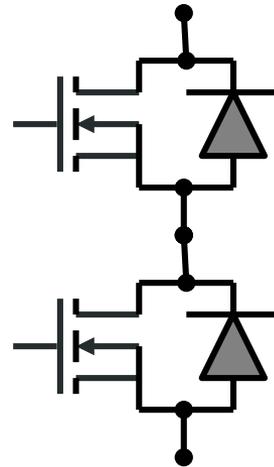
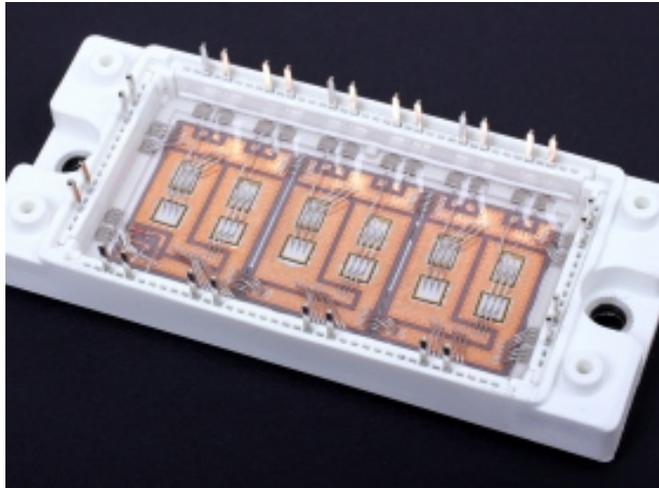
Energy Storage Opportunities

Possible Locations for Grid-Connected Energy Storage



- Many Energy storage opportunities require power electronics that can be made efficient
- Silicon Carbide high voltage devices will play a pivotal role

Goals for this Project: Phase Leg using Single Chip MIDSJT



Phase I (6/14-12/14)

- Demonstrate Integrated SJT/Diode chip at 600 V

Phase II (1/15-12/15)

- Develop SPICE Models for Integrated Device
- Quantify benefits of Integrated MIDSJT vs discrete

Phase III (1/16-12/16)

- 1200 V Integrated SJT/Diodes
- >20 A
- Optimized Packaging

Why SiC Power Devices at Medium Voltages?

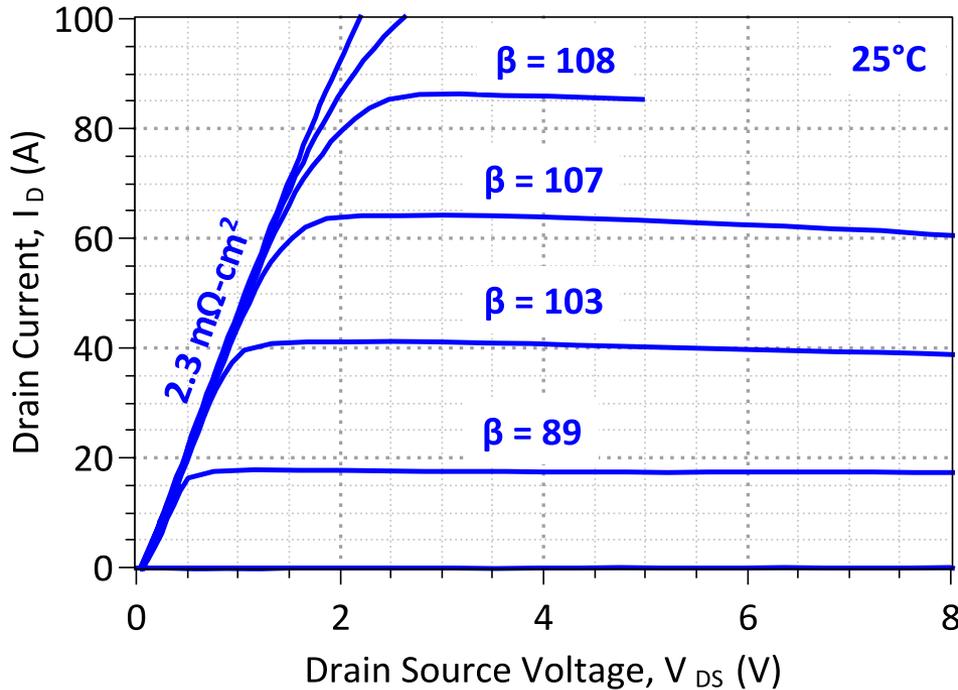
Properties SiC vs Si	Performance of SiC Devices	Impact on Power Circuits
Breakdown Field (10X)	Lower On-state Voltage drop (2-3X)	Higher Efficiency of circuits
Smaller Epitaxial Layers (10-20X)	Faster Switching speeds (100-1000X)	Compact circuits
Higher Thermal Conductivity (3.3-4.5 W/cmK vs 1.5 W/cmK)	Higher Chip Temperatures (250-300°C instead of 125°C)	Higher pulsed power Higher continuous current densities,
Melting Point (2X)	High Temperature Operation (3X)	Simple Heat Sink
Bandgap (3X) (10¹⁶X smaller n_i)	High Intrinsic Adiabatic Pulsed Current Level (3-10X?)	Higher Current Capability

SiC Switch Comparisons

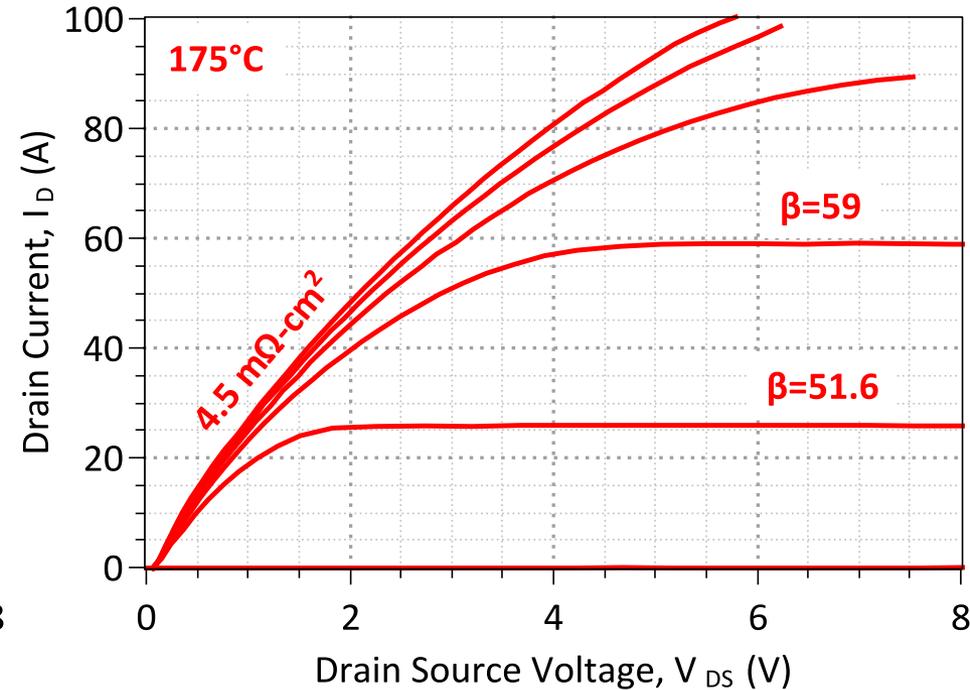
	MOSFET	JFET-ON	JFET-OFF	BJT	SJT
Gate Control	+20V/0V No Current	+0V/-20V Low Current	+3/0V Current Gain	+3V/0V Current Gain	+3V/0V Current Gain
Current Gain	Infinite	>1000	~50 (at rated current)	~30 (at rated current)	>100 (Target at rated current)
Current Rating	Very low	High	Low	High	High
Fabrication Cost	Very High	Medium	High	Low	Low
Switching Speed	Medium (Gate Cap)	High	Low/Medium (Gate-Source Cap)	Very low (Minority injection)	High (Low cap, No Minority)
High Temperature	Very Poor	Very Good	Medium	Very Good	Very Good

1200 V/20 mOhm SiC Junction Transistor (SJT) – Output Characteristics

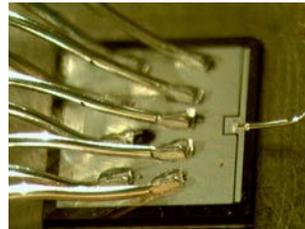
GA50JT12-247



GA50JT12-247



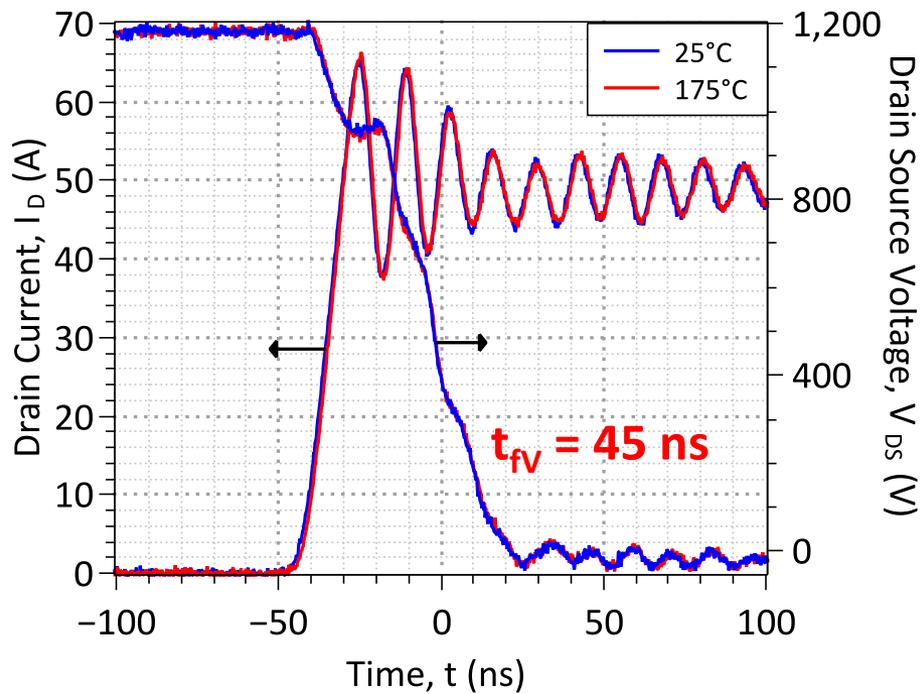
- $R_{on,sp} = 2.3 \text{ m}\Omega\text{-cm}^2$
- $V_{CE,sat} = 1.1 \text{ V (50 A)}$



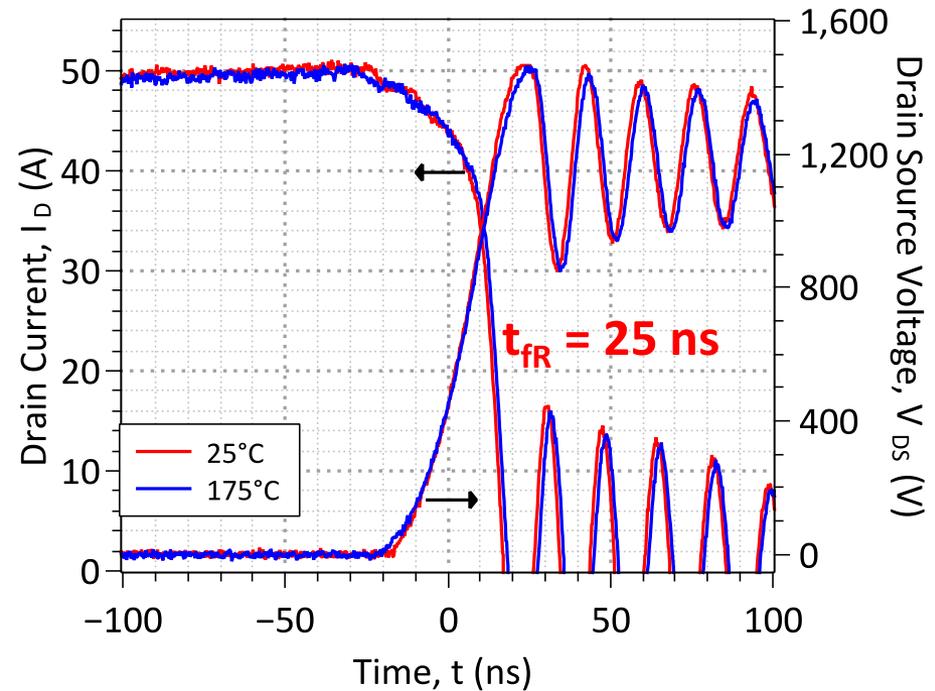
- $R_{on,sp} = 4.5 \text{ m}\Omega\text{-cm}^2$
- $V_{CE,sat} = 2.0 \text{ V (50 A)}$

SJT Switching at 1200 V and 175°C

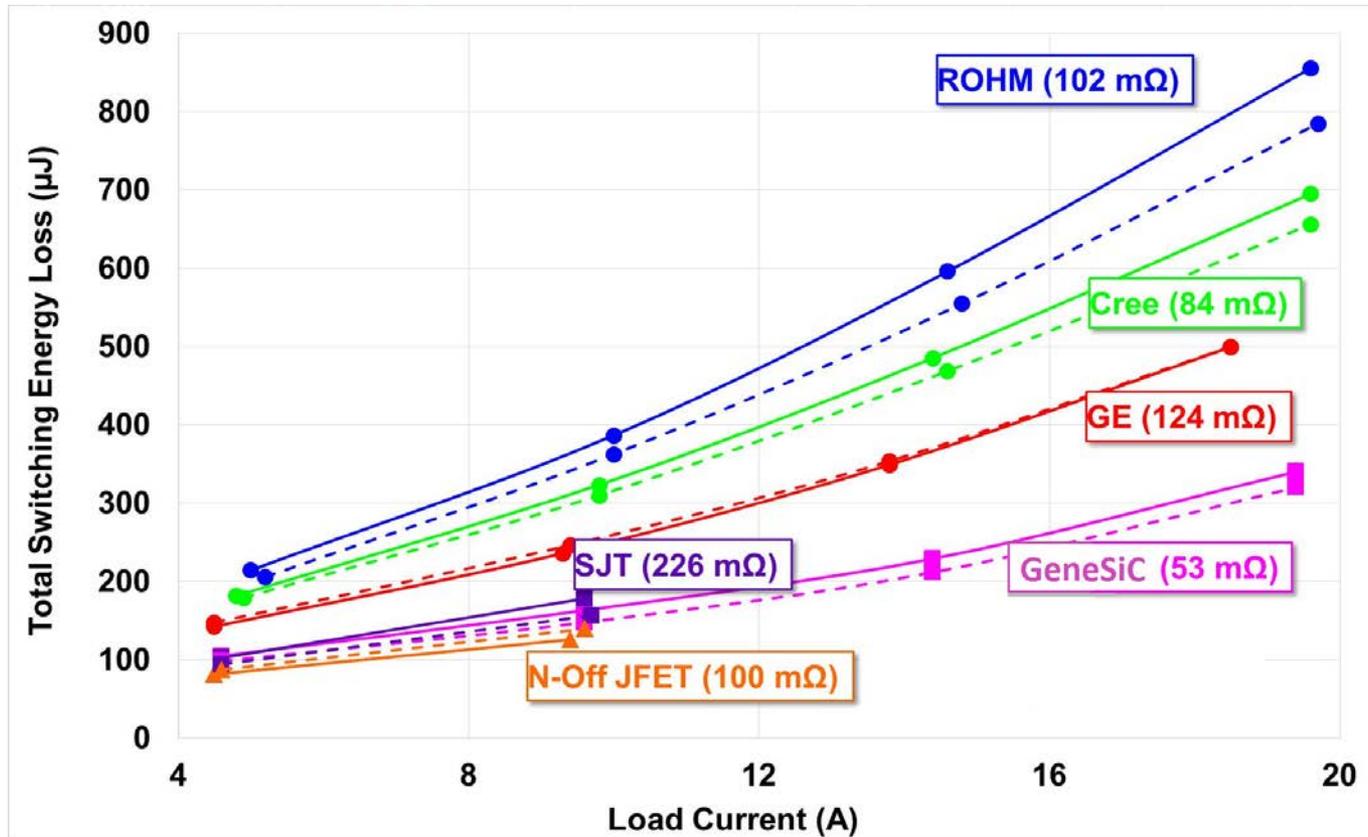
Turn-On Transient



Turn-Off Transient



GeneSiC SJT has Highest Efficiency



Source: Virginia Tech

1200 V (60-80 mΩ) SiC Transistors

Parameter	SiC SJT	SiC MOSFET#1	SiC MOSFET#2	SiC JFET
R_{on} (25° C)(mΩ-cm ²)	2.2	8*	7*	3.2
R_{on} (175° C)(mΩ-cm ²)	3.8	16.6*	16.2*	8
$V_{ds,on}$ (25° C, 20 A)(V)	1.2	1.8	1.75	1.3
$V_{ds,on}$ (175° C, 20 A)(V)	2.2	3.7	3.5	4.0
C_{iss} @ $V_d=1$ V (pF)	3160	1500	3000	1000
C_{oss} @ $V_d=1$ V (pF)	800	1500	1500	380
C_{riss} @ $V_d=1$ V (pF)	800	650	1200	380
R_{th} (° C/W)	1.16	0.60	0.52	1.1
$t_{F,V}$ (ns)-Ind. Load	25	20	22	26
$t_{R,V}$ (ns)-Ind. Load	19	15	36	33
E_{on} (μJ)-Ind. Load	175	170	174	180
E_{off} (μJ)-Ind. Load	38	35	40	185

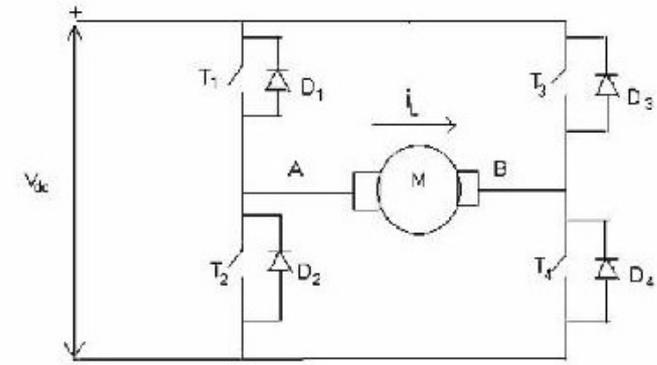
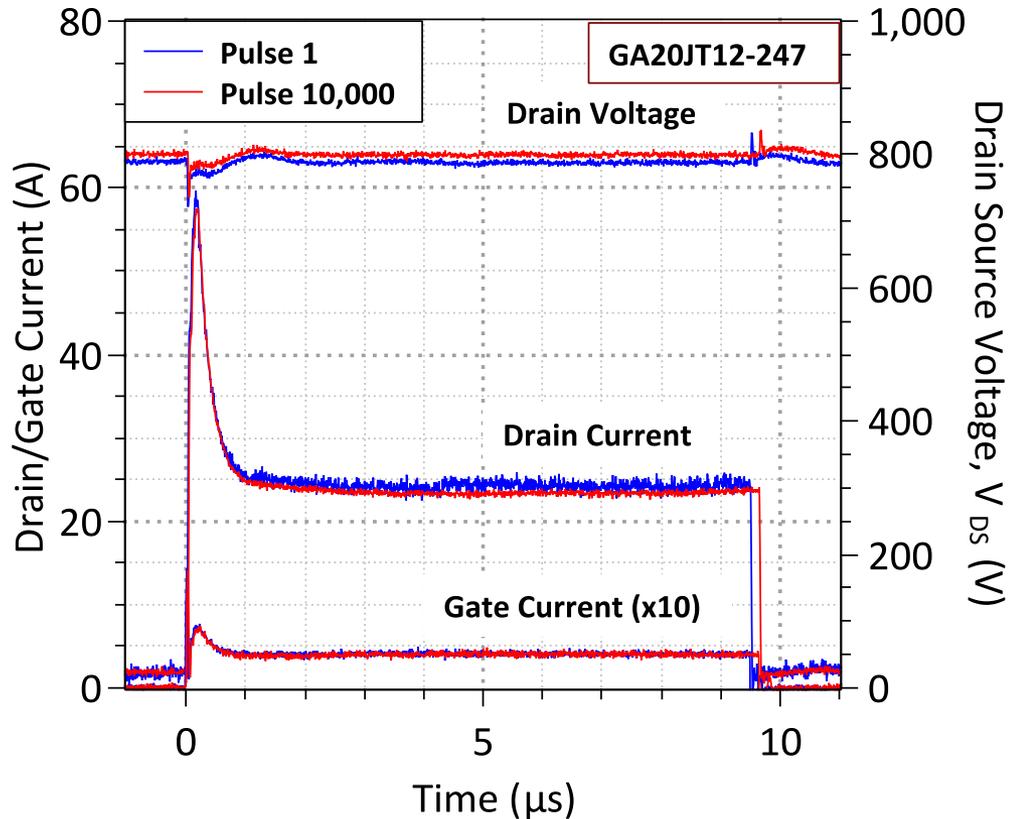
* The low transconductance in SiC MOSFETs causes the transition from triode (ohmic) to the saturation (constant current region) to be spread over a wide range of drain current. The R_{on} of these parts increases from 92 mΩ at 20 A to > 100 mΩ at the rated 32 A.

1200 V/60-80 mΩ SiC Transistors – Switching Figures of Merit

Category	FOM	T _J	SiC SJT	SiC MOSFET#1	SiC MOSFET#2	SiC JFET
Soft Switching (ZVS) [1]	NHFFOM $\frac{I}{R_{on,sp} C_{oss,sp}}$	150° C	11.4	4.2	5.6	10.5
Hard Switching	$\frac{\frac{T_J - T_C}{R_{th}} - R_{on} I_C^2 D}{E_{on} + E_{off}}$	150° C	592	601	567	380

- [1] I.-J.II-Jung Kim et al. in *Proc. Int. Symp. Power Semiconductor Devices ICs, Yokohama, Japan, 1995, pp.309–314.*
- In ZVS, the power transistor is turned on with zero voltage across it. Therefore, ZVS is insensitive to the Miller (cross-over) power losses, and only depends on Q_{OSS}, since the output capacitance needs to be fully discharged before the start of the next switching cycle.

Short Circuit Ruggedness



- Simultaneous application of operating voltage and full, rated current
- $>10 \mu\text{sec}$ short circuit testing successful

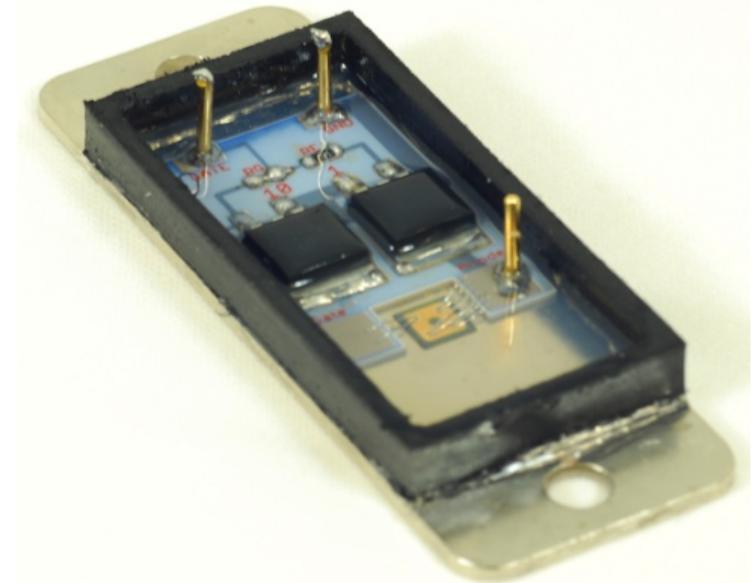
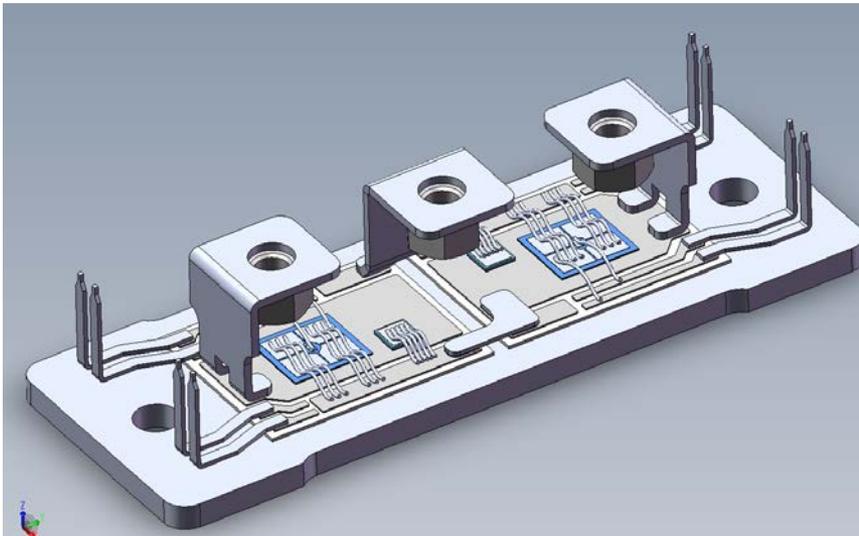
SPICE Models Developed and Published

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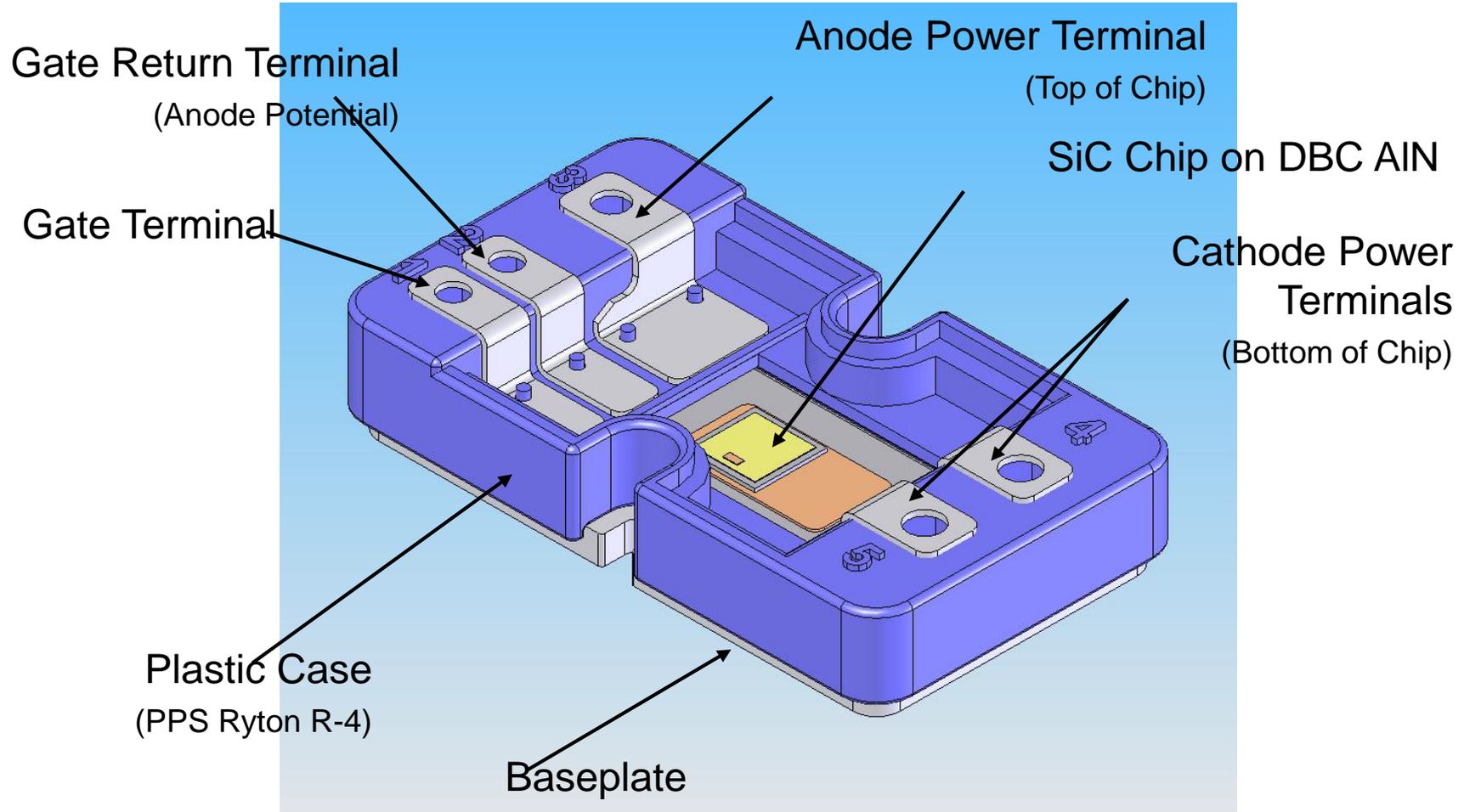
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*   $Revision: 1.0           $
*   $Date:      29-MAY-2015   $
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*   GeneSiC Semiconductor Inc.
*   43670 Trade Center Place Ste. 155
*   Dulles, VA 20166
*
*   COPYRIGHT (C) 2015 GeneSiC Semiconductor Inc.
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*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
* Start of GA10SICP12-247 SPICE Model
.SUBCKT GA10SICP12 DRAIN GATE SOURCE
Q1 DRAIN GATE SOURCE GA10SICP12_Q
D1 SOURCE DRAIN GA10SICP12_D1
D2 SOURCE DRAIN GA10SICP12_D2
*
.model GA10SICP12_Q NPN
+ IS      9.833E-48      ISE      1.073E-26      EG      3.23
+ BF      113           BR      0.55           IKF      5000
+ NF      1             NE      2             RB      4.67
+ RE      0.005         RC      0.083          CJC      427E-12
+ VJC     3.1004        MJC     0.4752         CJE      1373E-12
+ VJE     10.644        MJE     0.21376        XTI      3
+ XTB     -1.35         TRC1    7.0E-03          MFG      GeneSiC_Semi
+ IRB     0.001         RBM     0.16
.MODEL GA10SICP12_D1 D
+ IS      4.55E-15      RS      0.0736         N      1
+ IKF     1000          EG      1.2           XTI     -2
+ TRS1    0.0054347826 TRS2    2.71739E-05    CJO     6.40E-10
+ VJ      0.469         M      1.508          FC      0.5
+ TT      1.00E-10      BV      1200          IBV     1.00E-03
+ VPK     1200          IAVE    10
.MODEL GA10SICP12_D2 D
+ IS      1.54E-22      RS      0.19          TRS1    -0.004
+ N      3.941          EG      3.23           IKF      19
+ XTI     0             FC      0.5           TT      0
+ BV      1200          IBV     1.00E-03    VPK      1200
.ENDS
* End of GA10SICP12-247 SPICE Model

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GeneSiC's commercial Phase Leg Packaging



Module Configuration



Status and Future Efforts

- **Current Status**
 - SPICE Models for 1200 V and 600 V SiC MIDSJT Developed
 - Demonstration of 600 V MIDSJT Completed
 - Conduction and Switching losses calculated using analytical models
 - Commercial Release of DISCRETE SJT+Diodes Completed
- **Future Efforts in Phase II**
 - Undergoing H-Bridge Circuit Level simulation for Dual-Active Bridge in Energy Storage relevant 400 kW System
 - Circuit Efficiencies to be compared between Monolithically Integrated SJT-Diodes with DISCRETE SJT+Diodes



Grant Details

- Principal Investigator: Dr. Siddarth Sundaresan
- Program Manager: Dr. Ranbir Singh
- Grantee:
 - GeneSiC Semiconductor Inc.
 - 43670 Trade Center Place
 - Suite 155
 - Dulles VA 20166
 - +1 703 996 8200 (ph)
 - ranbir.singh@genesicsemi.com