Acknowledgments

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- **DOE Topic Number 8**: High Voltage DC-Link Power Conversion System for Energy Storage Applications
- **Subsection b.** Advanced Semiconductor Switches Modules for High Voltage Energy Storage Systems
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USCi colleagues: Dr. Larry Li, Dr. Leonid Fursin, Dr. Petre Alexandrov, Mike Lange, Matt Fox, Guy Moxey, Mari-Anne Gagliardi & Dr. Chris Dries

USCi Partner: Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy’s National Nuclear Security Administration under contract DE-AC04-94AL85000.
Contents

- Storage Applications
  - Role of Power Conversion
- Project Goals & Timeline
- Overall Project Objective
  - Impact
- Design Approach
  - Reliability Focused
- Device & Half-Bridge Simulations
- Next Steps
- Conclusions
Every storage technique involves Power Conversion where the most common interface is a DC-Link.

The Present Cost of Power Conversion Stages is ~30% or Higher of Total System Cost!
- USCi proposes a 6.5 kV Switch Module that can enable a DC-Link Voltage up to 5 kV using SiC wide bandgap devices:
  - Junction Field Effect Transistors (JFETs) and Junction Barrier Schottky Diodes (JBS’s)

- Presently, DC-Links reside at ~900 to 1100 V
  - Limited by the switch voltage ratings ~ 1200 V Si-IGBTs

- USCi has partnered with Princeton Power Systems to gain critical insight into the impact of a medium voltage switch on inverter systems

- **Phase I** – Design of SiC Power Module and Epitaxial Growth (9 months)
- **Phase II** – Fabrication of Power Module and Demonstration of 5 kV DC-link Power Inversion (2 years)

Start: 6/28/12 | Finish: 1/7/15
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Phase I: Design & Epitaxial Growth | March 1, 2013 | Phase II: Device Fabrication & 5 kV DC-Link Power Inversion Demonstration | 2014 | 2015
Overall Project Objective

- How does higher DC-Link voltage help on the Power Conversion System Level?
  - Higher Voltage Means Lower Current
  - Losses ~ $I^2R$ and Switching - More Efficient, Smaller Systems, Less Cooling
  - High Operating Frequency – Reduces Magnetics Drastically
  - Reduced Footprint, Balance-of-System, and Cost

Si-IGBTs

2 level Inverter
900 V DC-Link
I ~ 300 A/switch
$f < 10$ kHz

6.5 KV SiC-JFETs

2 level Inverter
5 kW DC-Link
I ~ 40 A/switch
$f > 20$ kHz

SiC-JFETs

5 level Inverter
20 kV DC-Link
I ~ 40 A/switch
$f > 20$ kHz
Impact of an all SiC Power Module on Systems

- How does a 6.5 kV SiC Switch Module Impact Storage Systems?
  - Costs and Efficiency of Power Conversion Stages

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Improvement over Si-IGBTs</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Efficiency</td>
<td>1.5-2.0% (~96 to 98%)</td>
<td>JFETs &amp; JBSs both contribute to efficiency improvements of module</td>
</tr>
<tr>
<td>Switch Frequency</td>
<td>2-5 X (&lt;10 kHz to &gt; 20 kHz)</td>
<td>Greatly Impacts Magnetics</td>
</tr>
<tr>
<td>Operating Current</td>
<td>X 10 Reduction (~400 A to 40 A)</td>
<td>Greatly Impacts Magnetics &amp; BoS</td>
</tr>
<tr>
<td>Operation Temperature</td>
<td>1.5 X (150 C to 250 C)</td>
<td>Reduces Cooling Complexity</td>
</tr>
</tbody>
</table>
### Why a Normally-off SiC JFET?

<table>
<thead>
<tr>
<th>Switch type</th>
<th>Property</th>
<th>Norm Off SiC JFET</th>
<th>SiC MOSFET</th>
<th>SiC Bipolar</th>
<th>Si IGBT Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC JFET</td>
<td>kV</td>
<td>&gt;&gt;6.5 kV</td>
<td>&gt;&gt;6.5 kV</td>
<td>&gt;&gt;&gt;6.5 kV</td>
<td>&lt;6.5 kV</td>
</tr>
<tr>
<td>SiC MOSFET</td>
<td>Switching speed</td>
<td>&gt;20 kHz</td>
<td>&gt;20 kHz</td>
<td>&lt;20 kHz</td>
<td>&lt;5 kHz</td>
</tr>
<tr>
<td>SiC Bipolar</td>
<td>Switching Loss</td>
<td>1X</td>
<td>1X</td>
<td>~5X</td>
<td>~5X</td>
</tr>
<tr>
<td>Si IGBT Stack</td>
<td>Driver Complexity</td>
<td>Simple</td>
<td>Simple</td>
<td>Complex</td>
<td>Moderate</td>
</tr>
<tr>
<td></td>
<td>Operational Tj</td>
<td>&gt;250°C</td>
<td>150°C</td>
<td>&gt;250°C</td>
<td>150°C</td>
</tr>
<tr>
<td></td>
<td>Reliability</td>
<td>No MOS Gate - Robust</td>
<td>MOS Gate - Reliability Concern</td>
<td>V drift (BPD) - Reliability Concern</td>
<td>Robust</td>
</tr>
</tbody>
</table>

- Cascode Configuration can utilize normally-on SiC JFETS - Very attractive option
- But is limited in operation temperature by the Si MOSFET
- USCi targets high temperature operation to reduce cooling needs → SiC Normally-off JFET
- **Design Focus on Reliability**
  - Utilize only N-type 4H-SiC Material for all devices in the module
    - Unipolar SiC devices more mature than bipolar - not sensitive to Basal Plane Defects
  - No MOS Gate
    - High Mobility N-channel
  - Modest Current Densities - keep heat generation low (50 A/cm²)
    - Less Stress on Packaging
  - Existing SiC Schottky Diode Market Proof of N-type SiC Material Reliability
USCi Schottky Reliability
N-type Unipolar Epitaxy

- **High Temperature Reverse Bias,** $T_{\text{case}} = 175^\circ \text{C}$

- **Intermittent Operation Lifetime** $\Delta T_j = 100^\circ \text{C}$

1200 V, 10 A
Junction Barrier
Schottky Diode
TO-220

Current Pulse = 3 min on/off

$V_r$ depicted is at end of heating pulse
6.5 kV Half-Bridge Expected Performance

**Parameter** | **Target**
--- | ---
Max DC-Link Voltage | ~ 5 kV
Max Current | 61 A
Target $R_{on}$ (RT) | 33 mΩ
Switching Speed | ~20 kHz
Max Ambient Temp | ~100°C
Max Junction Temp | ~270°C

- Full Device Simulation using TCAD Sentaurus
- Device Simulation Complete
- Packaging Simulation in Progress
- Gate Driver Design in Progress
Next Steps

- **Phase I Tasks**
  - Device Module Simulations
  - Packaging Simulations
  - Gate Driver Design
  - Define Manufacturing Concept
    - Epitaxial Growth of 6.5 kV JFET and JBS material

- **Future Phase II Tasks**
  - Device Fabrication
  - Module Assembly
  - Half-Bridge Module Demonstration with Princeton power Systems
  - **Target:** Alpha prototype by end of phase II (TRL 6)
United Silicon Carbide is proposing a tractable approach to developing a 6.5 kV medium voltage half-bridge switch module

- Will enable a 5 kV DC-Link voltage which will greatly impact Storage Systems by reducing costs of power conversion stages
- Impact current system designs as well as create a platform for highly innovative inverter/converter designs

Module is based on an all SiC half-bridge module

- Utilizes Vertical JFETs and JBS’s
- Focusing on reliability aspects of SiC materials
- All N-type SiC material system
- No MOS–Gate material

Currently in Phase I

- Device Simulations Completed
- Current Efforts focused on Epitaxial Growth of 6.5 kV material
Thank You!

USCi Welcomes Your Questions

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