Development of an Integrated Power Controller Based on HT SOI and SiC

Joseph A. Henfling, Stan Atcitty, Frank Maldonado, Sandia National Laboratories
Randy Normann, PermaWorks
Nicholas Summers, Trevor Thornton, ASU

Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin company, for the Untied State Department of Energy under contract DE-AC04-94AL85000.

SAND Number: 2009-5722C
Overview

• Program Goals for HT Power Controller
  – Ultimately a single module solution

• Power Controller Design Details
  – PWM options (Microcontroller, FPGA)
  – High side gate control
  – HT MESFET demonstrated to drive SiC JFET in low side applications

• Test Results

• Future work

• Conclusions
Project Goals

- Design HT power controller that can be integrated into a single module
  - **Benefits include:**
    - Size reduction of power controllers
      - Integration of the SOI based controller with (near) SiC power devices
    - Eases thermal management requirements
    - Increase reliability
      - Designed using HT components and elimination of board-level interconnects
    - Increase efficiency
      - Optimized to fully exploit the benefits of using SiC technology in power controllers
        - Higher breakdown voltage coupled with a lower “ON” resistance can reduce energy losses by 3-4%
    - High voltage capable designs (SiC JFET’s rated at 1200 Volts)
- Demonstrate HT power controller using discrete devices
  - Using HT devices:
    - SOI control circuits – 240 C
    - SiC Power devices – 300 C
- Establish commercialization path to quicken the adaptation of energy-saving SiC technology
Block Diagram of the Power Controller

60 Hz sine wave oscillator / sync for power line

Input DC Voltage (up to 1000 Volts)

60 Hz sine wave oscillator / sync for power line

ADC

Smart Grid Interface

FPGA/ EEPROM

HT 8051 Gate Controller and System Monitor

Level Shifter

PWM

JFET Gate Drive

H Bridge

JFET Gate Drive

PWM

JFET Gate Drive

H Bridge

JFET Gate Drive

Level Shifter

PWM

JFET Gate Drive

Load

Vout = Vin (1- Duty Cycle)

Input DC Voltage (up to 1000 Volts)
Block Diagram of the System Monitor

- **Sensors**
  - Temperature, output current and voltage

- **32 KB RAM**
  - Honeywell

- **Microprocessor**
  - Honeywell

- **Crystal Oscillator**
  - Quartzdyne, Honeywell

- **HT83SNL00 with internal “boot strap” program and interface circuits**
  - Sandia/Honeywell

- **Signal Conditioners**
  - Honeywell

- **Analog-to-Digital Converter**
  - Cissoid

- **5 Volt Reference**
  - Cissoid

- **Transmit Circuit**
  - Honeywell, Cissoid

- **5 Volt Regulator**
  - Cissoid

- **10 Volt Regulator**
  - Honeywell

- **5 Volt Regulator**
  - Cissoid

- **External Power Supply**
H-Bridge PWM Drive

PWM Gate Drive Waveform

PWM Gate Drive at Q1 and Q3; 60Hz at Q2 and Q4
Microcontroller-Based PWM

Probably not fast enough
FPGA-Based PWM

• FPGA generated a square wave
• Square wave was filtered and measured using a 10 bit A/D converter by the FPGA
• FPGA adjusted the pulse width based on the reference sine wave
Test Setup
Test Results

- This graph shows the output waveform during one of the lab tests. Test conditions were:
  - 240°C ambient temperature
  - JFET case temperature approximately 280°C
  - Supply voltage was 100 Volts

Green and blue traces are the voltages at the load. Yellow trace is the current measurement and the red is the differential voltage across the load (divided down).
Note: Prototype design exaggerated the dead band between cycles to ensure the JFETs were not damaged due to timing issues. This substantially reduced the overall efficiency. Future work will eliminate the excessive dead band.

Scope image depicting the gate drive for the H bridge:
Yellow trace is high side A, blue is low-side B, red is high-side B and green is low-side A.
Proposed Integrated Power Controller

HV Converter to Control Logic Voltage

Power Distribution

State Machine (FPGA)

Non-Volatile Memory

Microcontroller

High Voltage DC

Smart Grid Interface

SOI Gate Control

SJT Micropower Gate Driver

Analog-to-Digital Converter

SiC Power Devices

Inductive Load (Motor)

To Smart Grid Controls

Dotted line represents components of the proposed MCM
Aluminum Nitride Substrate

Controller and gate drive MCM

SiC MCM

Potentially Same Substrate for MCM’s

<table>
<thead>
<tr>
<th>Aluminum Nitride</th>
<th>Units of Measure</th>
<th>SI/Metric</th>
<th>(Imperial)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mechanical</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Density</td>
<td>gm/cc (lb/ft³)</td>
<td>3.26</td>
<td>(203.5)</td>
</tr>
<tr>
<td>Porosity</td>
<td>% (%)</td>
<td>0</td>
<td>(0)</td>
</tr>
<tr>
<td>Color</td>
<td>—</td>
<td>gray</td>
<td>—</td>
</tr>
<tr>
<td>Flexural Strength</td>
<td>MPa (lb/in²x10^6)</td>
<td>320</td>
<td>(46.4)</td>
</tr>
<tr>
<td>Elastic Modulus</td>
<td>GPa (lb/in²)</td>
<td>330</td>
<td>(47.8)</td>
</tr>
<tr>
<td>Shear Modulus</td>
<td>GPa (lb/in²x10^6)</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Bulk Modulus</td>
<td>GPa (lb/in²x10^6)</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Poisson’s Ratio</td>
<td>—</td>
<td>0.24</td>
<td>(0.24)</td>
</tr>
<tr>
<td>Compressive Strength</td>
<td>MPa (lb/in²x10^6)</td>
<td>2100</td>
<td>(304.5)</td>
</tr>
<tr>
<td>Hardness</td>
<td>Kg/mm²</td>
<td>1100</td>
<td>—</td>
</tr>
<tr>
<td>Fracture Toughness K&lt;sub&gt;IC&lt;/sub&gt;</td>
<td>MPa·m&lt;sup&gt;1/2&lt;/sup&gt;</td>
<td>2.6</td>
<td>—</td>
</tr>
<tr>
<td>Maximum Use Temperature (no load)</td>
<td>°C (°F)</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td><strong>Thermal</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>W/m<em>K (BTU/in²</em>hr*°F)</td>
<td>140–180</td>
<td>(970–1250)</td>
</tr>
<tr>
<td>Coefficient of Thermal Expansion</td>
<td>10&lt;sup&gt;-6&lt;/sup&gt;C (10&lt;sup&gt;-6&lt;/sup&gt;/°F)</td>
<td>4.5</td>
<td>(2.5)</td>
</tr>
<tr>
<td>Specific Heat</td>
<td>J/Kg<em>K (Btu/lb</em>°F)</td>
<td>740</td>
<td>(0.18)</td>
</tr>
<tr>
<td><strong>Electrical</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric Strength</td>
<td>ac-kv/mm (volts/mil)</td>
<td>17</td>
<td>(425)</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>@ 1 MHz</td>
<td>9</td>
<td>(9)</td>
</tr>
<tr>
<td>Dissipation Factor</td>
<td>@ 1 MHz</td>
<td>0.0003</td>
<td>(0.0003)</td>
</tr>
<tr>
<td>Loss Tangent</td>
<td>@ 1 MHz</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Volume Resistivity</td>
<td>ohm·cm</td>
<td>&gt;10&lt;sup&gt;14&lt;/sup&gt;</td>
<td>—</td>
</tr>
</tbody>
</table>

http://www.accuratus.com/index.htm
Future Work

• “Fine-Tune” prototype design
  – Design, fabricate and test a version 2 board to optimize system efficiency. Improvements include:
    • Enhancing the high side gate drive of the H bridge
    • Mitigating the current spikes
    • Minimizing the switching “dead time”
    • Optimizing the output filter
    • Improving microcontroller design.
      – Better control of the power devices.
      – Active feedback

• White paper on future packaging options to enhance commercial viability.
Conclusion

• A prototype microcontroller-based HT power controller was successfully demonstrated at 240 °C.
• It had basic control capabilities including monitoring the JFET case temperature and safely shutting the system down if a programmed temperature was exceeded.
• High side / Low side SOI gate drive for the JFET power devices was demonstrated.
• SOI MESFET gate drive was also successfully tested.
• In summary, by combining SOI control and drive circuits with SiC, an intelligent system capable of operation up to 240 °C (JFET junction temperature approaching 300 °C) was successfully demonstrated.
Collaborative Effort with Academia and Industry

• DOE Funded
  – Participants include:
    • Sandia (Lead)
    • ASU (Circuit simulation, fabrication of test circuits using HT MESFET – JFET gate drive)
    • PermaWorks (Inverter design simulation and fabrication of HV supply)
  – Commercial-of-the-Shelf suppliers
    • Honeywell SSEC
    • Cissoid
    • SemiSouth

The authors would like to thank the Department of Energy Office of Electricity and Gil Bindewald for financial support of this research.