“High Power Silicon Carbide Inverter Design -- 100kW Grid Connect Building Blocks ”

Leo Casey Bogdan Borowy Gregg Davis
SatCon Technology Corporation
leo.casey@satcon.com

EESAT 2005

Stan Atcitty of Sandia National Laboratories

Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy’s National Nuclear Security Administration under contract DE-AC04-94AL85000.

ACKNOWLEDGMENTS

- Funded by the Small Business Innovation Research (SBIR) program of the U.S. Department of Energy (DOE/ESS - Dr. Imre Gyuk, Mgr.), and managed by Sandia National Laboratories (SNL).

“High Power Silicon Carbide Inverter Design”

Overview

- **Company**
- **Application**
- **SiC Technology – Potential, Status**
- **Devices**
- **Roadmap**
- **Design**

Acknowledgements

NORTHROP GRUMMAN

CREE

SemiSouth

AIR FORCE RESEARCH LABORATORY

DARPA

DEPARTMENT OF ENERGY · UNITED STATES OF AMERICA

ARL

OFFICE OF ONR NAVAL RESEARCH

Sandia National Laboratories

EPRI Electric Power Research Institute

TARDEC

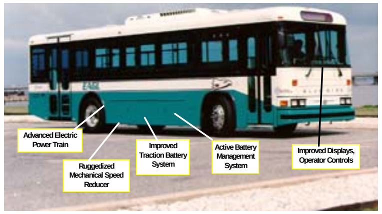
SatCon Highlights

Technology … Applications … Products

Today

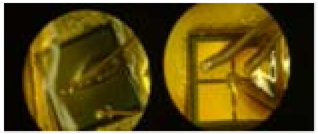
- 200 Employees
- 3 Divisions

Technology



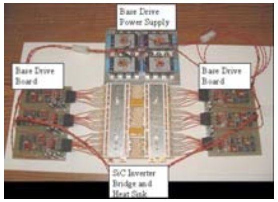
BEACON 1997

2003 Subsidiary Corporations



WEC/NG 1999

InverPower 2001



Patriot - 1992

FMI & HiComp 1998

Magmotor 1997

1985 MIT-DRAPER

Applications

High Bandwidth Controls

Packaging & Thermal Management

Electric Machines & Magnetics

Modular Power Electronics

Motivation for Utility Scale Storage

- Increasing electrification, dominant secondary source of energy, Electricity is >1/3 of our 100 Quad Energy Economy
- Grid is a BEAUTIFUL thing
  - Energy moves at the speed of light
  - Rugged Electro-mechanical generators
  - Spinning "reserve"
  - Excess capacity (>15% is critical) **SIZED FOR 20%+**
  - Low Impedance – typically 1% of rating at PCC
  - Fault clearance
  - Overload
  - ac – Simple Impedance Transformation, and Isolation
- Beautiful – but complex, congested
  - Distributed network with no significant energy storage
  - Supply must equal demand
  - Load transients (generator power angle)
  - System stability problems (minimal local control), tap-changing, relaying, v and f droop
  - Time constraints of protective devices
- Importance of storage to address
  - Distribution (remoteness of generation and utilization)
  - Load leveling (excess capacity), energy arbitrage
  - Power Quality
  - Intermittent Renewables

100 Quads = 100 exajoule (100.10^{18}J)

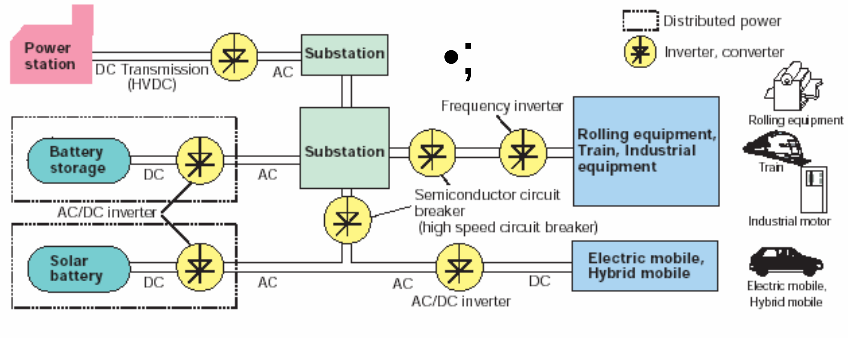
NOTE: Major transmission bottlenecks as identified in NERC reports, TLR log files, POST studies, press accounts, and national energy reports.

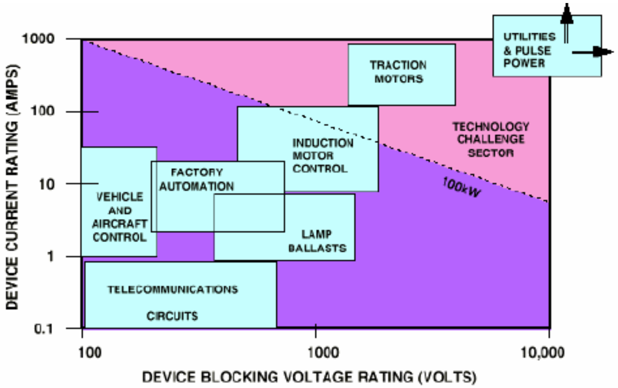
Electricity Infrastructure

Transmission SCADA control points	
FERC grid monitor/control	12
Network Reliability CoordinatingCenters	20
Regional Transmission Control Centers	130
Utility control centers	>300
Power plants	10,500
Large (>500 MW)	500
Small (<500 MW)	10,000
Transmission Lines	680,000 miles
Transmission substations	7,000
Local distribution lines	2.5 million miles
Local distribution substations	100,000

Some Potential SiC (WBG) Impacts on Grid

- **Relaying** (electromechanical is 6-10 cycle, solid-state for LV, MV, HV)
  - Isolation (SSR)
  - Protection
  - Fault clearing
  - Fault limiting (SSCL)
- **Transmission Electronics** (MV, HV)
  - FACTS
  - VARS, (SVAR, DVAR)
  - DVR
  - STS
- **Grid electronics** (storage, renewables, PQ)
  - Volume
  - Weight
  - Efficiency
  - Reliability
  - Cost
  - Overload capability
  - Voltage/Power Application Range
- **Solid State Suppression**
  - Spikes
- **Solid State Transformers** (HF Link)

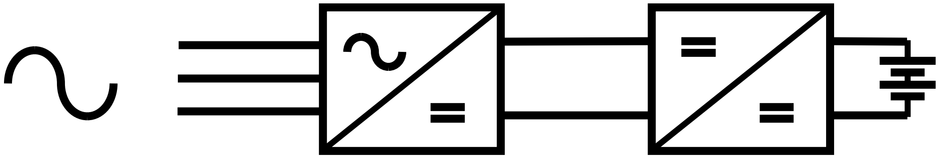




New Switch Capabilities enables new Applications

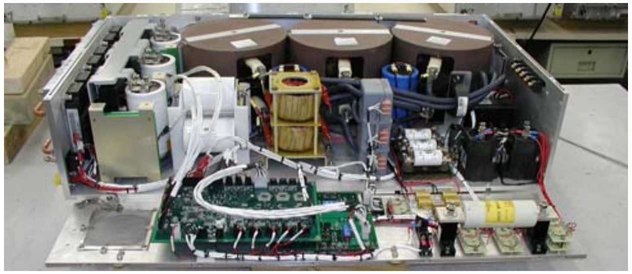
Hi-T, Hi Rad, Hi V, Hi f

Application -- Modular SiC Grid Connected Inverter



AC ← → DC ← → DC

Used today in DD(X)



- **5.7 kHz PWM hard switched, 1 pu, 100kW, 480V, 120Arms**
- **Approx 19” W x 8” H x 35” L, 375 lbs. Output LC filter, Input L EMI filter.**
- **Liquid cooled IGBT power stage, gated drive PWAs, and bulk capacitors.**
- **DC Input, 800V nominal, 1200V Pk**

- **modular 100 kW DC-AC inverters (800 VDC/480 Vac 3 phase)**
- **modern computer controls with both PLC and industrial computer with dual redundant LAN interface**
- **Expandable to 3MW**
- **SSIMs are hot swappable (electrical and mechanical)**
- **Power electronics in each SSIM are cooled by a sealed water-cooled cold plate**
- **Modular building block → volume → more cost effective application of SiC**

Power Electronic Systems

SiC

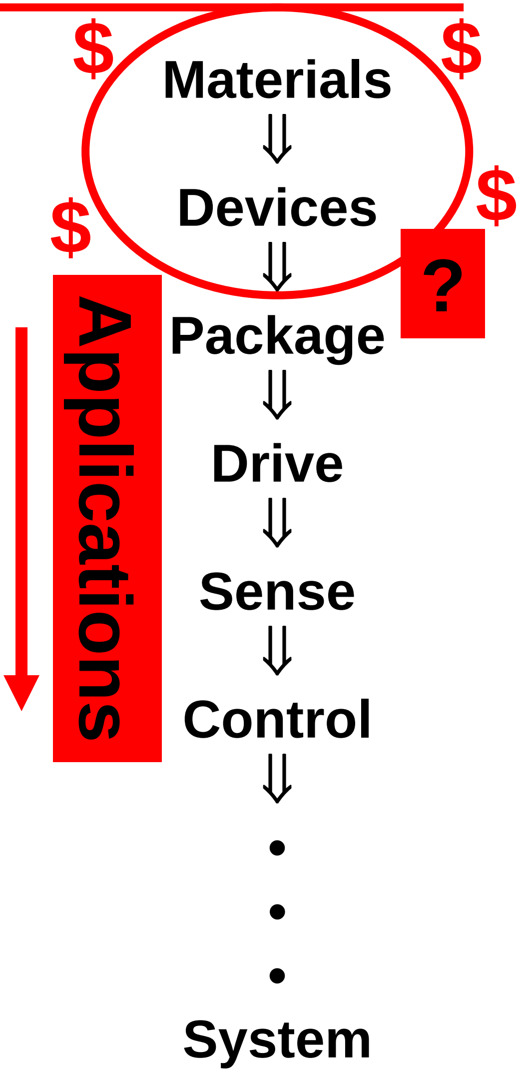
- Power Circuits
- Power Components, active and passive
- Signal Electronics
- Control
- Software
- Thermal Management
- Mechanical Design & Packaging

Full benefit comes from addressing all areas

SiC devices are NOT drop in replacements

?

Is the performance acceptable?
Are the devices reliable?
Are they consistent (matched)?
What are the next hurdles?



Materials
⇓
Devices
⇓
Package
⇓
Drive
⇓
Sense
⇓
Control
⇓
•
•
•
System

Beyond Silicon, Why? (other than temperature or radiation niches)

- Ideally in Power Conversion we use switching elements to move energy in discrete packets between source and load, with reactive elements for the energy storage and filtering, but …
  - Voltage Rating
  - Current Rating
  - Temperature Rating
  - Radiation limitation
  - Parasitics, R, C, switching time, R_{TH}, V_{ON},
  - Fundamental limitations of Switching speed
  - $$$ total cost

Si SOA

MOSFET 1983, 1.2 μs → 2004, 0.1 μs 600V, 20A

IGBT 1986, 3 μs → 2004, 1.2 μs 6kV, 150A

WBG Materials

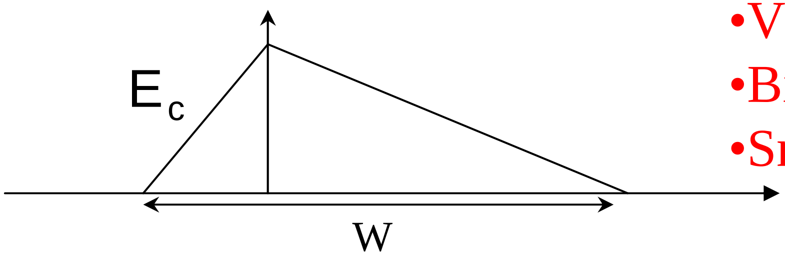
Property	Si	6H-SiC	4H-SiC	GaN	Diamond
Bandgap E_g (eV)	1.1	3.0	3.3	3.45	5.45
Dielectric Constant, ε_r	11.9	9.7	10.1	9	5.5
Breakdown Field, E_c (kV/cm)	300	2500	2200	2000	10000
Electron mobility, μ_n (cm^2/V-s)	1500	500	1000	1250	2200-4500
Hole mobility, μ_p (cm^2/V-s)	600	101	115	250	1600-3000
Thermal Conductivity λ (W/cm-K)	1.5	4.9	4.9	1.3	22
Thermal expansion ($\times 10^{-6}$)/ºK	2.6	3.8	4.2	5.6	1-2
Saturated e^- Drift Velocity, ν_{sat} ($\times 10^7$ cm/s)	1	2	2	2.2	2.7

- **Wide Band Gap, high-T, high Rad, low leakage**
- **High E_c**
- **Good λ**

+ve Impact

- Weight
- Volume
- Efficiency
- Ruggedness

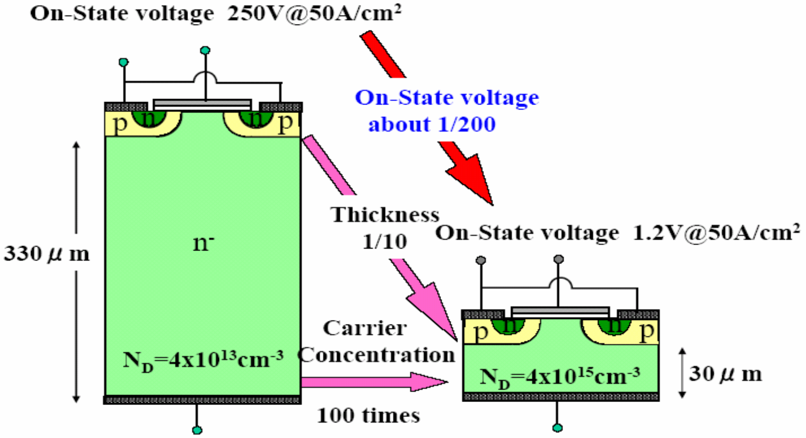
E_c – thickness, doping



- Voltage is area under curve
- Big E_C → small W
- Small W → large N_D

$$W = \frac{2 \cdot V_{MAX}}{E_C} \qquad W \approx \frac{1}{\sqrt{N_D}}$$

Materials → Benefits

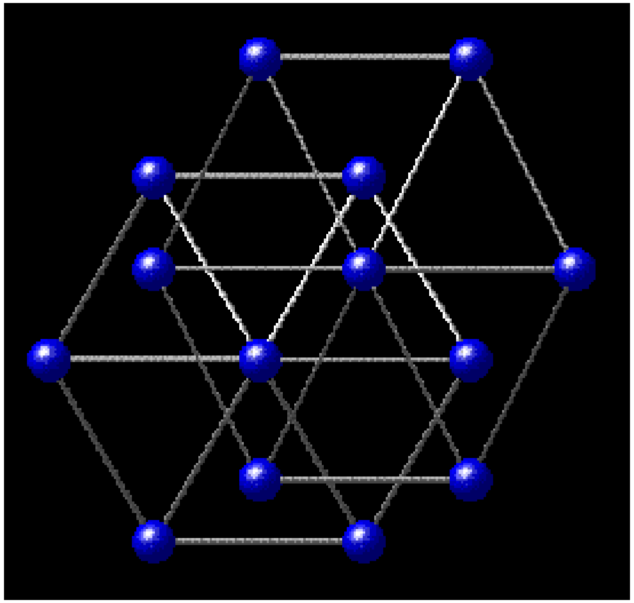


Si-MOSFET **SiC-MOSFET**

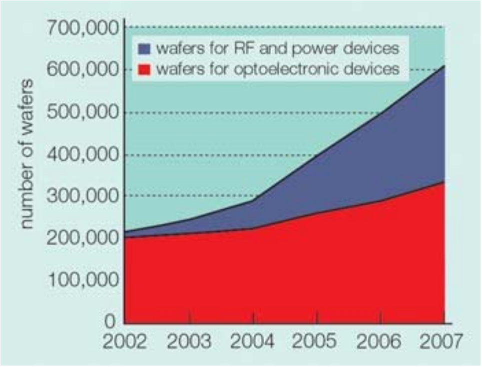
- **Order of magnitude higher breakdown field**
- **100 times higher blocking layer dopant density**
  - **→ 1/10th blocking layer thickness**
- **100 times faster for minority carrier device**
- **Larger band gap gives high temperature capability**
- **Significant improvement in thermal conductivity**
  - **→reduced heat sink requiements**
- **Improve failure mechanisms for fault conditions**
- **Higher power with future high temperature packages**

Whats in the way?

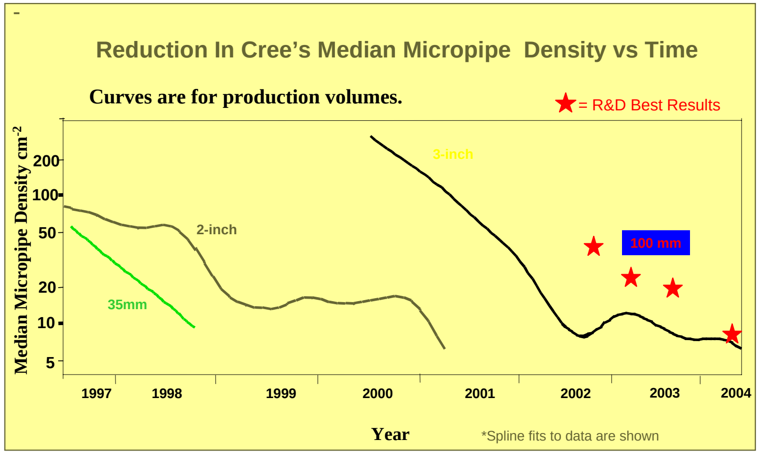
- Materials Issues
  - 180+ Xtal structures (polytytpes)
    - 6H, 15R, 4H and 3C, main candidates
  - No liquid phase, growth at 2200ºC+
    - Sublimation
    - CVD
  - Negligible Dopant diffusion, dope epi as it is grown or hi-energy implant at high-T
  - Defects
    - Micro-pipe
    - Screw dislocation
    - Basel plane defects
  - Oxide quality and reliability
  - Stability of Ohmic contacts



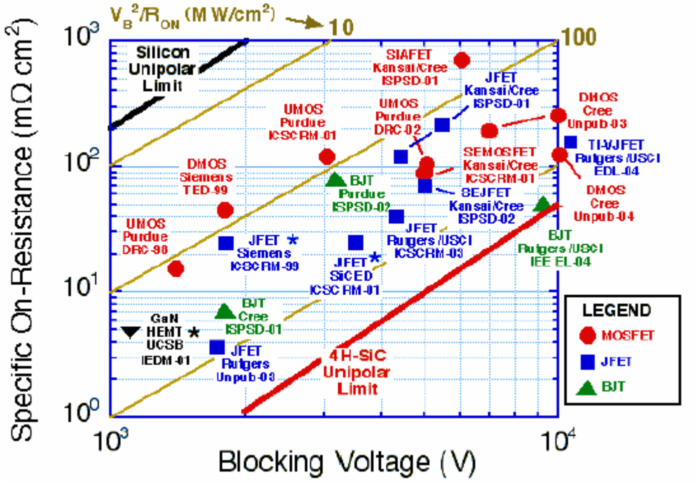
Optical Market driving SiC Wafer demand

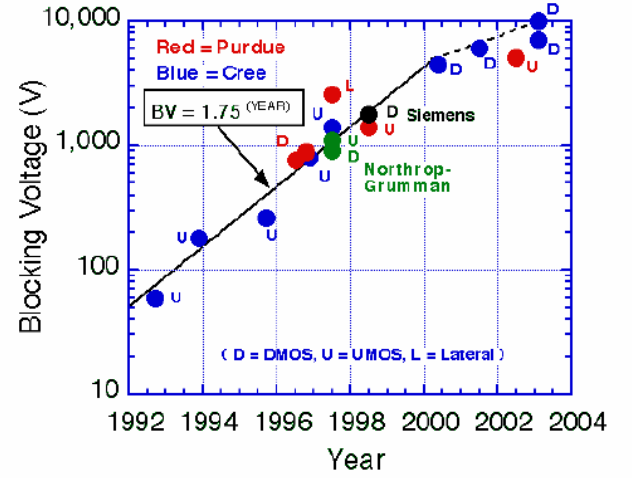


- 4 inch wafers
- Substrates for GaN LEDs
  - Better thermal conductivity
  - Good electrical conductor
- Volume has driven quality



SiC Devices Developing : Example, MOSFETs

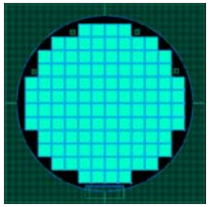


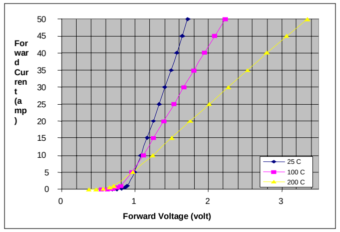


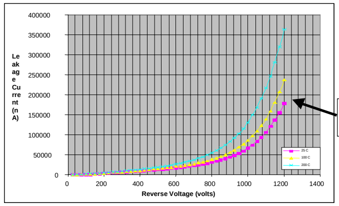
SiC Schottky

1200V/50A SiC Schottky Diode

Die size: 5.6 mm x 5.6 mm

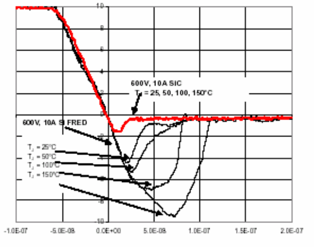






1200 V blocking @ 180µA leakage

- First commercial SiC power device (other than RF)
- 2 sources, Cree & Infineon
- 10,20 A 600,1200V

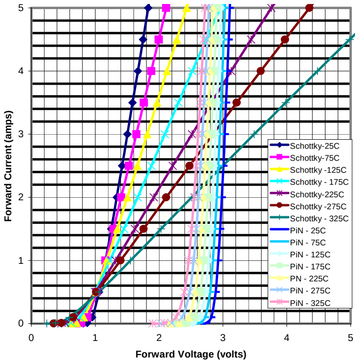


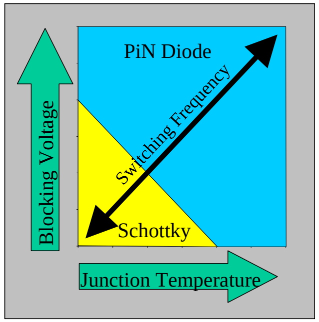
SiC Schottky diode switching characteristics are unaffected by temperature, di/dt or forward current; all of which increase reverse recovery current in silicon diodes

SiC PiN Diode

SiC Schottky vs PiN Diode

1200 volt - 5 Amp Forward I-V over Temperature

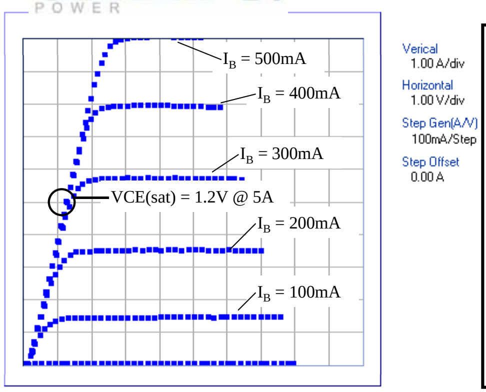


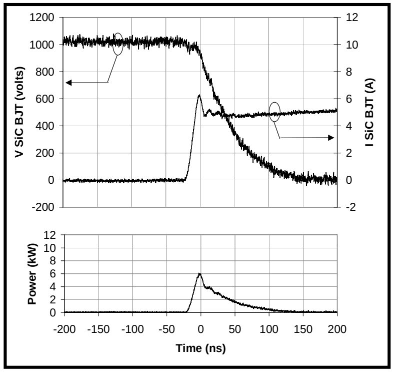


- 20kV+ devices have been demonstrated

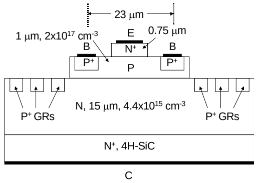
- 20kV devices have been demonstrated

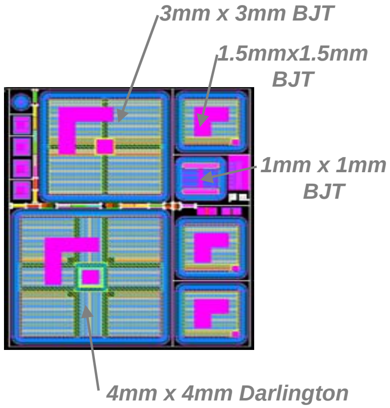
SiC Bipolar

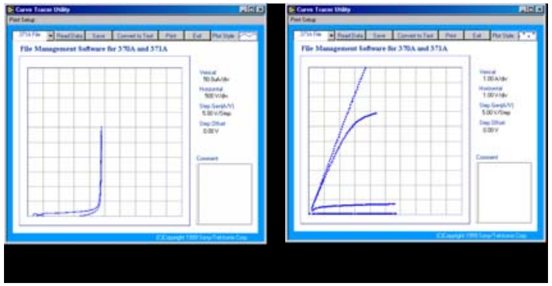




1200 V SiC BJTs







SiC JFET

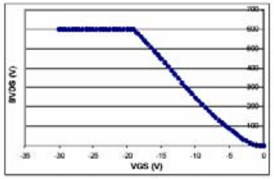


Figure 2a. BVDS vs VGS for *Normally On* VJFET

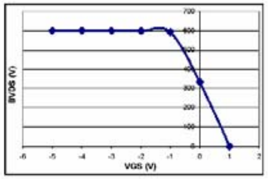
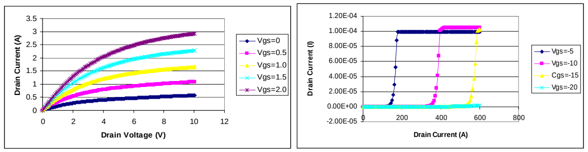
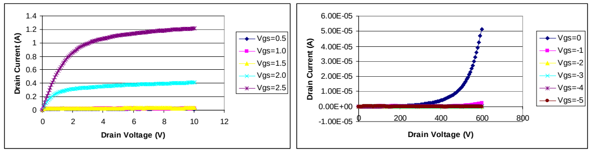


Figure 2b. BVDS vs VGS for *Quasi-Off* VJFET

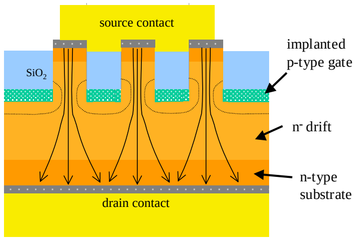
Normally-On : 7/2004



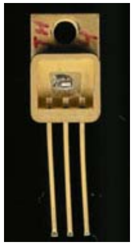
Normally Off –7/2004



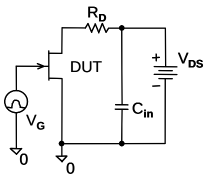
Basic device cross-section



Finished JFET in a TO-257



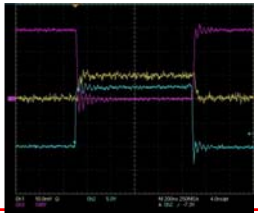
Switching Test Circuit



JEDEC Standard #24

V_{DS} = 300 V

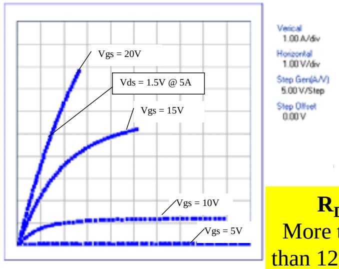
f = 20 MHz

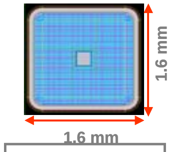


SiC MOSFET

SiC MOSFET

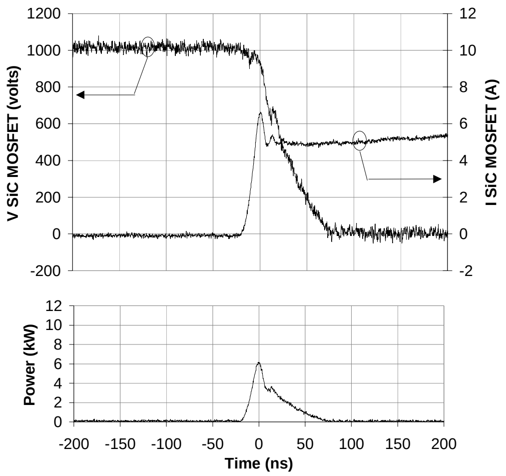
Output Characteristics @ T_j = 25°C

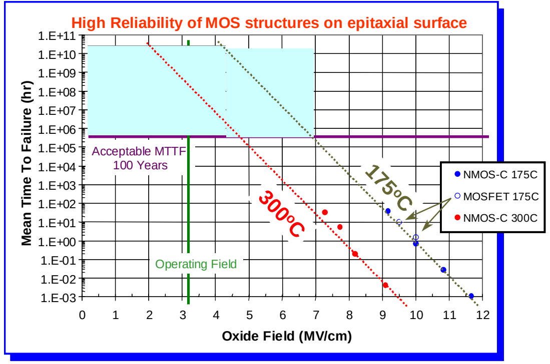




3 - Die Connected in Parallel for 5 amp Device

$R_{DS(on)}$ = 0.3 ohm
More than 30 times lower than 1200 Volt Si MOSFET

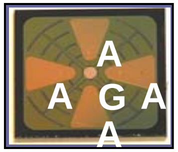




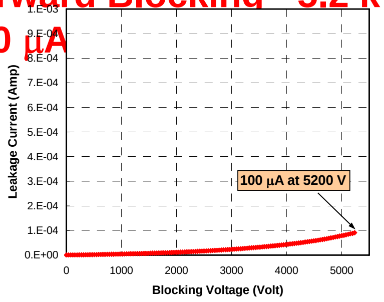
- **Native oxide is SiO_2**
- **Only WBG with native oxide**
- **Grow in Silane Environment**
- **IGBT?**

SiC GTOs

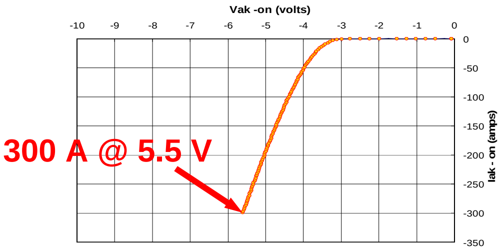
1 cm x 1 cm 4H-SiC Thyristor



Forward Blocking - 5.2 kV @ 100 µA

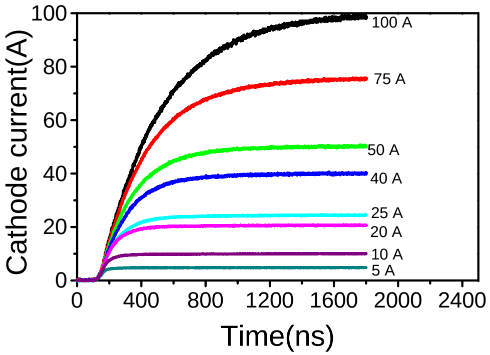


Forward I-V at 100 mA gate current

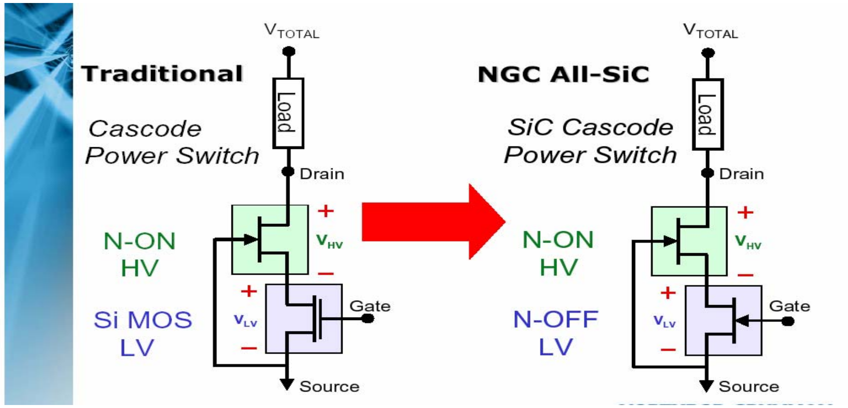


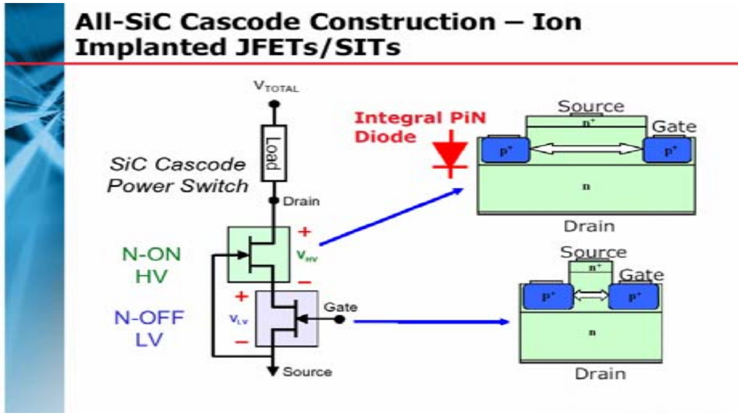
300 A @ 5.5 V

Turn-on time versus I_{AK}



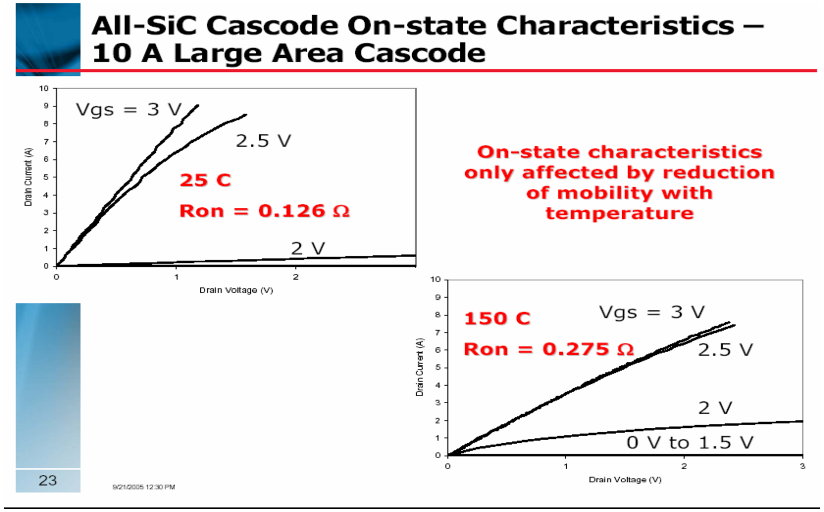
Northrop – All SiC Cascode





All-SiC Cascode Construction – Ion Implanted JFETs/SITs

NORTHROP GRUMMAN

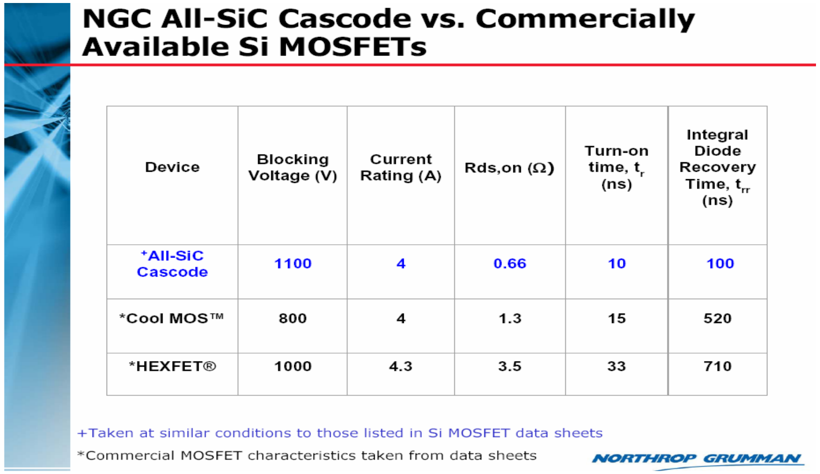


All-SiC Cascode On-state Characteristics – 10 A Large Area Cascode

On-state characteristics only affected by reduction of mobility with temperature

23

9/21/2005 12:30 PM



NGC All-SiC Cascode vs. Commercially Available Si MOSFETs

Device	Blocking Voltage (V)	Current Rating (A)	Rds,on (Ω)	Turn-on time, t_r (ns)	Integral Diode Recovery Time, t_{rr} (ns)
⁺All-SiC Cascode	1100	4	0.66	10	100
*Cool MOS™	800	4	1.3	15	520
*HEXFET®	1000	4.3	3.5	33	710

+Taken at similar conditions to those listed in Si MOSFET data sheets

*Commercial MOSFET characteristics taken from data sheets

NORTHROP GRUMMAN

Ruggedness – Hi T

25us Si IGBT test

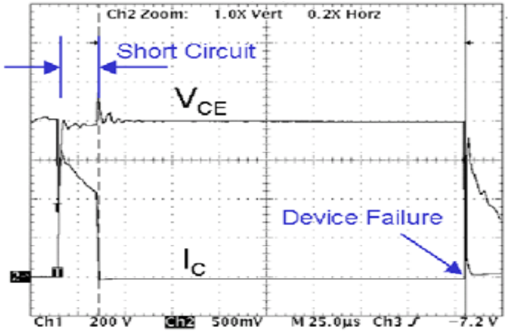
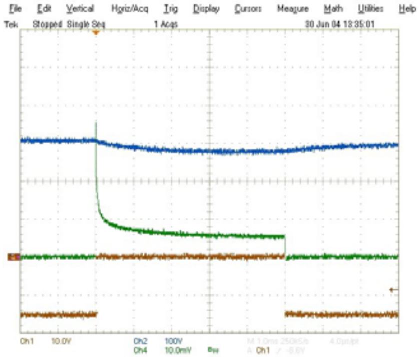


Figure 1. Experimentally measured 1200V FS-IGBT short-circuit failure.
V_{CE}:200V/div,I_C:250A/div,time:25µs/div

5ms SiC JFET test



- **Better thermal conductivity**
- **Higher Temperature Material, Dopant Stability**

“Available”SiC SOA Summary

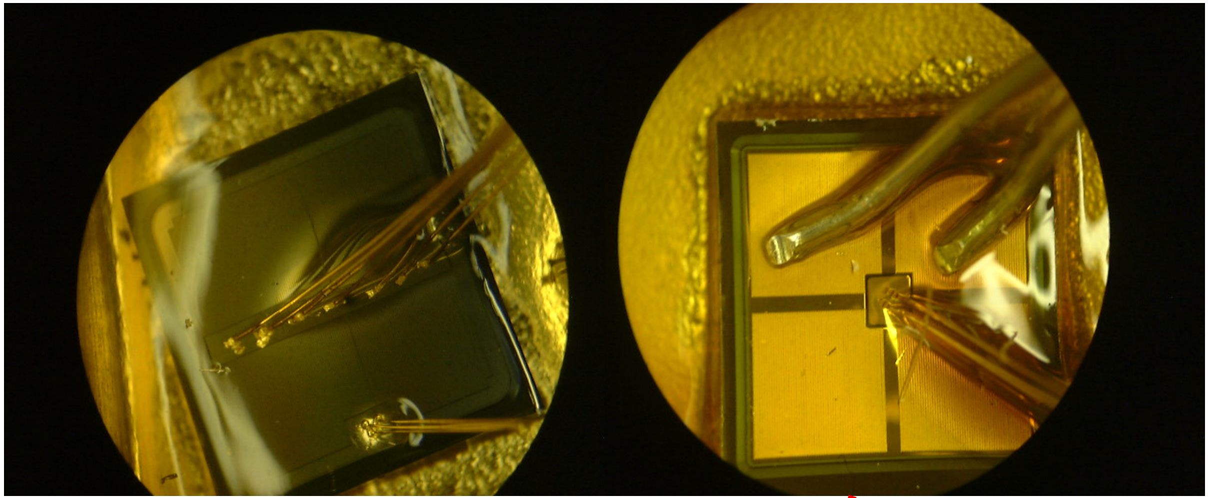
Device	Voltage (V)	Current (A)	Demonstrated Switching times
Schottky	600 1200	100 50	~ns
PIN	20,000	20	~10ns
Bipolar	1200	20	~100ns, β ~30
MOSFET	1200	10	~100ns
JFET	10,000 1,200	1 20A	~100ns

1% conduction loss at 0.67(V_{PK})

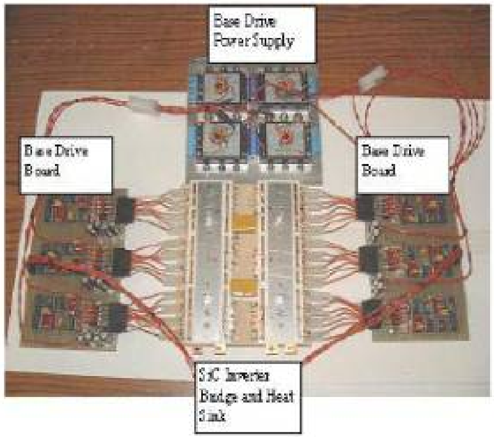
Critical that Devices Parallel well

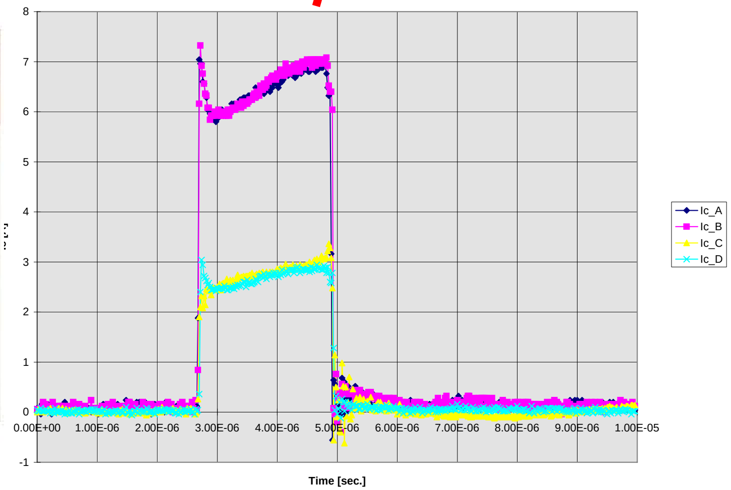
- JFETs √
- Bipolars √
- MOSFETs √

- Static
  - PTC
- Dynamic
  - Turn on
  - Turn off
- Need to be well matched
  - Over temperature
- Transitions critical



All SiC 7.5 kW, 400V, BJT

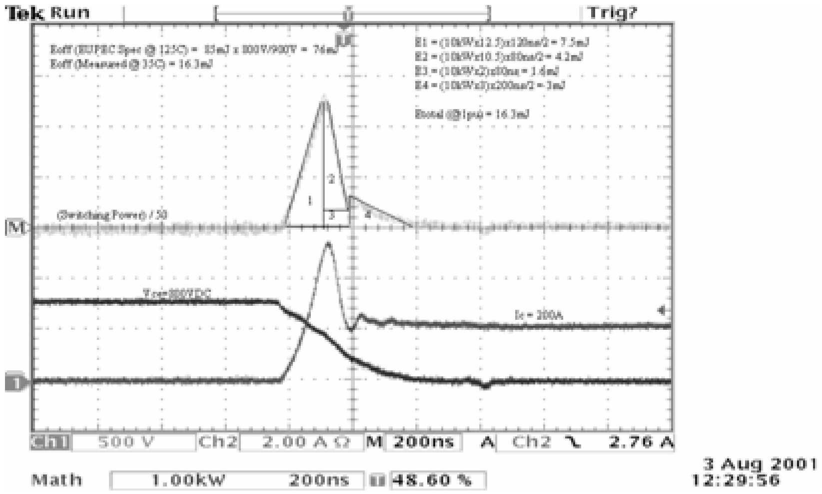


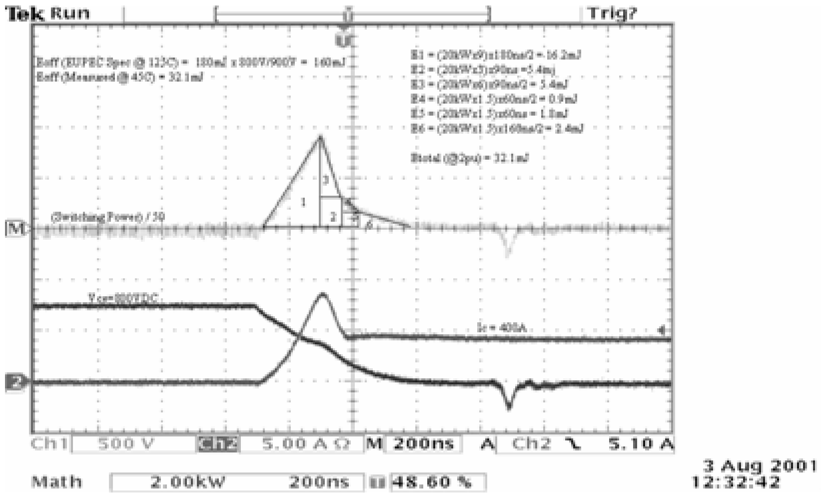


Switching Time – Loss -- Frequency

- Generally, (t_{on} + t_{off}) sets f_{sw}, losses go approximately as V.I.(t_{on} + t_{off})/2
- 1µs → 10kHz for 1%
- 100ns → 100kHz for 1%

- New Technology
  - Lower conduction and switching
  - Trade efficiency off vs. L, C

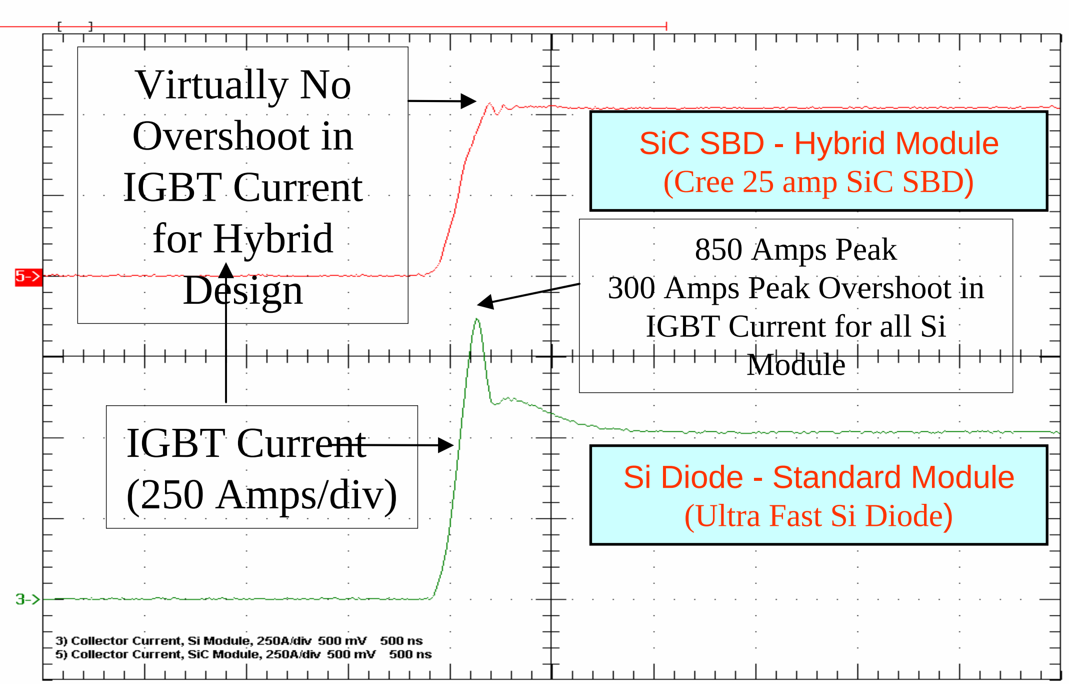




Full SiC Grid Interactive Inverter Design

	Silicon SOA	Full SiC Design
Size/Density/Efficiency	10 -- 100 W/in^3 (16 W/in^3 for module)	50 -- 500 W/in^3 (80 W/in^3 for module) (30% Vol., 20%P)
Cooling	80ºC max. liquid or 25 ºC Air	>100ºC liquid or 40-50 ºC Air
Response Time	10 ms for 5.6 kHz with V and I loops	50 µS for 100kHz with dead-beat control
High Temperature Design	Si limits entire system to < 110ºC	Partial High-Temperature design then eventually complete High-Temperature design if needed (analog degradtion)
Overload Capability	100-500 ms	10+ seconds
Robustness	10-20,000 hr. MTBF	50-100,000 hr. MTBF

Today – losses, on, off, rectifier



Virtually No Overshoot in IGBT Current for Hybrid Design

SiC SBD - Hybrid Module
(Cree 25 amp SiC SBD)

850 Amps Peak
300 Amps Peak Overshoot in IGBT Current for all Si Module

IGBT Current
(250 Amps/div)

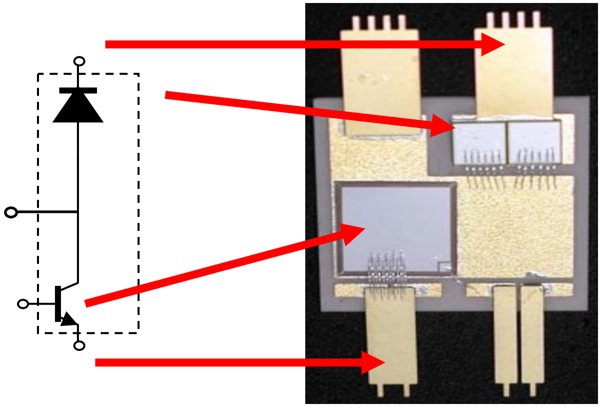
Si Diode - Standard Module
(Ultra Fast Si Diode)

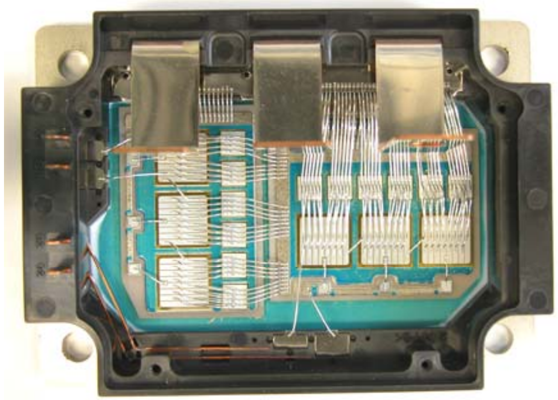
- **Losses are comparable, on, off, rect**
- **Schottky saves Rectifier**
- **Some associated turn-on**
- **.FRED → SiC, ~39% saving in sw. loss**
- **Why are turn-on loss so high?**
  - **Slow transitions**
  - **Paralleling?**
  - **Due to diode?**
- **Experiment and Simulate with rapid Turn-off (commercial devices have integrated polysilicon Rs)**

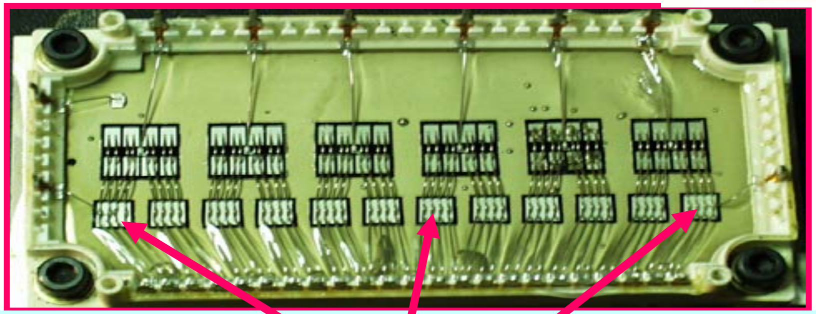
Interim Approach

Hybrid Si IGBT/SiC Schottky Diodes

Can be done today



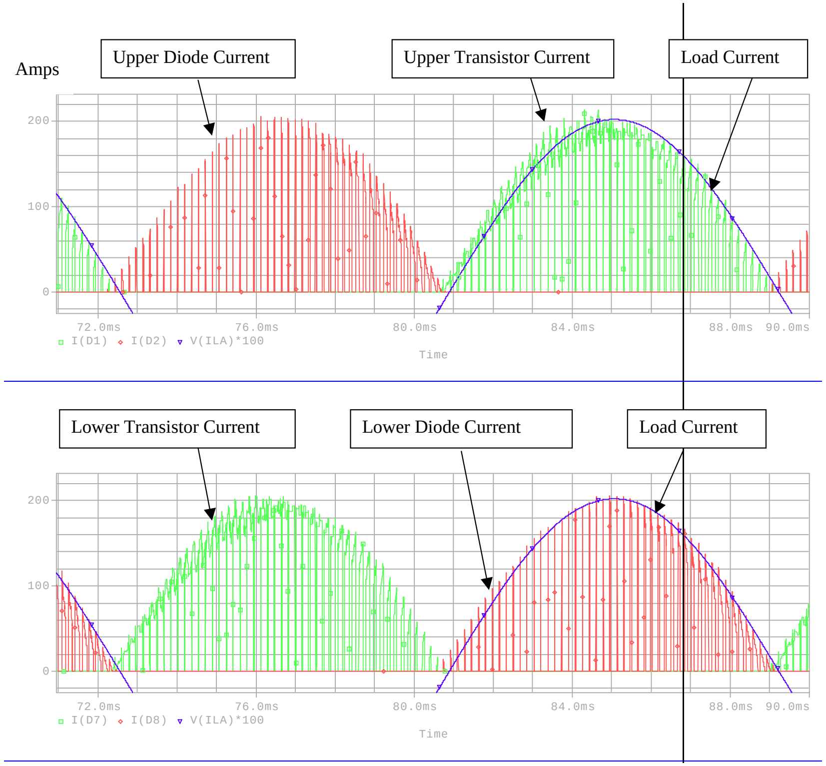


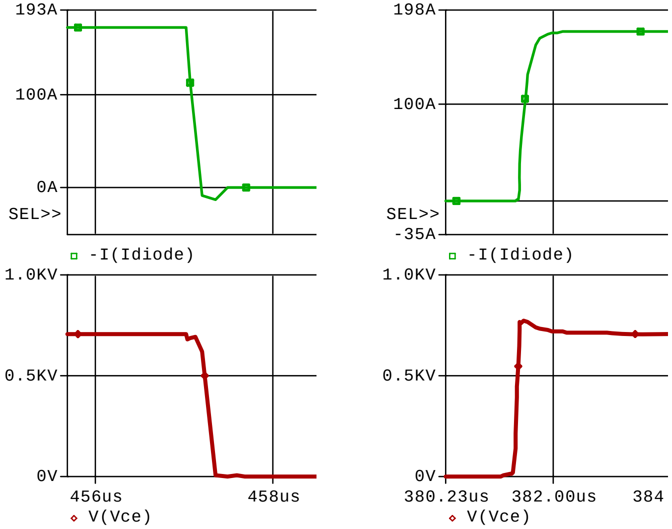


Si PiN Diodes

Replaced with SiC Schottky Diodes

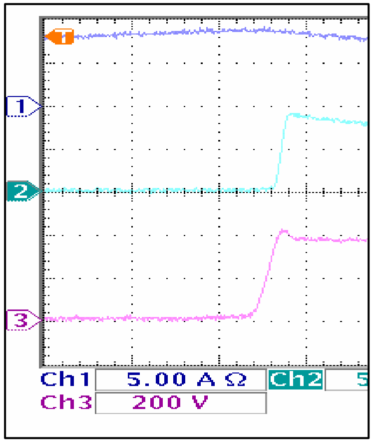
Simulations – System and Device





Turn On

Turn Off



Load Current 100A/div

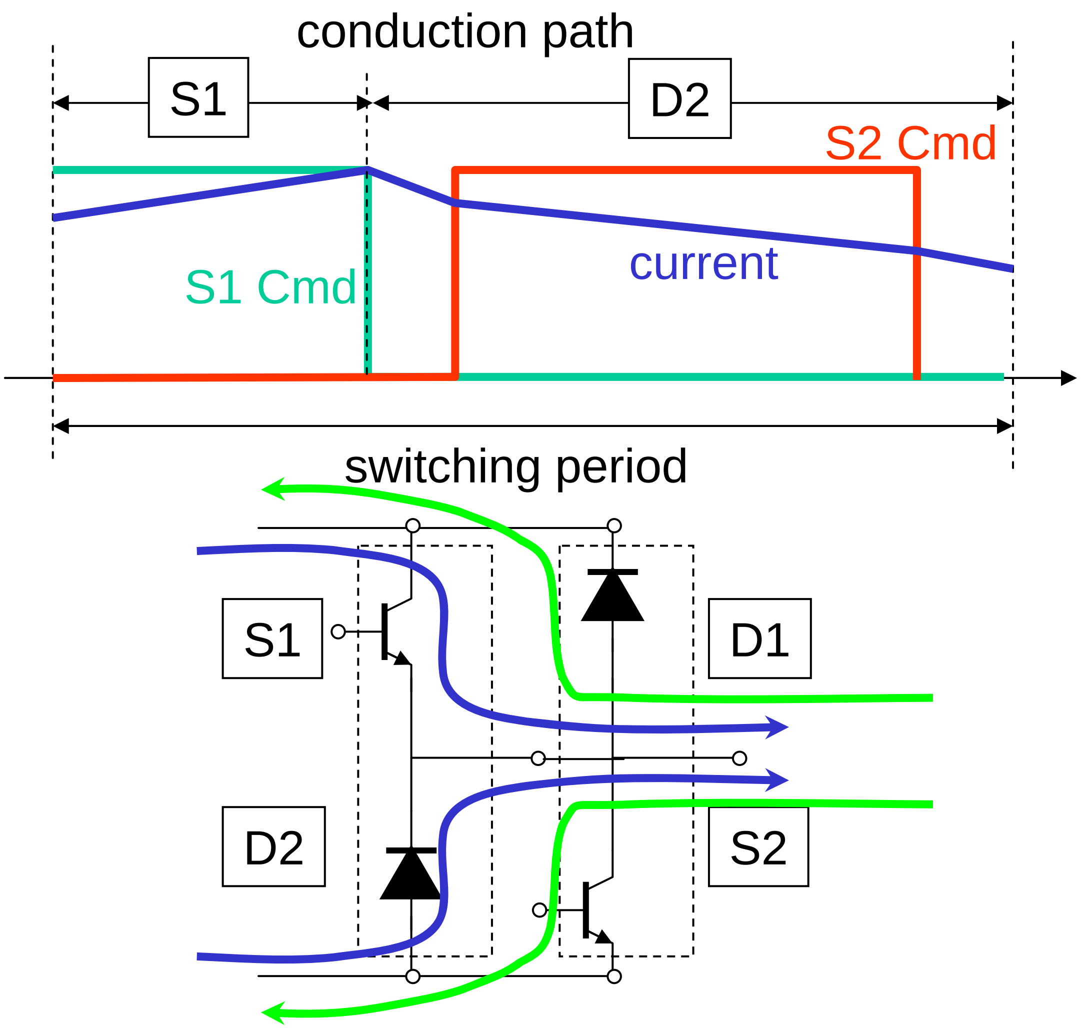
Diode Current 100A/div

IGBT Voltage 200V/div

Study
- System Performance
- Transients
- Tradeoffs (L, C, f_{sw})

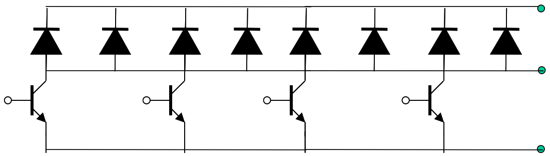
~50%
sw. loss
~25% total loss
~70% vol, wgt.

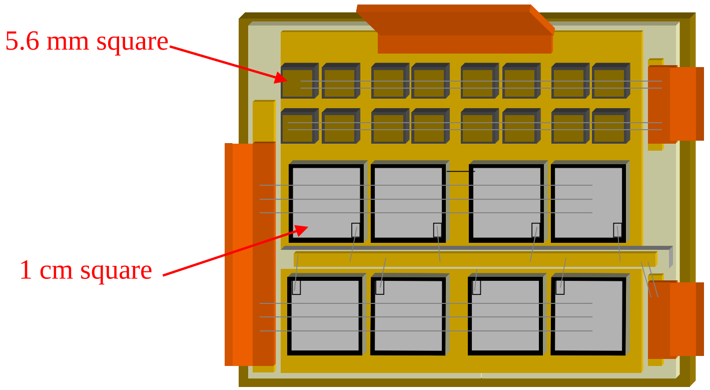
Rationale for Packaging IGBT with Forward Diode

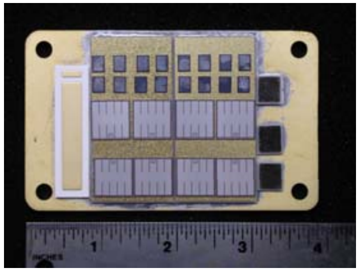


- Commutation is normally between the IGBT and forward current diode
  - Minimizing inductance in this commutation path reduces switching losses
  - Commutation between IGBT and flyback diode does not normally occur
- Packaging the forward diode with its IGBT instead of the flyback diode therefore can produce a more efficient, faster switching bridge
- Full phase leg also option

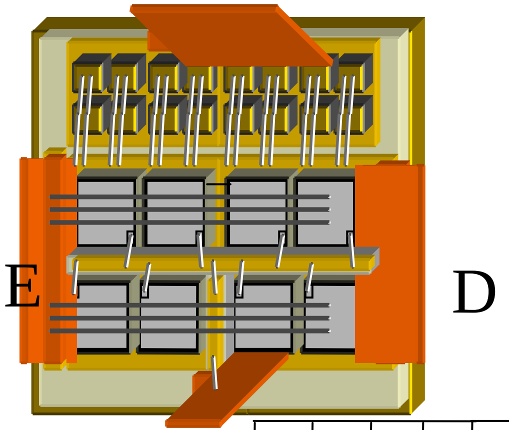
Conceptual Layout

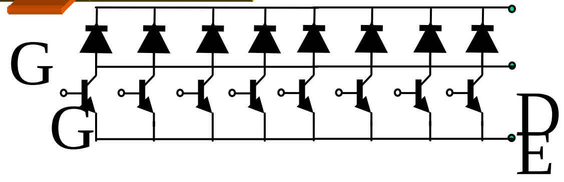






7.5 square inches (x2) Contrast this with the 25 square inches

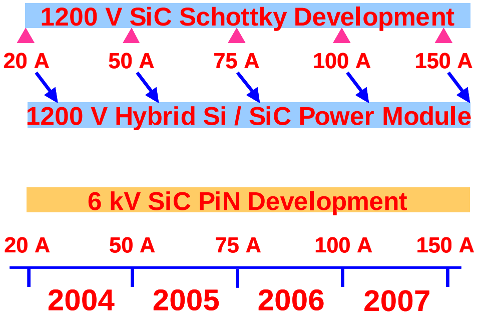




Layer #	Layer Thick	Material	Lambda	Theta	Temp
1	5	Silicon	1.092	0.016	117.8
2	1	Eutectic (Au-Sn)	1.528	0.002	105.8
3	10	Copper	3.952	0.008	104.1
4	10	Aluminum Nitride	1.521	0.019	98.1
5	100	AlSiC HOPG	2.250	0.079	84.0
6		Isotherm			25.0

Ongoing Cree Developments

Road Map - Hybrid Si/SiC Power Module



1200 V SiC Schottky Development

20 A 50 A 75 A 100 A 150 A

1200 V Hybrid Si / SiC Power Module

6 kV SiC PiN Development

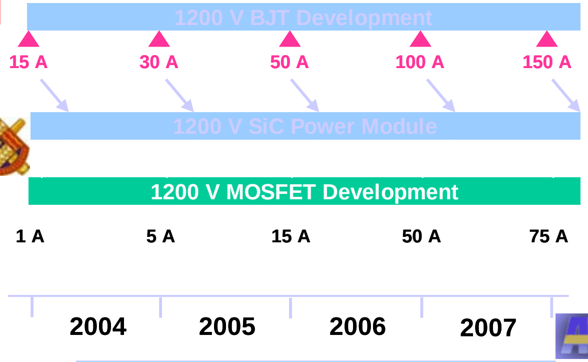
20 A 50 A 75 A 100 A 150 A

2004 2005 2006 2007

1200 V / 50 A SiC MOSFETs and Schottky Diodes

- **200°C Operation**
- **100 kHz Operation**
- **Reduction in size of passives**
- **4x reduction in cooling**

Road Map-All SiC Power Module



1200 V BJT Development

15 A 30 A 50 A 100 A 150 A

1200 V SiC Power Module

1200 V MOSFET Development

1 A 5 A 15 A 50 A 75 A

2004 2005 2006 2007

1200 V / 50 A SiC BJTs and PiN Diodes

- **300°C Operation**
- **100 kHz Operation**
- **Reduction in size of passives**
- **8x reduction in cooling**

- SiC material improved to allow large area devices to be demonstrated
- 1200 V, 150 A Schottkys, PiNs, and BJTs on pace for 2007
- 1200 V, 75 A MOSFETs on pace for 2007
- 1200 V, 600 A all SiC modules can be built by 2007 for electric drives

Some Cost Considerations

Assume: SiC will reach 3x Si, diode is ½ of active, LC product goes down by 4, choose L or C

	Today's Si Design	Hybrid Si/SiC-1	Hybrid Si/SiC-2
Semiconductors	4.11	6.81	6.81
Magnetics	9.83	4.91	2.455
Filter Caps	1.7	0.85	1.7
Heatsinks + Hardware	2.4	1.2	1.2
Fans	1	1	1
Sum (% of total parts cost)	19.04	14.77	13.165

Percentage Costs for Si/SiC Inverter

1% increase, 2% improvement round-trip efficiency

For the 100kW Inverter, feeding a 200kWHr battery, once per day charging cycle 2kWHr saving of off-peak energy, 2KWHr of peak electrical energy.

German feed in tariff for PV as an indicator (~55 c€/kWh) we could argue that the 1% of efficiency is worth US $1/day, or with a 20% return on investment approximately $1,800

on the order of 10% of the parts cost of the inverter and so the increase in cost of the semiconductors in moving to a hybrid Si/SiC IGBT module is easily justified in savings due to improved efficiency

Or CEC have put a monetary value on KW capability of up to $3.50/watt and so the 1% efficiency improvement would have a direct monetary value in a subsidy situation of up to $3,500. Could be more for roundtrip and with 2 stage

Other factors: EMI, Snubbers, metal, MOVs, Electrolytics!, …

Again -- Systems Approach is Critical

	APPROACH	IMPACT
1	SiC power devices	Higher frequency, higher temperature, lower loss
2	High frequency enables minimization of filter capacitors, Bulk Capacitors, and filter inductors	Reliable and robust Low line harmonics and current ripple Reduction of common mode
3	Dead-Beat Control	Faster rectifier and inverter response
4	Feed-Forward control from load and line	Minimize storage and response times
5	Wide frequency range	Non-linear control techniques, faster control
6	CSI (Current Sourced Inverter0	More Compatible with Normally-On devices

Other Critical Issues for Full SiC System

- Passives
- Packaging
  - Heat Removal
  - CTE
  - Metallization
  - Electromigration
- Gate Drives
  - Bipolar
  - Adaptive
- Controls
  - Nonlinear
- Signal Electronics
  - High Temperature

T, ΔT, dT/dt --Dominant Causes of Power Module Failure

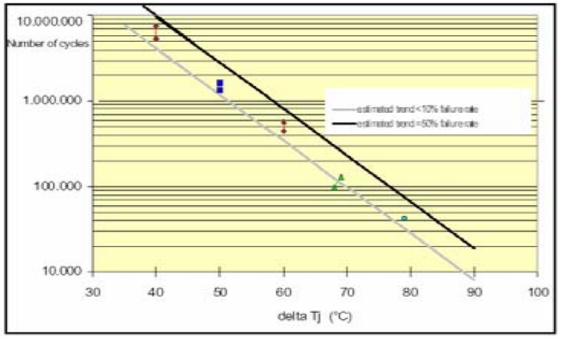
- Die attach to DBC Ceramic (bimorph failure due to CTE mismatch → fatigue)
- Wirebonds (delaminate)
- Interface between Ceramic and Baseplate

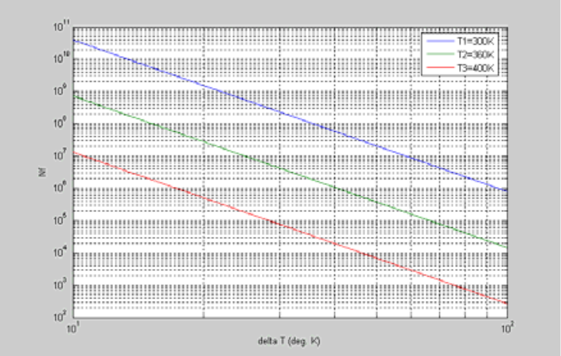
The cycles to failure (N_f) has a relationship to T and ΔT that is approximately

$$N_f = \frac{10^{24} \cdot (0.9354)^{T_{abs}}}{(\Delta T_{abs})^{4.696}}$$

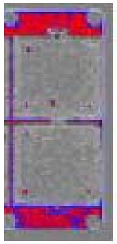
Exponential function of ΔT and dimensions

→limits die size →need to parallel





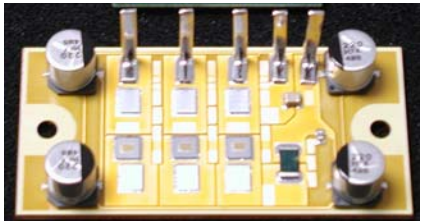
4000 cycles (Cu)



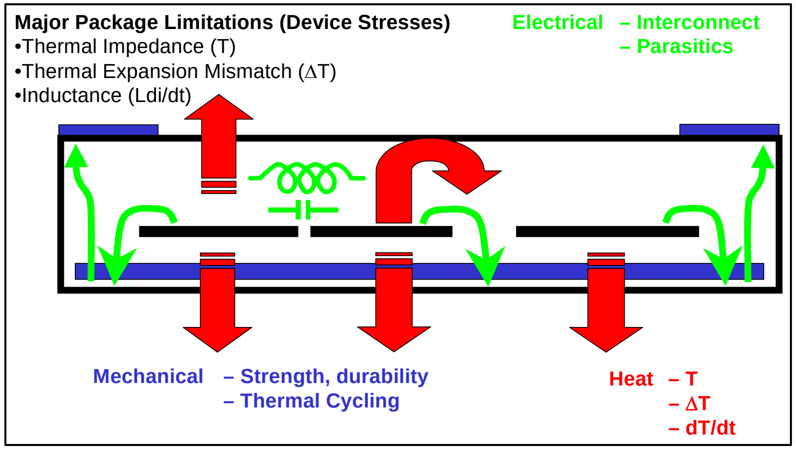
(AlSiC)

Conventional Packaging

- Insulated Metal Substrates (IMS)
  - Good Thermal performance
  - Low Cost $\$3/\text{in}^2$
  - Large CTE Mismatch



- Direct Bonded Copper (DBC)
  - Better CTE matching
  - Good Thermal performance
  - Medium Cost $\$10/\text{in}^2$

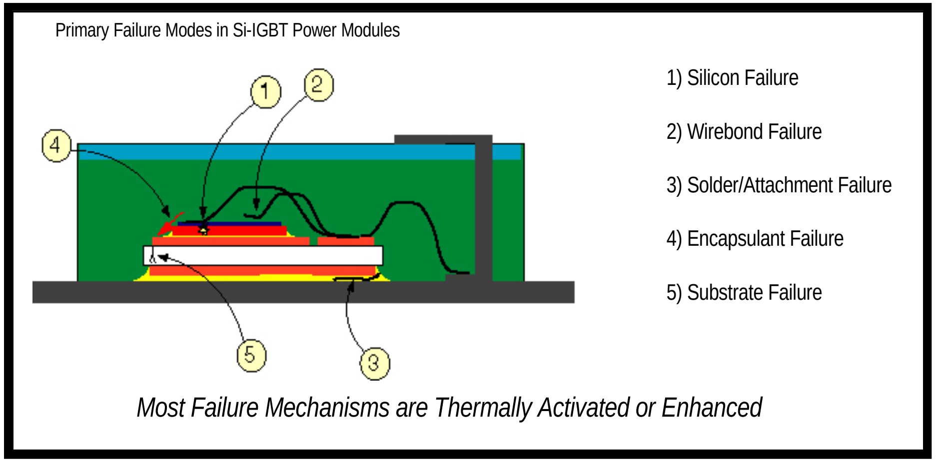


Major Package Limitations (Device Stresses)
•Thermal Impedance (T)
•Thermal Expansion Mismatch (ΔT)
•Inductance (Ldi/dt)

Electrical **– Interconnect**
– Parasitics

Mechanical **– Strength, durability**
– Thermal Cycling

Heat **– T**
– ΔT
– dT/dt



Primary Failure Modes in Si-IGBT Power Modules

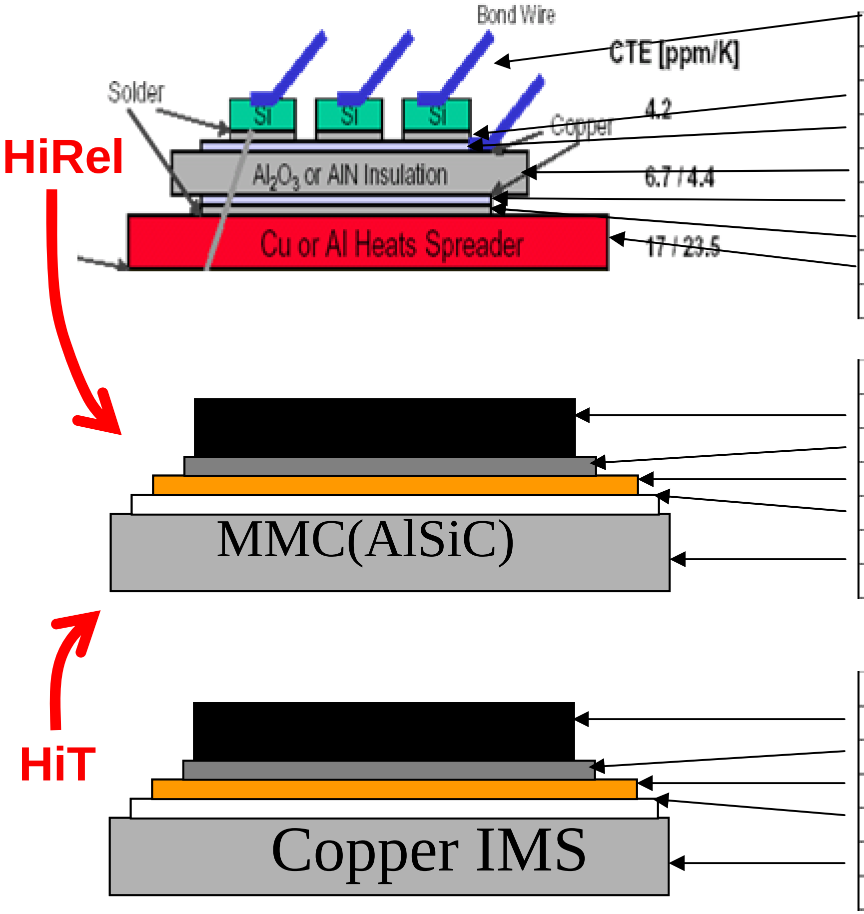
1) Silicon Failure
2) Wirebond Failure
3) Solder/Attachment Failure
4) Encapsulant Failure
5) Substrate Failure

Most Failure Mechanisms are Thermally Activated or Enhanced

ISSUES

- Devices, physics and characteristics
- Metallization
- Inter-Metallics
- Creep
- Thermal Design
- Mechanical Design
- Circuits, power and control
- Electro-migration
- Solid State Diffusion
- Composites
- Thermal Mechanics
- Materials

DBC/CuMo vs MMC(AlSiC) vs Cu IMS



Layer #	Layer Thick	Material	Lambda	Theta	Temp
1	5	Silicon	1.006	0.017	143.8
2	2	Eutectic (Au-Sn)	0.772	0.009	130.7
3	10	Copper	3.935	0.008	124.2
4	20	Aluminum Nitride	1.497	0.036	118.2
5	10	Copper	3.960	0.006	91.4
6	2	Eutectic (Au-Sn)	0.772	0.006	87.0
7	100	CuMo 15-20% Mo	1.900	0.077	82.8
8		Isotherm			25.0

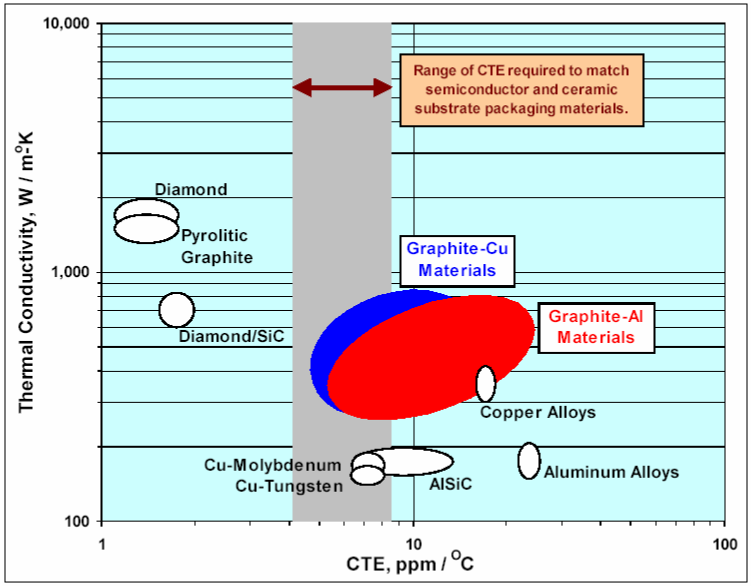
Layer #	Layer Thick	Material	Lambda	Theta	Temp
1	5	Silicon	1.092	0.016	117.8
2	1	Eutectic (Au-Sn)	1.528	0.002	105.8
3	10	Copper	3.952	0.008	104.1
4	10	Aluminum Nitride	1.521	0.019	98.1
5	100	AlSiC HOPG	2.250	0.079	84.0
6		Isotherm			25.0

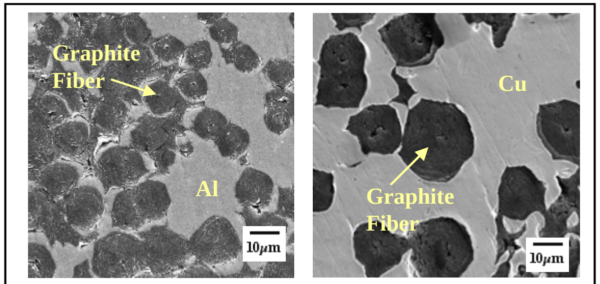
Layer #	Layer Thick	Material	Lambda	Theta	Temp
1	5	Silicon	1.129	0.016	107.9
2	2	Lead-tin (Sn62)	0.524	0.013	96.2
3	10	Copper	3.965	0.008	86.6
4	3	Alumina	0.317	0.028	80.7
5	100	Copper	4.010	0.047	59.9
6		Isotherm			25.0

MMC (AlSiC) retains 5 layer High Conductivity stackup but adds high rel TCE matching

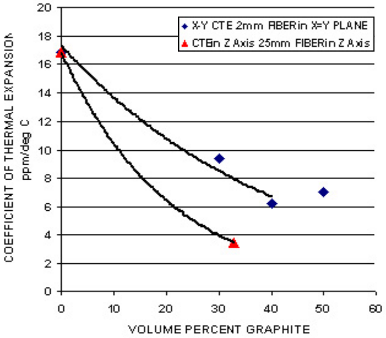
ΔT -- CTE Matching

- High Power Reliability demands good λ
- High Thermal Conductivity is not the only concern….
- Also need to optimize/match CTEs
- Metal alloys involve compromise (Kovar, Cu-Moly,)
- MMCs emerging, AlSiC, (Graphite, -ve CTE)





a) SEM of SAMPLE Al-1: Graphite & Al b) SEM of SAMPLE Cu-1: Graphite & Cu



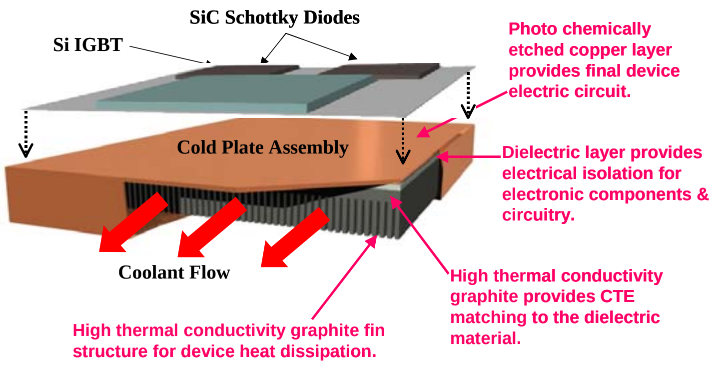


Photo chemically etched copper layer provides final device electric circuit.

Dielectric layer provides electrical isolation for electronic components & circuitry.

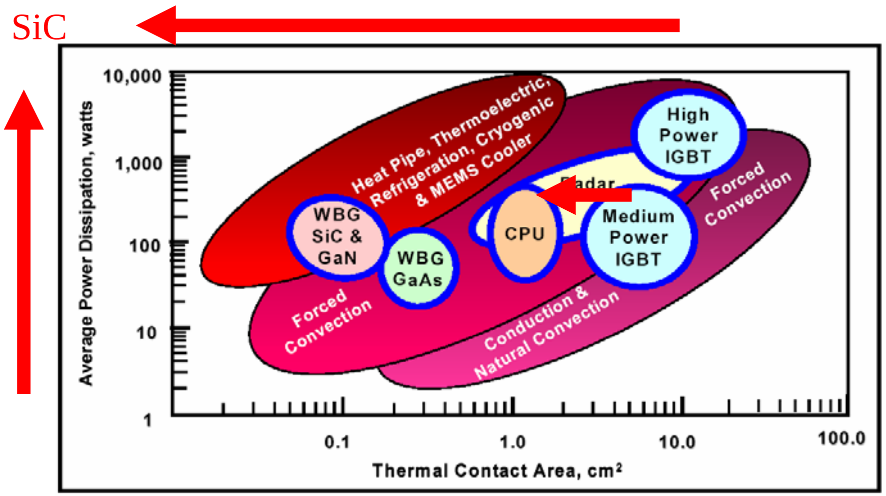
High thermal conductivity graphite provides CTE matching to the dielectric material.

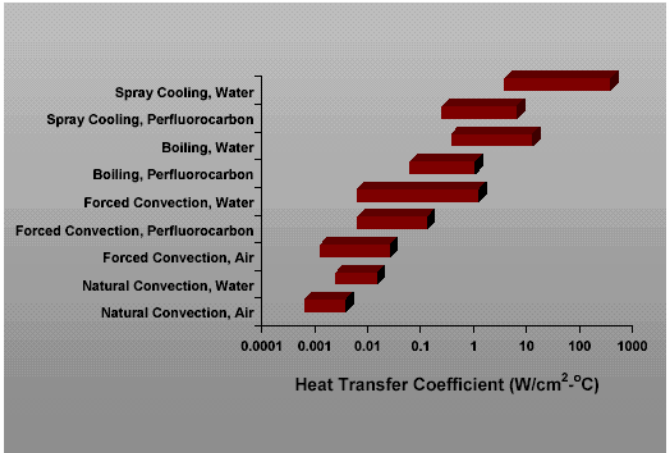
High thermal conductivity graphite fin structure for device heat dissipation.

Summary of Hi-T Packaging Approaches

- Minimization of number/types of materials
- Use of materials stable at high temperatures
- Near-perfect matching of thermal expansions, including metal conductor layers
- Use of multiple parallel die to minimize interface stresses, relative to single large die
- Complete elimination of bond wires through use of bump-bonding (flip-chip), compression packaging and other advanced techniques.

Is Heat Transfer Technology Adequate for SiC ?





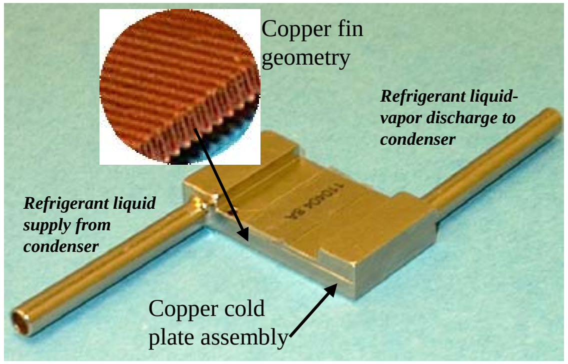
SiC Technology

- Smaller areas
- Comparable (?) Power Dissipation
- Overall higher heat flux density
- Want to take advantage of hi-T

- Typically
    - $100 A/cm^2 \rightarrow 500 A/cm^2$
    - $100 W/cm^2 \rightarrow 500 W/cm^2$

2 Stage Cooling/2ϕ

- **Heat must go to ambient**
- **Power buys Reliability (ΔT)**
- **Vol, Wgt, determines Rejection (7X for passive vs active)**
- **CoP of 50+ for liquid (2ϕ)**



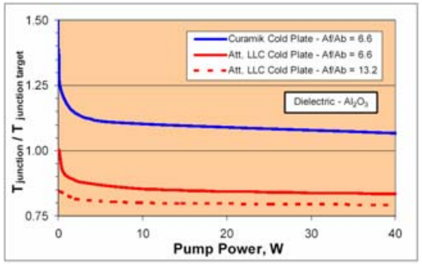
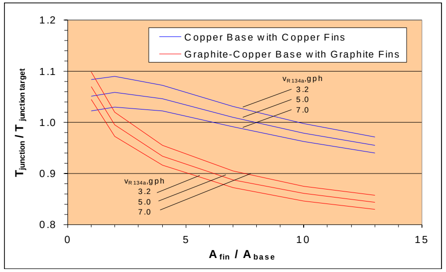
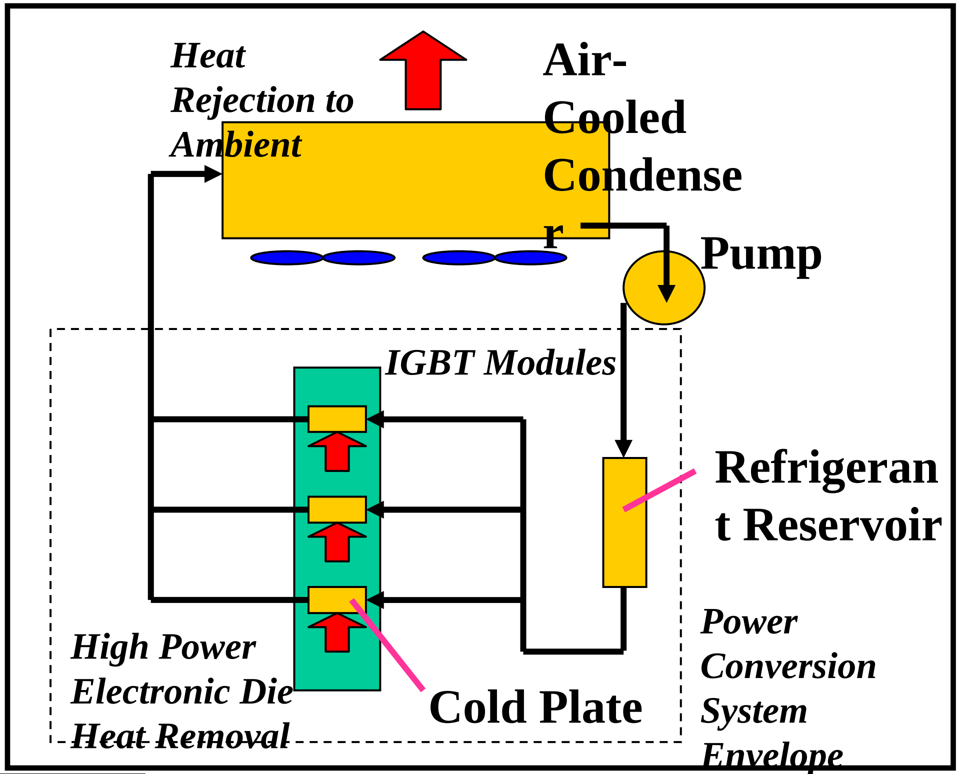


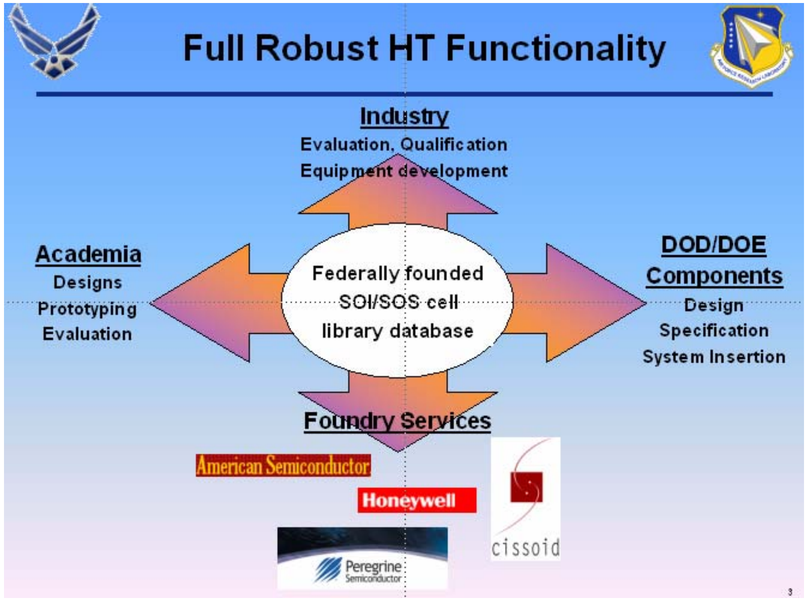
Figure 12 – Junction Temperature versus Pumping Power for SiC IGBT Operating at 1,000 W/cm^2





- **500—1000W/cm2 CuC design**

High T Electronics



Full Robust HT Functionality

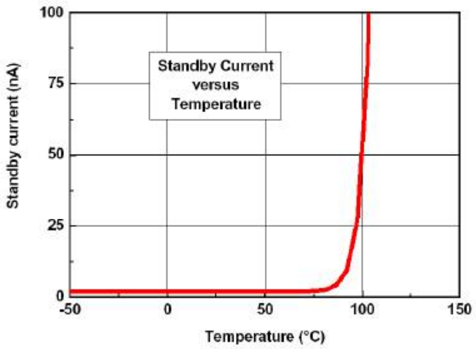
Industry
Evaluation, Qualification
Equipment development

Academia
Designs
Prototyping
Evaluation

Federally founded
SOI/SOS cell
library database

DOD/DOE Components
Design
Specification
System Insertion

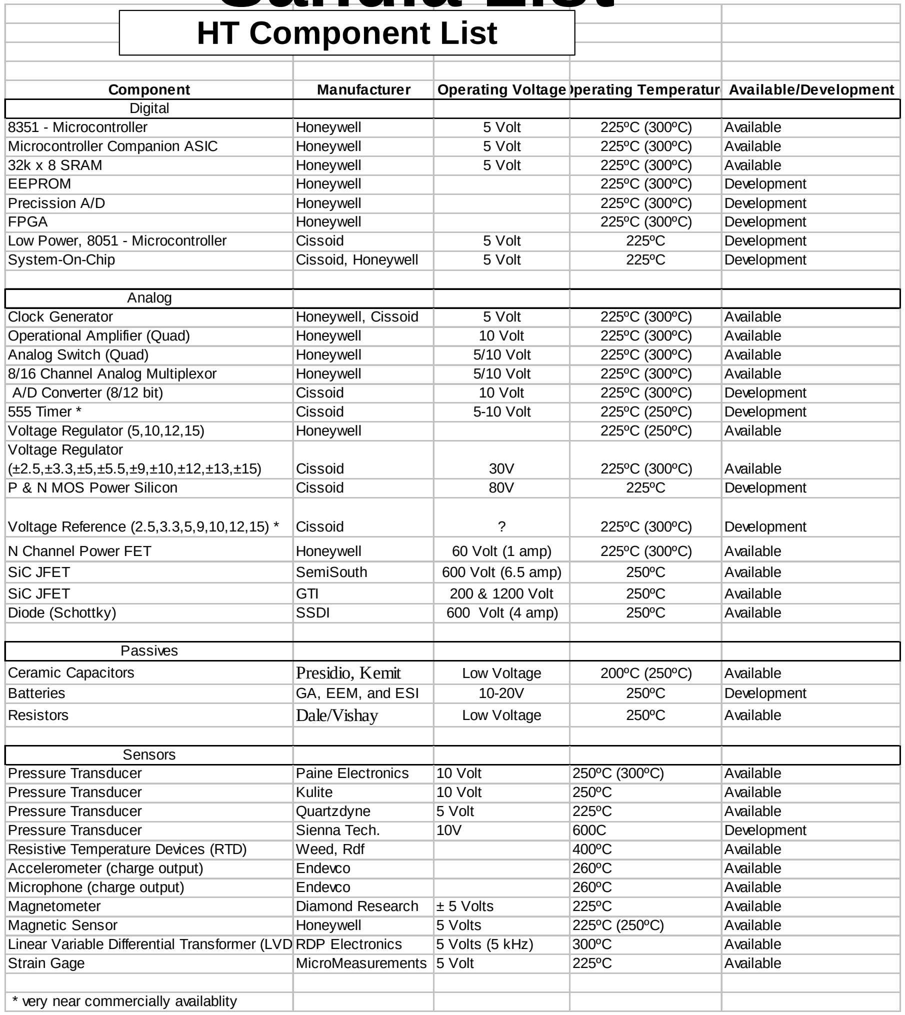
Foundry Services



- •No SSD in Si (500°C+)
- •Leakage is problem
- •Exponential, hard limit
- •Thermal Runaway in bulk devices
- •PD and FD SOI proven at High T
  - •Commercial
  - •Deeptrek program
- •Other problems
  - •Electromigration
    - •Low density
    - •Cu

High T,f Components

Sandia List



HT Component List

Component	Manufacturer	Operating Voltage	Operating Temperatur	Available/Development
Digital				
8351 - Microcontroller	Honeywell	5 Volt	225ºC (300ºC)	Available
Microcontroller Companion ASIC	Honeywell	5 Volt	225ºC (300ºC)	Available
32k x 8 SRAM	Honeywell	5 Volt	225ºC (300ºC)	Available
EEPROM	Honeywell		225ºC (300ºC)	Development
Precission A/D	Honeywell		225ºC (300ºC)	Development
FPGA	Honeywell		225ºC (300ºC)	Development
Low Power, 8051 - Microcontroller	Cissoid	5 Volt	225ºC	Development
System-On-Chip	Cissoid, Honeywell	5 Volt	225ºC	Development
Analog				
Clock Generator	Honeywell, Cissoid	5 Volt	225ºC (300ºC)	Available
Operational Amplifier (Quad)	Honeywell	10 Volt	225ºC (300ºC)	Available
Analog Switch (Quad)	Honeywell	5/10 Volt	225ºC (300ºC)	Available
8/16 Channel Analog Multiplexor	Honeywell	5/10 Volt	225ºC (300ºC)	Available
A/D Converter (8/12 bit)	Cissoid	10 Volt	225ºC (300ºC)	Development
555 Timer *	Cissoid	5-10 Volt	225ºC (250ºC)	Development
Voltage Regulator (5,10,12,15)	Honeywell		225ºC (250ºC)	Available
Voltage Regulator (±2.5,±3.3,±5,±5.5,±9,±10,±12,±13,±15)	Cissoid	30V	225ºC (300ºC)	Available
P & N MOS Power Silicon	Cissoid	80V	225ºC	Development
Voltage Reference (2.5,3.3,5,9,10,12,15) *	Cissoid	?	225ºC (300ºC)	Development
N Channel Power FET	Honeywell	60 Volt (1 amp)	225ºC (300ºC)	Available
SiC JFET	SemiSouth	600 Volt (6.5 amp)	250ºC	Available
SiC JFET	GTI	200 & 1200 Volt	250ºC	Available
Diode (Schottky)	SSDI	600 Volt (4 amp)	250ºC	Available
Passives				
Ceramic Capacitors	Presidio, Kemit	Low Voltage	200ºC (250ºC)	Available
Batteries	GA, EEM, and ESI	10-20V	250ºC	Development
Resistors	Dale/Vishay	Low Voltage	250ºC	Available
Sensors				
Pressure Transducer	Paine Electronics	10 Volt	250ºC (300ºC)	Available
Pressure Transducer	Kulite	10 Volt	250ºC	Available
Pressure Transducer	Quartzdyne	5 Volt	225ºC	Available
Pressure Transducer	Sienna Tech.	10V	600C	Development
Resistive Temperature Devices (RTD)	Weed, Rdf		400ºC	Available
Accelerometer (charge output)	Endevco		260ºC	Available
Microphone (charge output)	Endevco		260ºC	Available
Magnetometer	Diamond Research	± 5 Volts	225ºC	Available
Magnetic Sensor	Honeywell	5 Volts	225ºC (250ºC)	Available
Linear Variable Differential Transformer (LVD	RDP Electronics	5 Volts (5 kHz)	300ºC	Available
Strain Gage	MicroMeasurements	5 Volt	225ºC	Available
* very near commercially availablity				

Passives

- **Magnetics**
  - **100kHz limit for ferrites**
  - **Powdered iron**
  - **nanocrystalline**
- **Caps**
  - **FPE**
  - **Biaxial-oriented polypropylene**
  - **Metalized teflon**
  - **Antiferroelectric ceramic**

Summary/Conclusions

- Silicon Carbide technology is rapidly maturing
- Will impact all Power Conversion applications including grid connect electronics for energy storage
- Design and analysis of 100kW Inverter application
  - full SiC system at 30% of the volume and weight of today's systems or alternatively could save 80% of the conduction and switching loss in the same volume.
  - Similarly, hybrid Si/SiC technology available today can save approximately 30% of either the volume or weight or of the switching energy being dissipated (25%+ lower losses).
- This provides the designer with choices and trade-offs.
- The economics look reasonable once Silicon Carbide costs come down to some reasonable multiplier of Silicon.
- Inverter costing very interesting, all energy intensive raw materials are rising significantly in cost (have been).
- There are many further tasks and challenges to be addressed before full SiC power conversion systems become a reality.