“High Power Silicon Carbide Inverter Design -- 100kW Grid Connect Building Blocks ”

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Stan Atcitty of Sandia National Laboratories

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“High Power Silicon Carbide Inverter Design”

Overview

• Company
• Application
• SiC Technology – Potential, Status
• Devices
• Roadmap
• Design

Acknowledgements
SatCon Highlights
Technology … Applications … Products

Technology

Today
- 200 Employees
- 3 Divisions

2003 Subsidiary Corporations

InverPower
2001

FMI & HiComp
1998

WEC/NG
1999

BEACON
1997

Patriot -
1992

Magmотор
1997

1985 MIT-
DRAPER

Applications

High Bandwidth Controls
Packaging & Thermal Management
Electric Machines & Magnetics
Modular Power Electronics

SatCon Applied Technology
27 Drydock Ave, Boston, MA 02210
Motivation for Utility Scale Storage

- Increasing electrification, dominant secondary source of energy, Electricity is >1/3 of our 100 Quad Economy
- Grid is a BEAUTIFUL thing
  - Energy moves at the speed of light
  - Rugged Electro-mechanical generators
  - Spinning “reserve”
  - Excess capacity (>15% is critical) SIZED FOR 20%+
  - Low Impedance – typically 1% of rating at PCC
  - Fault clearance
  - Overload
  - ac – Simple Impedance Transformation, and Isolation
- Beautiful – but complex, congested
  - Distributed network with no significant energy storage
  - Supply must equal demand
  - Load transients (generator power angle)
  - System stability problems (minimal local control), tap-changing, relaying, v and f droop
  - Time constraints of protective devices
- Importance of storage to address
  - Distribution (remoteness of generation and utilization)
  - Load leveling (excess capacity), energy arbitrage
  - Power Quality
  - Intermittent Renewables

100 Quads = 100 exajoule (100.10^{18} J)

Electricity Infrastructure

<table>
<thead>
<tr>
<th>Category</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission SCADA control points</td>
<td>12</td>
</tr>
<tr>
<td>FERC grid monitor/control</td>
<td></td>
</tr>
<tr>
<td>Network Reliability Coordinating Centers</td>
<td>20</td>
</tr>
<tr>
<td>Regional Transmission Control Centers</td>
<td>130</td>
</tr>
<tr>
<td>Utility control centers</td>
<td>&gt;300</td>
</tr>
<tr>
<td>Power plants</td>
<td>10,500</td>
</tr>
<tr>
<td>Large (&gt;500 MW)</td>
<td>500</td>
</tr>
<tr>
<td>Small (&lt;500 MW)</td>
<td>10,000</td>
</tr>
<tr>
<td>Transmission Lines</td>
<td>680,000 miles</td>
</tr>
<tr>
<td>Transmission substations</td>
<td>7,000</td>
</tr>
<tr>
<td>Local distribution lines</td>
<td>2.5 million miles</td>
</tr>
<tr>
<td>Local distribution substations</td>
<td>100,000</td>
</tr>
</tbody>
</table>
Some Potential SiC (WBG) Impacts on Grid

- **Relaying** (electromechanical is 6-10 cycle, solid-state for LV, MV, HV)
  - Isolation (SSR)
  - Protection
  - Fault clearing
  - Fault limiting (SSCL)
- **Transmission Electronics** (MV, HV)
  - FACTS
  - VARS, (SVAR, DVAR)
  - DVR
  - STS
- **Grid electronics** (storage, renewables, PQ)
  - Volume
  - Weight
  - Efficiency
  - Reliability
  - Cost
  - Overload capability
  - Voltage/Power Application Range
- **Solid State Suppression**
  - Spikes
- **Solid State Transformers** (HF Link)

New Switch Capabilities enables new Applications
Hi-T, Hi Rad, Hi V, Hi f
Application -- Modular SiC
Grid Connected Inverter

- modular 100 kW DC-AC inverters (800 VDC/480 Vac 3 phase)
- modern computer controls with both PLC and industrial computer with dual redundant LAN interface
- Expandable to 3MW
- SSIMs are hot swappable (electrical and mechanical)
- Power electronics in each SSIM are cooled by a sealed water-cooled cold plate
- Modular building block → volume → more cost effective application of SiC

5.7 kHz PWM hard switched, 1 pu, 100kW, 480V, 120Arms
Approx 19” W x 8” H x 35” L, 375 lbs. Output LC filter, Input L EMI filter.
Liquid cooled IGBT power stage, gated drive PWAs, and bulk capacitors.
DC Input, 800V nominal, 1200V Pk

Used today in DD(X)
Power Electronic Systems

- Power Circuits
- Power Components, active and passive
- Signal Electronics
- Control
- Software
- Thermal Management
- Mechanical Design & Packaging

Full benefit comes from addressing all areas.

SiC devices are NOT drop in replacements.

Is the performance acceptable?
Are the devices reliable?
Are they consistent (matched)?
What are the next hurdles?
Beyond Silicon, Why? (other than temperature or radiation niches)

• **Ideally** in Power Conversion we use switching elements to move energy in discrete packets between source and load, with reactive elements for the energy storage and filtering, but …
  
  • Voltage Rating  
  • Current Rating  
  • Temperature Rating  
  • Radiation limitation  
  • Parasitics, R, C, switching time, $R_{TH}$, $V_{ON}$  
  • Fundamental limitations of Switching speed  
  • $$$ total cost  

<table>
<thead>
<tr>
<th>Si SOA</th>
<th>MOSFET 1983, 1.2 μs $\rightarrow$ 2004, 0.1 μs</th>
<th>600V, 20A</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT 1986, 3 μs $\rightarrow$ 2004, 1.2 μs</td>
<td>6kV, 150A</td>
<td></td>
</tr>
</tbody>
</table>
# WBG Materials

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap $E_g$ (eV)</td>
<td>1.1</td>
<td>3.0</td>
<td>3.3</td>
<td>3.45</td>
<td>5.45</td>
</tr>
<tr>
<td>Dielectric Constant, $\varepsilon_r$</td>
<td>11.9</td>
<td>9.7</td>
<td>10.1</td>
<td>9</td>
<td>5.5</td>
</tr>
<tr>
<td>Breakdown Field, $E_c$ (kV/cm)</td>
<td>300</td>
<td>2500</td>
<td>2200</td>
<td>2000</td>
<td>10000</td>
</tr>
<tr>
<td>Electron mobility, $\mu_n$ (cm$^2$/V-s)</td>
<td>1500</td>
<td>500</td>
<td>1000</td>
<td>1250</td>
<td>2200-4500</td>
</tr>
<tr>
<td>Hole mobility, $\mu_p$ (cm$^2$/V-s)</td>
<td>600</td>
<td>101</td>
<td>115</td>
<td>250</td>
<td>1600-3000</td>
</tr>
<tr>
<td>Thermal Conductivity $\lambda$ (W/cm-K)</td>
<td>1.5</td>
<td>4.9</td>
<td>4.9</td>
<td>1.3</td>
<td>22</td>
</tr>
<tr>
<td>Thermal expansion ($\times 10^{-6}$)/ºK</td>
<td>2.6</td>
<td>3.8</td>
<td>4.2</td>
<td>5.6</td>
<td>1-2</td>
</tr>
<tr>
<td>Saturated e$^-$ Drift Velocity, $v_{sat}$ ($\times 10^7$ cm/s)</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2.2</td>
<td>2.7</td>
</tr>
</tbody>
</table>

- **Wide Band Gap**, high-T, high Rad, low leakage
- **High** $E_c$
- **Good** $\lambda$

**+ve Impact**
- Weight
- Volume
- Efficiency
- Ruggedness
E\textsubscript{c} – thickness, doping

- Voltage is area under curve
- Big E\textsubscript{c} → small W
- Small W → large N\textsubscript{D}

\[ W = \frac{2 \cdot V_{\text{MAX}}}{E_{\text{c}}} \quad W \approx \frac{1}{\sqrt{N_{\text{D}}}} \]

Materials → Benefits

- Order of magnitude higher breakdown field
- 100 times higher blocking layer dopant density  
  → 1/10\textsuperscript{th} blocking layer thickness
- 100 times faster for minority carrier device
- Larger band gap gives high temperature capability
- Significant improvement in thermal conductivity  
  → reduced heat sink requirements
- Improve failure mechanisms for fault conditions
- Higher power with future high temperature packages
Whats in the way?

- Materials Issues
  - 180+ Xtal structures (polytypes)
    - 6H, 15R, 4H and 3C, main candidates
  - No liquid phase, growth at 2200ºC+
    - Sublimation
    - CVD
  - Negligible Dopant diffusion, dope epi as it is grown or hi-energy implant at high-T
  - Defects
    - Micro-pipe
    - Screw dislocation
    - Basel plane defects
  - Oxide quality and reliability
  - Stability of Ohmic contacts
Optical Market driving SiC Wafer demand

- 4 inch wafers
- Substrates for GaN LEDs
  - Better thermal conductivity
  - Good electrical conductor
- Volume has driven quality

SiC Devices Developing: Example, MOSFETs

Curves are for production volumes.

Reduction in Cree’s Median Micropipe Density vs Time

*Spline fits to data are shown

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SiC Schottky

- First commercial SiC power device (other than RF)
- 2 sources, Cree & Infineon
- 10,20 A 600,1200V

SiC PiN Diode

SiC Schottky vs PiN Diode

- 20kV+ devices have been demonstrated

• 20kV devices have been demonstrated
SiC Bipolar

1200 V SiC BJTs

SiC JFET

Basic device cross-section

Finished JFET in a TO-251

Switching Test Circuit

$V_{DS} = 300$ V

$f = 20$ MHz

Normally-On : 7/2004

Normally Off –7/2004
SiC MOSFET

- Native oxide is SiO₂
- Only WBG with native oxide
- Grow in Silane Environment
- IGBT?

SiC GTOs

Forward I-V at 100 mA gate current

300 A @ 5.5 V

Turn-on time versus $I_{AK}$
Northrop – All SiC Cascode

All-SiC Cascode On-state Characteristics – 10 A Large Area Cascode

On-state characteristics only affected by reduction of mobility with temperature

NGC All-SiC Cascode vs. Commercially Available Si MOSFETs

<table>
<thead>
<tr>
<th>Device</th>
<th>Blocking Voltage (V)</th>
<th>Current Rating (A)</th>
<th>Rds, on (Ω)</th>
<th>Turn-on time, t_on (ns)</th>
<th>Integral Diode Recovery Time, t_di (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>All-SiC Cascode</em></td>
<td>1100</td>
<td>4</td>
<td>0.66</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td><em>Cool MOS™</em></td>
<td>800</td>
<td>4</td>
<td>1.3</td>
<td>15</td>
<td>520</td>
</tr>
<tr>
<td><em>HEXFET®</em></td>
<td>1000</td>
<td>4.3</td>
<td>3.5</td>
<td>33</td>
<td>710</td>
</tr>
</tbody>
</table>

*Taken at similar conditions to those listed in Si MOSFET data sheets
*Commercial MOSFET characteristics taken from data sheets
Ruggedness – Hi T

25us Si IGBT test

5ms SiC JFET test

- Better thermal conductivity
- Higher Temperature Material, Dopant Stability

“Available” SiC SOA Summary

<table>
<thead>
<tr>
<th>Device</th>
<th>Voltage (V)</th>
<th>Current (A)</th>
<th>Demonstrated Switching times</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schottky</td>
<td>600</td>
<td>100</td>
<td>∼ns</td>
</tr>
<tr>
<td></td>
<td>1200</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>PIN</td>
<td>20,000</td>
<td>20</td>
<td>∼10ns</td>
</tr>
<tr>
<td>Bipolar</td>
<td>1200</td>
<td>20</td>
<td>∼100ns, β ∼30</td>
</tr>
<tr>
<td>MOSFET</td>
<td>1200</td>
<td>10</td>
<td>∼100ns</td>
</tr>
<tr>
<td>JFET</td>
<td>10,000</td>
<td>1</td>
<td>∼100ns</td>
</tr>
<tr>
<td></td>
<td>1,200</td>
<td>20A</td>
<td></td>
</tr>
</tbody>
</table>

1% conduction loss at 0.67(V_PK)
Critical that Devices Parallel well

- JFETs ✓
- Bipolars ✓
- MOSFETs ✓

- Static
  - PTC
- Dynamic
  - Turn on
  - Turn off
- Need to be well matched
  - Over temperature
- Transitions critical

**All SiC 7.5 kW, 400V, BJT**
Switching Time – Loss -- Frequency

- Generally, \( (t_{\text{on}} + t_{\text{off}}) \) sets \( f_{\text{sw}} \), losses go approximately as \( V.I. (t_{\text{on}} + t_{\text{off}})/2 \)
- \( 1\mu s \rightarrow 10\text{kHz} \) for 1%
- \( 100\text{ns} \rightarrow 100\text{kHz} \) for 1%

- New Technology
  - Lower conduction and switching
  - Trade efficiency off vs. L, C
Full SiC Grid Interactive Inverter Design

<table>
<thead>
<tr>
<th></th>
<th>Silicon SOA</th>
<th>Full SiC Design</th>
</tr>
</thead>
</table>
| **Size/Density/Efficiency** | 10 -- 100 W/in³  
(16 W/in³ for module)                                                                | 50 -- 500 W/in³  
(80 W/in³ for module)  
(30% Vol., 20%P) |
| **Cooling**             | 80°C max. liquid or 25°C Air                                                                 | >100°C liquid or 40-50 °C Air |
| **Response Time**       | 10 ms for 5.6 kHz with V and I loops                                               | 50 µS for 100kHz with dead-beat control |
| **High Temperature Design** | Si limits entire system to < 110°C                                                 | Partial High-Temperature design then eventually complete High-Temperature design if needed (analog degradation) |
| **Overload Capability** | 100-500 ms                                                                   | 10+ seconds                                                                |
| **Robustness**          | 10-20,000 hr. MTBF                                                          | 50-100,000 hr. MTBF                                                        |
Today – losses, on, off, rectifier

- Losses are comparable, on, off, rect
- Schottky saves Rectifier
- Some associated turn-on
- FRED → SiC, ~39% saving in sw. loss
- Why are turn-on loss so high?
  - Slow transitions
  - Paralleling?
  - Due to diode?
- Experiment and Simulate with rapid Turn-off (commercial devices have integrated polysilicon Rs)
Interim Approach

Hybrid Si IGBT/SiC Schottky Diodes

Can be done today

Si PiN Diodes
Replaced with SiC Schottky Diodes
Simulations – System and Device

Study
• System Performance
• Transients
• Tradeoffs (L, C, f_{sw})

~50% sw. loss
~25% total loss
~70% vol, wgt.
Rationale for Packaging IGBT with Forward Diode

- Commutation is normally between the IGBT and forward current diode
  - Minimizing inductance in this commutation path reduces switching losses
  - Commutation between IGBT and flyback diode does not normally occur
- Packaging the forward diode with its IGBT instead of the flyback diode therefore can produce a more efficient, faster switching bridge
- Full phase leg also option
Conceptual Layout

5.6 mm square

1 cm square

7.5 square inches (x2) Contrast this with the 25 square inches

<table>
<thead>
<tr>
<th>Layer #</th>
<th>Layer Thick</th>
<th>Material</th>
<th>Lambda</th>
<th>Theta</th>
<th>Temp</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5</td>
<td>Silicon</td>
<td>1.092</td>
<td>0.016</td>
<td>117.8</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>Eutectic (Au-Sn)</td>
<td>1.528</td>
<td>0.002</td>
<td>105.8</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>Copper</td>
<td>3.952</td>
<td>0.008</td>
<td>104.1</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>Aluminium Nitride</td>
<td>1.521</td>
<td>0.019</td>
<td>98.1</td>
</tr>
<tr>
<td>5</td>
<td>100</td>
<td>AISiC HOPG</td>
<td>2.250</td>
<td>0.079</td>
<td>84.0</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>kohem</td>
<td></td>
<td></td>
<td>25.0</td>
</tr>
</tbody>
</table>
Ongoing Cree Developments

Road Map - Hybrid Si/SiC Power Module

- 200 V SiC Schottky Development
- 20 A, 50 A, 75 A, 100 A, 150 A
- 1200 V Hybrid Si / SiC Power Module

Road Map - All SiC Power Module

- 1200 V SiC MOSFET Development
- 20 A, 50 A, 75 A, 100 A, 150 A
- 200°C Operation
- 100 kHz Operation
- Reduction in size of passives
- 4x reduction in cooling

- SiC material improved to allow large area devices to be demonstrated
- 1200 V, 150 A Schottkys, PiNs, and BJTs on pace for 2007
- 1200 V, 75 A MOSFETs on pace for 2007
- 1200 V, 600 A all SiC modules can be built by 2007 for electric drives
Some Cost Considerations

Assume: SiC will reach 3x Si, diode is ½ of active, LC product goes down by 4, choose L or C

<table>
<thead>
<tr>
<th></th>
<th>Today’s Si Design</th>
<th>Hybrid Si/SiC-1</th>
<th>Hybrid Si/SiC-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductors</td>
<td>4.11</td>
<td>6.81</td>
<td>6.81</td>
</tr>
<tr>
<td>Magnetics</td>
<td>9.83</td>
<td>4.91</td>
<td>2.455</td>
</tr>
<tr>
<td>Filter Caps</td>
<td>1.7</td>
<td>0.85</td>
<td>1.7</td>
</tr>
<tr>
<td>Heatsinks + Hardware</td>
<td>2.4</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Fans</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Sum (% of total parts cost)</td>
<td>19.04</td>
<td>14.77</td>
<td>13.165</td>
</tr>
</tbody>
</table>

Percentage Costs for Si/SiC Inverter

1% increase, 2% improvement round-trip efficiency
For the 100kW Inverter, feeding a 200kWhr battery, once per day charging cycle 2kWhr saving of off-peak energy, 2kWhr of peak electrical energy.
German feed in tariff for PV as an indicator (~55 c€/kWh) we could argue that the 1% of efficiency is worth US $1/day, or with a 20% return on investment approximately $1,800
on the order of 10% of the parts cost of the inverter and so the increase in cost of the semiconductors in moving to a hybrid Si/SiC IGBT module is easily justified in savings due to improved efficiency
Or CEC have put a monetary value on KW capability of up to $3.50/watt and so the 1% efficiency improvement would have a direct monetary value in a subsidy situation of up to $3,500. Could be more for roundtrip and with 2 stage

Other factors: EMI, Snubbers, metal, MOVs, Electrolytics!, …
## Again -- Systems Approach is Critical

<table>
<thead>
<tr>
<th>APPROACH</th>
<th>IMPACT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 SiC power devices</td>
<td>Higher frequency, higher temperature, lower loss</td>
</tr>
<tr>
<td>2 High frequency enables minimization of filter capacitors, Bulk Capacitors, and filter inductors</td>
<td>Reliable and robust Low line harmonics and current ripple Reduction of common mode</td>
</tr>
<tr>
<td>3 Dead-Beat Control</td>
<td>Faster rectifier and inverter response</td>
</tr>
<tr>
<td>4 Feed-Forward control from load and line</td>
<td>Minimize storage and response times</td>
</tr>
<tr>
<td>5 Wide frequency range</td>
<td>Non-linear control techniques, faster control</td>
</tr>
<tr>
<td>6 CSI (Current Sourced Inverter0)</td>
<td>More Compatible with Normally-On devices</td>
</tr>
</tbody>
</table>
Other Critical Issues for Full SiC System

- Passives
- Packaging
  - Heat Removal
  - CTE
  - Metallization
  - Electromigration
- Gate Drives
  - Bipolar
  - Adaptive
- Controls
  - Nonlinear
- Signal Electronics
  - High Temperature
T, ΔT, dT/dt -- Dominant Causes of Power Module Failure

- Die attach to DBC Ceramic (bimorph failure due to CTE mismatch → fatigue)
- Wirebonds (delaminate)
- Interface between Ceramic and Baseplate

The cycles to failure ($N_f$) has a relationship to $T$ and $ΔT$ that is approximately an exponential function of $ΔT$ and dimensions:

$$N_f = \frac{10^{24} \cdot (0.9354)^{T_{abs}}}{(ΔT_{abs})^{4.696}}$$

Exponential function of $ΔT$ and dimensions → limits die size → need to parallel
Conventional Packaging

- Insulated Metal Substrates (IMS)
  - Good Thermal performance
  - Low Cost $3/in²
  - Large CTE Mismatch

- Direct Bonded Copper (DBC)
  - Better CTE matching
  - Good Thermal performance
  - Medium Cost $10/in²

ISSUES

- Devices, physics and characteristics
- Metallization
- Inter-Metallics
- Creep
- Thermal Design
- Mechanical Design

- Circuits, power and control
- Electro-migration
- Solid State Diffusion
- Composites
- Thermal Mechanics
- Materials

Major Package Limitations (Device Stresses)
- Thermal Impedance (T)
- Thermal Expansion Mismatch (ΔT)
- Inductance (Ldi/dt)

Electrical – Interconnect
- Parasitics

Mechanical – Strength, durability
- Thermal Cycling

Heat – T
- ΔT
- dT/dt

Primary Failure Modes in Si-IGBT Power Modules

1) Silicon Failure
2) Wirebond Failure
3) Solder/Attachment Failure
4) Encapsulant Failure
5) Substrate Failure

Most Failure Mechanisms are Thermally Activated or Enhanced
DBC/CuMo vs MMC(AlSiC) vs Cu IMS

MMC (AlSiC) retains 5 layer High Conductivity stackup but adds high rel TCE matching.

---

Layer | Layer Thick | Material     | Lambda | Theta | Temp
--- |------------|--------------|--------|-------|------
1    | 5          | Silicon      | 1.006  | 0.017 | 143.8
2    | 2          | Eutectic (Au-Sn) | 0.772  | 0.009 | 130.7
3    | 10         | Copper       | 3.935  | 0.008 | 124.2
4    | 20         | Aluminum Nitride | 1.497  | 0.036 | 118.2
5    | 10         | Copper       | 3.960  | 0.006 | 91.4
6    | 2          | Eutectic (Au-Sn) | 0.772  | 0.006 | 87.0
7    | 100        | CuMo 15-20% Mo | 1.900  | 0.077 | 82.8
8    |             | Isotherm     |        |       | 25.0

Layer | Layer Thick | Material     | Lambda | Theta | Temp
--- |------------|--------------|--------|-------|------
1    | 5          | Silicon      | 1.092  | 0.016 | 117.8
2    | 1          | Eutectic (Au-Sn) | 1.528  | 0.002 | 105.8
3    | 10         | Copper       | 3.952  | 0.008 | 104.1
4    | 10         | Aluminum Nitride | 1.521  | 0.019 | 98.1
5    | 100        | AlSiC HOPG   | 2.250  | 0.079 | 84.0
6    |             | Isotherm     |        |       | 25.0

Layer | Layer Thick | Material     | Lambda | Theta | Temp
--- |------------|--------------|--------|-------|------
1    | 5          | Silicon      | 1.129  | 0.016 | 107.9
2    | 2          | Lead-tin (Sn62) | 0.524  | 0.013 | 96.2
3    | 10         | Copper       | 3.965  | 0.008 | 86.6
4    | 3          | Alumina      | 0.317  | 0.028 | 80.7
5    | 100        | Copper       | 4.010  | 0.047 | 59.9
6    |             | Isotherm     |        |       | 25.0
\[ \Delta T -- \text{CTE Matching} \]

- High Power Reliability demands good $\lambda$
- High Thermal Conductivity is not the only concern….
- Also need to optimize/match CTEs
- Metal alloys involve compromise (Kovar, Cu-Moly, )
- MMCs emerging, AlSiC, (Graphite, -ve CTE)
Summary of Hi-T Packaging Approaches

- Minimization of number/types of materials
- Use of materials stable at high temperatures
- Near-perfect matching of thermal expansions, including metal conductor layers
- Use of multiple parallel die to minimize interface stresses, relative to single large die
- Complete elimination of bond wires through use of bump-bonding (flip-chip), compression packaging and other advanced techniques.
SiC Technology
- Smaller areas
- Comparable (?) Power Dissipation
- Overall higher heat flux density
- Want to take advantage of hi-T

Typically
- 100A/cm² → 500A/cm²
- 100W/cm² → 500W/cm²
2 Stage Cooling/2φ

- Heat must go to ambient
- Power buys Reliability ($\Delta T$)
- Vol, Wgt, determines Rejection (7X for passive vs active)
- CoP of 50+ for liquid (2φ)

![Diagram of 2 Stage Cooling/2φ system]

- Refrigerant liquid supply from condenser
- Copper cold plate assembly
- Copper fin geometry
- Refrigerant liquid-vapor discharge to condenser

![Graph showing Junction Temperature versus Pumping Power for SiC IGBT Operating at 1,000 W/cm²]

- 500—1000W/cm² CuC design

SatCon Applied Technology
27 Drydock Ave, Boston, MA 02210
High T Electronics

- No SSD in Si (500°C+)
- Leakage is problem
- Exponential, hard limit
- Thermal Runaway in bulk devices
- PD and FD SOI proven at High T
  - Commercial
  - Deeptrek program
- Other problems
  - Electromigration
    - Low density
    - Cu
**Sandia List**

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer</th>
<th>Operating Voltage</th>
<th>Operating Temperature</th>
<th>Available/Development</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Digital</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8051 - Microcontroller</td>
<td>Honeywell</td>
<td>5 Volt</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>Microcontroller Companion ASIC</td>
<td>Honeywell</td>
<td>5 Volt</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>32k x 8 SRAM</td>
<td>Honeywell</td>
<td>5 Volt</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Honeywell</td>
<td></td>
<td>225ºC (300ºC)</td>
<td>Development</td>
</tr>
<tr>
<td>Precision A/D</td>
<td>Honeywell</td>
<td></td>
<td>225ºC (300ºC)</td>
<td>Development</td>
</tr>
<tr>
<td>FPGA</td>
<td>Honeywell</td>
<td></td>
<td>225ºC (300ºC)</td>
<td>Development</td>
</tr>
<tr>
<td>Low Power, 8051 - Microcontroller</td>
<td>Cissoid</td>
<td>5 Volt</td>
<td>225ºC (300ºC)</td>
<td>Development</td>
</tr>
<tr>
<td>System-On-Chip</td>
<td>Cissoid, Honeywell</td>
<td>5 Volt</td>
<td>225ºC (300ºC)</td>
<td>Development</td>
</tr>
<tr>
<td><strong>Analog</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock Generator</td>
<td>Honeywell, Cissoid</td>
<td>5 Volt</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>Operational Amplifier (Quad)</td>
<td>Honeywell</td>
<td>10 Volt</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>Analog Switch (Quad)</td>
<td>Honeywell</td>
<td>5/10 Volt</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>8/16 Channel Analog Multiplexer</td>
<td>Honeywell</td>
<td>5/10 Volt</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>A/D Converter (8/12 bit)</td>
<td>Cissoid</td>
<td>10 Volt</td>
<td>225ºC (300ºC)</td>
<td>Development</td>
</tr>
<tr>
<td>555 Timer *</td>
<td>Cissoid</td>
<td>5-10 Volt</td>
<td>225ºC (300ºC)</td>
<td>Development</td>
</tr>
<tr>
<td>Voltage Regulator (5, 10, 12, 15)</td>
<td>Honeywell</td>
<td></td>
<td>225ºC (250ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>Voltage Regulator</td>
<td>Cissoid</td>
<td>30V</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>Voltage Regulator (±2.5, ±3.3, ±5, ±6, ±10, ±12, ±13, ±15)</td>
<td>Cissoid</td>
<td>80V</td>
<td>225ºC (250ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>N &amp; P MOS Power Silicon</td>
<td>Cissoid</td>
<td></td>
<td>225ºC (250ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>Voltage Reference (2.5, 3, 5, 9, 10, 12, 15, 15)</td>
<td>Cissoid</td>
<td></td>
<td>225ºC (300ºC)</td>
<td>Development</td>
</tr>
<tr>
<td>N Channel Power FET</td>
<td>Honeywell</td>
<td>60 Volt (1 amp)</td>
<td>225ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td><strong>Passives</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ceramic Capacitors</td>
<td>ProTek, Kenet Ultra Low Voltage</td>
<td>200ºC (250ºC)</td>
<td>Available</td>
<td></td>
</tr>
<tr>
<td>Batteries</td>
<td>GA, EEM, and ESI</td>
<td>10-20V</td>
<td>250ºC</td>
<td>Development</td>
</tr>
<tr>
<td>Resistors</td>
<td>DaleVis LLC</td>
<td>Low Voltage</td>
<td>250ºC</td>
<td>Available</td>
</tr>
<tr>
<td><strong>Sensors</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pressure Transducer</td>
<td>Flame Electronics</td>
<td>10 Volt</td>
<td>250ºC (300ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>Pressure Transducer</td>
<td>Kulite</td>
<td>10 Volt</td>
<td>250ºC</td>
<td>Available</td>
</tr>
<tr>
<td>Pressure Transducer</td>
<td>Quartzyne</td>
<td>5 Volt</td>
<td>225ºC</td>
<td>Available</td>
</tr>
<tr>
<td>Pressure Transducer</td>
<td>Sienna Tech.</td>
<td>12V</td>
<td>600ºC</td>
<td>Development</td>
</tr>
<tr>
<td>Resilient Temperature Devices (RTD)</td>
<td>Weed, RAf</td>
<td></td>
<td>400ºC</td>
<td>Available</td>
</tr>
<tr>
<td>Accelerometer (charge output)</td>
<td>Endecoe</td>
<td></td>
<td>260ºC</td>
<td>Available</td>
</tr>
<tr>
<td>Microphone (charge output)</td>
<td>Endecoe</td>
<td></td>
<td>260ºC</td>
<td>Available</td>
</tr>
<tr>
<td>Magnetometer</td>
<td>Diamond Research</td>
<td>± 5 Volts</td>
<td>225ºC</td>
<td>Available</td>
</tr>
<tr>
<td>Magnetic Sensor</td>
<td>Honeywell</td>
<td>5 Volts</td>
<td>225ºC (250ºC)</td>
<td>Available</td>
</tr>
<tr>
<td>Linear Variable Differential Transformer (LVD)</td>
<td>RDP Electronics</td>
<td>5 Volts (5 kHz)</td>
<td>300ºC</td>
<td>Available</td>
</tr>
<tr>
<td>Strain Gage</td>
<td>MicroMeasurements</td>
<td>5 Volt</td>
<td>225ºC</td>
<td>Available</td>
</tr>
</tbody>
</table>

* very near commercially availability

- **Passives**
  - Magnetics
  - 100kHz limit for ferrites
  - Powdered iron
  - Nanocrystalline
- **Caps**
  - FPE
  - Biaxial-oriented polypropylene
  - Metalized teflon
  - Antiferroelectric ceramic
Summary/Conclusions

- Silicon Carbide technology is rapidly maturing
- Will impact all Power Conversion applications including grid connect electronics for energy storage
- Design and analysis of 100kW Inverter application
  - full SiC system at 30% of the volume and weight of today’s systems or alternatively could save 80% of the conduction and switching loss in the same volume.
  - Similarly, hybrid Si/SiC technology available today can save approximately 30% of either the volume or weight or of the switching energy being dissipated (25%+ lower losses).
- This provides the designer with choices and trade-offs.
- The economics look reasonable once Silicon Carbide costs come down to some reasonable multiplier of Silicon.
- Inverter costing very interesting, all energy intensive raw materials are rising significantly in cost (have been).
- There are many further tasks and challenges to be addressed before full SiC power conversion systems become a reality.