SIC JFETS REDUCE THE BALANCE-OF-SYSTEM FOR STATIONARY ENERGY STORAGE POWER CONVERSION SYSTEMS

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The widespread adoption of energy storage deployment requires the cost for the power conversion stages to be significantly reduced. The high cost of inversion is driven largely by the performance limitations of Si-IGBTs and Si-IGCTs, especially when a higher DC-link voltage (>1 kV) is desired to facilitate the reduction of the balance-of-system. SiC unipolar devices, however, offer great promise for increasing the DC link voltage, while maintaining high system efficiency without increasing system complexity. Such a switch platform could enable small, lightweight, transformerless topologies for industrial medium voltage grid applications operating at 3.3 or 4.16 kV AC. This report discusses the state-of-the-art 1.2kV SiC JFETs as a proven technology platform, and demonstrates the benefits of the JFET through operational comparisons with SiC-MOSFETs and Si-IGBTs. In addition, SiC JFET device reliability is demonstrated up to 200°C and the impact of a 6.5 kV JFET platform on power conversion systems is discussed.

Keywords: Silicon Carbide, JFET, Storage, Inverter, DC-Link

INTRODUCTION

The widespread adoption of energy storage applications for both renewable resources and power conditioning can be greatly facilitated if the cost for the power conversion stages, which can be 30% or higher of a total storage system, is significantly reduced. The balance-of-system costs for inverters are driven largely by the performance limitations of existing Si-IGBTs and Si-IGCTs when increasing the DC-link voltage above 1 kV, which reduces the effective device switching speed and results in a severe impact on system component size and cooling. The excellent material properties of silicon carbide (SiC) semiconductors offer great promise for increasing the DC link voltage to well over 1 kV, while maintaining high efficiency and also achieving smaller more cost effective power conversion [1]. The ability to increase the DC-link voltage up to 4 kV, is especially attractive for SiC unipolar devices, for example, a JFET or MOSFET rated at 6.5kV, could easily accommodate such operational voltages, while maintaining high switching speeds of 20kHz. Such a platform could enable small, lightweight, transformerless topologies for industrial medium voltage grid applications operating in the 3.3kV or 4.16 kV regimes.

The recent emergence of reliable 1.2kV SiC devices has solidified the process and supply chains, where Schottky diodes have now demonstrated commercial success and clearly show efficiency benefits for hybrid systems, such as PFC applications, micro-inverters and motor drives, running in tandem with Si-MOSFETs and Si-IGBTs. Furthermore, demonstrations of inverters utilizing 1.2kV SiC-JFETs and SiC-MOSFETs are emerging, where the efficiencies are reaching >99% and operating at a 1 kV DC link voltage [2,3,4]. This report will outline the current state-of-the-art for 1.2kV SiC JFETs as a commercially proven technology device platform, demonstrating the benefits of the JFET through operational comparisons with SiC-MOSFETs, and Si-IGBTs of similar rating. Switch losses and device reliability for the normally on and normally off cascoded SiC JFET are presented.

The second topic of the report will outline the progress and benefits of commercializing a 6.5 kV SiC switch platform. The benefits lie in the ability to increase the DC link voltage without suffering device switching speed. Higher DC-link MW power conversion systems present an attractive space for SiC wide bandgap devices, as no other technology can reach such high voltage ratings (up to 20kV), and maintain high frequency operation with significantly reduced cooling constraints. As 1.2-1.7kV SiC devices continue to gain commercial acceptance, the processes and supply chain infrastructure needed for 5-10 kV devices is quickly being solidified. One key challenge is obtaining high yield epitaxial wafers requiring a 70 μm low doped drift layer needed for 6.5 kV rated devices. However, significant advancements have been made on the substrate and epitaxial quality and are discussed.

To demonstrate the benefits of 6.5kV rated SiC-JFETs, a single stage of an inverter was simulated using Gecko-CIRCUITS where the circuit used in the simulation represents one stage of a cascaded H-bridge inverter. The system efficiency was calculated and compared to commercially available 6.5kV Si-IGBTs. Results show that at frequencies ranging from 5 to 20 kHz, SiC devices can provide a path to reduce losses and system complexity for MW storage power conversion systems.

1.2 kV SIC VJFET DEVICES

Figure 1 shows the cross-section of USCi's 1.2 kV, 60mΩ Vertical Junction Field Effect Transistor (VJFET) and packaging in a TO-247. The depletion mode device performance is plotted in Figure's 2 and 3 for ambient temperatures up to T_{amb}=175°C.

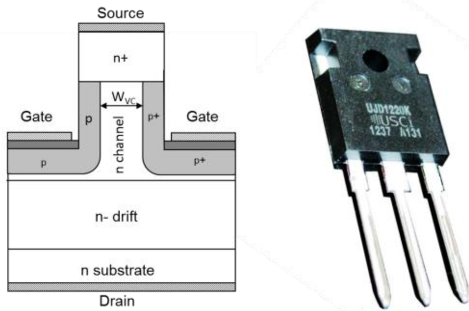


Fig. 1 Normally on VJFET cross-section and TO-247 package.

Figure 2 shows the forward conduction for a range of negative gate biases for the normally on JFET exhibiting a -5V pinch off voltage.

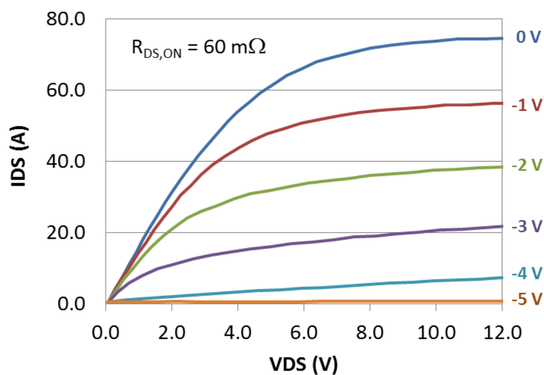
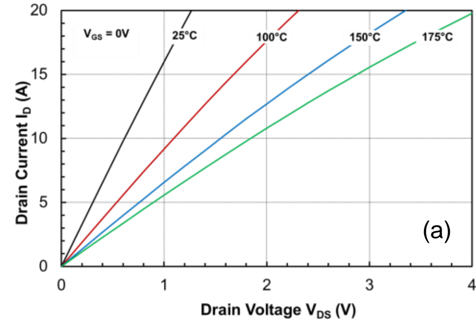
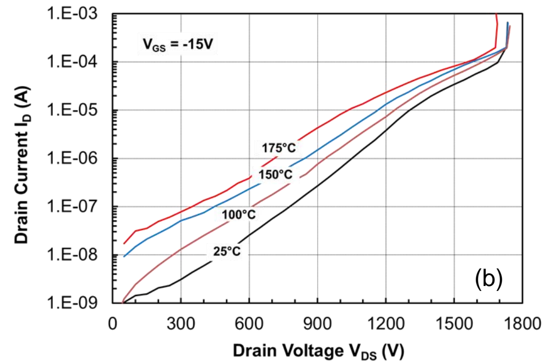


Fig. 2 USCi's 1.2kV normally on 60mΩ JFET at 25°C showing a pinch off voltage at -5V.

The forward conduction (Fig. 3a) at 0V gate bias has a positive temperature coefficient as expected for a unipolar device where the resistance goes from 60mΩ at T_{amb}=25°C to 180mΩ at T_{amb}=175°C. A positive temperature coefficient is beneficial for paralleling switches in power modules for scaling up in current as it facilitates current sharing. At a gate bias of -15V (Fig. 3b) the device avalanches at 1.7 kV and has a very low leakage at T_{amb}=175°C of 25 µA at V_{DS}=1.2kV. The gate-source leakage vs. temperature (Fig. 3c) also demonstrates a small variation with temperature and a maximum leakage of 2 µA at T_{amb}=175°C. The SiC JFET's performance invariance with temperature is the fundamental reason why it exhibits robust reliability which will be discussed in a later section. Being JFETs, the devices do not contain a SiC-MOS gate interface, and are thus also immune to the common temperature related reliability problems exhibited by SiC MOSFETs [5,6].





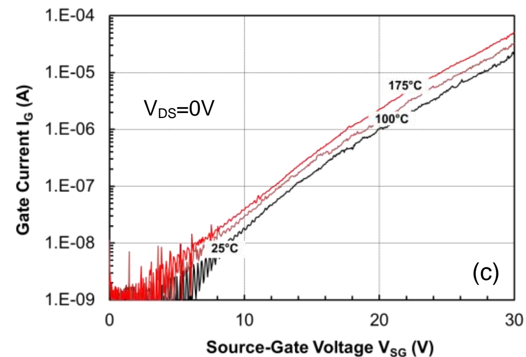


Fig 3 (a) Forward conduction under 0 V gate bias for T_{amb} ranging from 25°C to 175°C, and (b) drain leakage and (c) gate-source leakage.

Cascoded 1.2 kV SiC VJFET Devices

In addition to the discrete normally on JFET, a cascoded version has been assembled where the SiC JFET is in series with a low voltage Si-MOSFET as seen in Figure 4. The cascoded JFET behaves as a normally off device which has two advantages. The first satisfying fail safe topologies requiring normally off devices and the second, the cascoded normally on JFET can be driven by a standard MOSFET driver providing a "plug and play" alternative for power conversion systems utilizing Si-IGBT's, but with the benefits of enhanced switching speed at higher voltage.

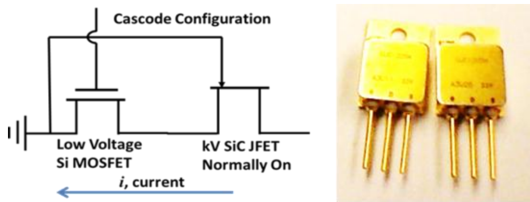


Fig. 4 Cascoded normally on SiC JFET with Si-MOSFET to create a normally off device and TO-254 high temperature package.

Figure 5 shows the forward conduction of a cascoded 80mΩ JFET using a Si-MOSFET with V_{TH}=4V. The cascode has a body diode formed by the reverse-conducting SiC normally-on JFET and the Si MOSFET body diode. Since the Si MOSFET is a low voltage device, typically rated from 25V to 50V, the cascode body diode has virtually no stored charge and a very low diode forward voltage drop. Like the normally on device, the cascoded JFET also demonstrates a strong invariance of parameters over wide temperature ranges and is described in detail in an earlier paper [7].

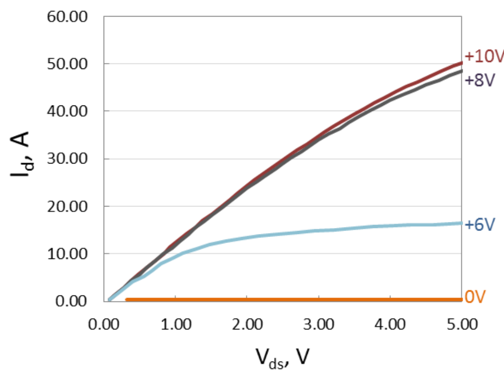


Fig. 5 USCi's 1.2kV normally off cascoded 80mΩ JFET at 25°C showing a turn on voltage at +8V.

1.2 kV Switching Characteristics

To demonstrate the benefits of SiC devices over similarly rated Si-IGBTs, the switching behaviors of the devices were investigated under an inductive load condition. Figure 6a presents the measured switching turn on waveforms at 600V-10A with an inductive load at 150°C. For comparison, commercially available 1.2kV SiC MOSFETs and 1.2kV Si-IGBTs are also plotted. The turn on times vary from ~30 ns for the cascoded JFET and the commercial vendor 1 SiC MOSFET to >100 ns for the Si-IGBT and the commercial vendor 2 SiC MOSFET. The normally on JFET has an increased turn-on time of ~50ns from the cascoded version, resulting from the high C_{RSS} of the trench structure.

The real benefit of the unipolar SiC devices is seen in the turn off waveforms presented in Figure 6b for the same devices under the same conditions. The bipolar Si-IGBT turn off waveform (black) exhibits a long current tail due the need to remove carriers from the drift layer upon turn off. Furthermore, the current tail is a strong function of temperature and operation voltage. In contrast, the SiC unipolar devices turn-off times are not only an order of magnitude shorter, but are also invariant with temperature, thus allowing SiC unipolar devices to be pushed to much higher operation frequencies than Si-IGBTs without nonlinear heating effects that require excessive cooling apparatus. In addition, SiC devices can run at temperatures up to 200°C, thereby relieving the cooling constraints even further.

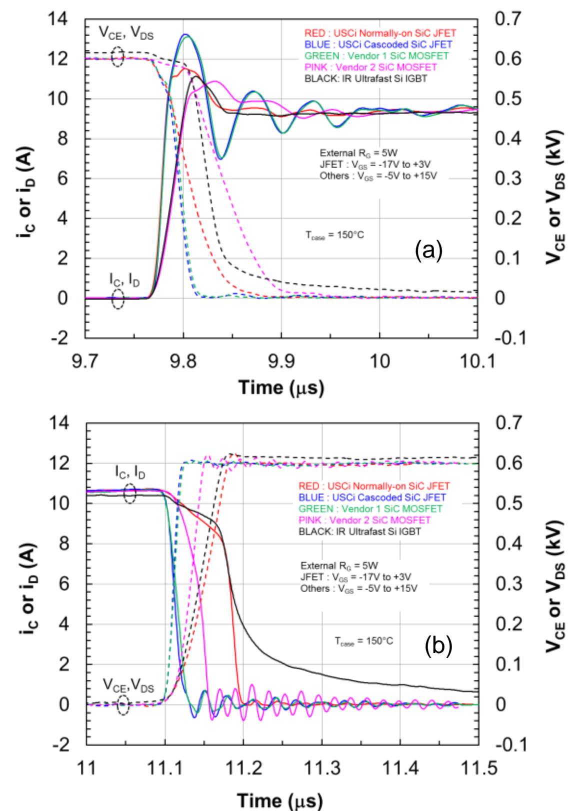


Fig. 6 (a) Turn-on and (b) turn-off waveforms at 600V,10A comparing USCi's normally on JFET in standard and cascoded configurations with 2 commercially available SiC MOSFETs and a Si-IGBT of similar rating.

1.2 kV SiC VJFET Reliability

Demonstrating reliability of SiC devices is key to gaining widespread adoption of the technology. The SiC VJFET is inherently reliable due to its simple structure that does not involve a SiC-MOS interface. The SiC-MOS interface has a well-documented reliability issue that has kept the operation temperature lower than other SiC devices to avoid threshold drifting [8,9]. The SiC JFET operation temperature, however, is only limited by the packaging temperature limits.

Figure 7 shows the DC characteristics of the normally on JFET after 550 hours of a simultaneous High Temperature Reverse Bias (HTRB) and a High Temperature Gate Bias (HTGB) at rated voltage of 1.2 kV and -20V respectively. The case temperature was held at T_{case}=175°C. The HTRB/HTGB test is designed to accelerate the failure modes at the metal-SiC interfaces, the junctions, as well as the edge termination process under reverse bias by increasing the ambient temperature. After 550 hrs, the devices show no degradation as seen in Fig 8a for forward conduction, Fig 8b for drain leakage, Fig 8c for gate leakage and Fig 8d for gate threshold.

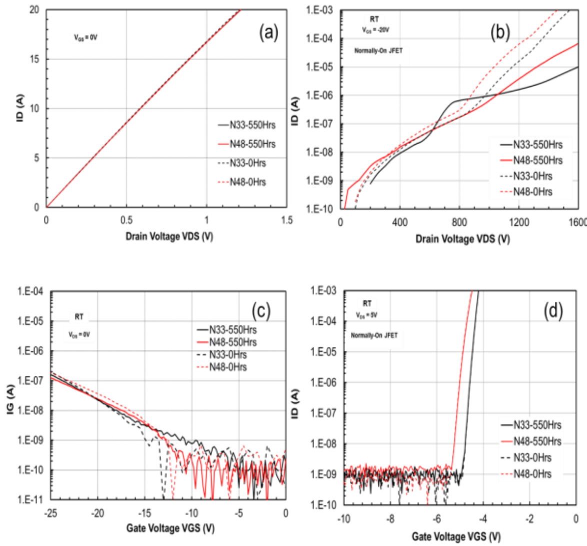


Fig 7 Before and after HTRB/HTGB stress for normally on SiC JFETs (a) forward, (b) drain leakage, (c) gate leakage and (d) gate threshold currents showing no degradation after 550 hrs at T=175°C and 1.2kV DC bias.

The cascoded JFETs were also tested under similar conditions, where a step-stress in temperature was used to evaluate the ability of the assembly to withstand the HTRB test. A high temperature hard solder was used on both devices in a TO-254 package to allow testing up to 200°C [7]. For the cascode, the drain bias was held at 960 V (80% device rating) and the gate tied to the source. The step stress conditions are shown in Fig 9a, where the devices were held at 150°C for 60 hrs, then elevated to 175°C for 100 hrs, then to 200°C for 80 hrs. Figure's 8(b-d) show the DC characteristics at room temperature before and after step stress including the (b) forward current, (c) drain leakage and (d) gate threshold and leakage.

Both of the devices, the normally on and cascoded normally off SiC JFETs, show robust behavior at elevated temperatures well above the temperature limits of SiC-MOSFETs and demonstrate the superior performance of the unipolar SiC JFET.

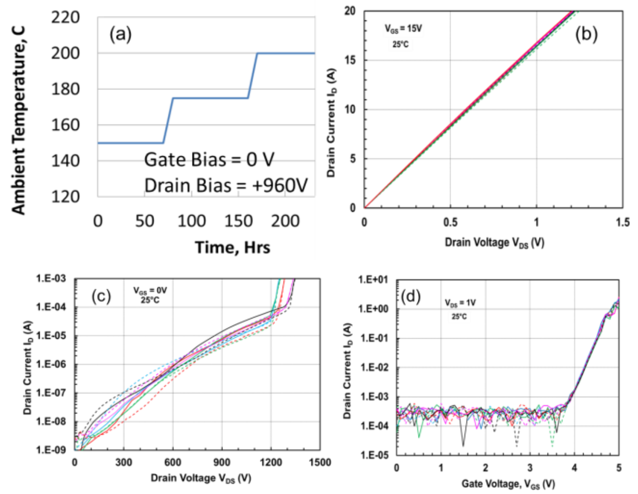


Fig 8 Before and after HTRB stress for normally off cascoded SiC VJFETs (b) forward, (c) drain leakage, (d) gate threshold currents showing no degradation after 200 hrs of temperature step stressing at 80% rated drain bias (960V).

6.5 kV SIC VJFETs AND INCREASING DC-LINK VOLTAGES

There is currently a push with MW conversion systems to increase the DC-link voltage above the typical ~1 kV level to facilitate reductions in system complexity and the entire balance-of-system costs [10,11]. At a given power level, a higher DC-Link voltage can reduce the system current, decrease losses and enhance reliability. However, higher DC-link voltages require higher voltage rated switches, or many stacks of lower rated devices. For example, the 40MW battery energy storage system for Golden Valley Electric Association built by ABB in Alaska utilizes high current (kA) 4.5 kV rated IGCTs to operate with a 5 kV DC link [12]. Such IGCTs run at sub-kHz frequencies and must be water cooled with elaborate DI water systems or run in very short higher frequency burst modes to avoid overheating [13]. High current 6.5 kV rated IGBTs are also employed for MW class inverters, but the long current tail and excessive heating at this power level limit the frequency of operation to a few kHz and below [14]. The high current and slow frequency offered by these high voltage Si switches has a large impact on the power converter system as bulky and expensive magnetics, cabling and DI water systems are needed.

Higher DC-link MW power conversion systems present an attractive space for SiC wide bandgap devices, as no other technology can reach such high voltage ratings (up to 20kV) and (or while maintaining) maintain high frequency operation with significantly reduced cooling constraints. As 1.2-1.7 kV SiC devices continue to gain commercial acceptance, the processes and supply chain infrastructure needed for 5-10 kV devices is quickly being solidified. In addition, the fabrication of 5-10 kV unipolar devices is highly similar to the 1.2-1.7kV node, thus the technology will enable new topologies and applications such as high DC-link MW storage and renewable energy systems in the future. The material growth issues for thick (>50

μm) 4H-SiC drift layers are rapidly advancing due to improvements in the substrate quality and CVD recipe development. Micropipes are no longer an issue, and many groups have now demonstrated conversion methods for other defects like stacking faults and basal plane dislocations to yield high quality thick epitaxy layers [15, 16]. Figure 9 shows epitaxial results for a 70 μm drift layer thickness and doping for 6.5 kV rated devices on 100 mm wafers. In addition, 150 mm substrates are now emerging and will be employed in the next few years, which will have a drastic effect on the cost of SiC devices.

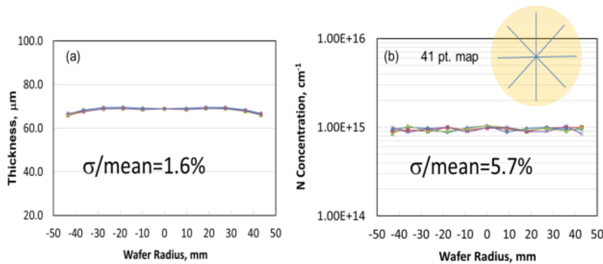


Fig. 9 Epitaxial drift layer (a) thickness and (b) doping uniformity measurements across a 100 mm 4H-SiC wafer grown at USCi.

To demonstrate the benefit of unipolar 6.5 kV rated SiC-JFETs, an analysis was performed to compare the losses of a 6.5kV rated Si-IGBT to that of SiC JFETs currently being fabricated at USCi. For the 6.5 kV rated normally off SiC-JFETs, a simulation of the turn-on and turn-off energies vs. current was generated. For the 6.5 kV Si-IGBTs, the same curves were taken from the product datasheet for the 6.5 kV/250A Infineon module (FZ250R65KE3). Figure 10 (a-d) shows the simulated results for the 6.5 kV normally off SiC-JFET.

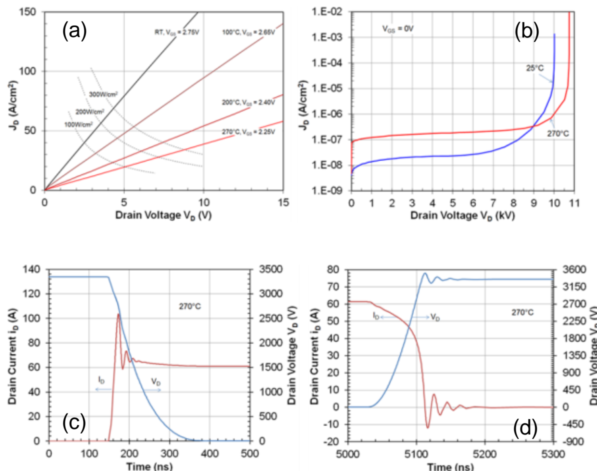


Fig 10 Simulated (a) forward conduction, (b) blocking, (c) turn-on waveform and (d) turn-off waveform for a 6.5 kV normally off JFET operating a 3.3 kV and 60 A.

The turn-on and turn off energies vs. current are depicted in Figure 11, where it can easily be seen that the switching losses of the Si-IGBT are estimated to be 4X that of the SiC-JFET, as the JFET is expected to have much shorter turn-on and turn-off times, as demonstrated at the 1.2kV node. The data for the JFET was simulated at 125°C to compare to the datasheet of the Si-IGBT module.

To demonstrate the benefits of SiC-JFETs, a single stage of an inverter was simulated using Gecko-CIRCUITS where the circuit used in the simulation represents one stage of a cascaded H-Bridge inverter. Since all H-bridges would be identical, this is sufficient for evaluating the losses in the switching devices. The inverter was dimensioned for 100kVA output per phase. An input voltage of 4 kV was selected and the

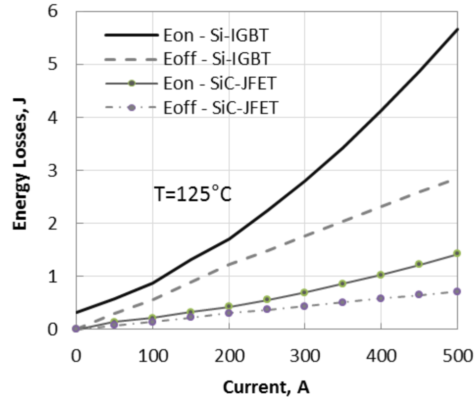


Fig. 11 Turn on and turn off energies vs. current for 6.5 kV rated SiC JFET (simulated) and Si-IGBT (datasheet) at 125°C.

output voltage was set to 2.4 kV RMS at 60 Hz. The inverter load was modeled as a resistor with an LC filter optimized for 100 kW output power at 60 Hz. Figure 12 below shows the simulation circuit depicting one of the three inverter phases, the other two are identical. For the evaluation of the losses, only one phase was taken into account.

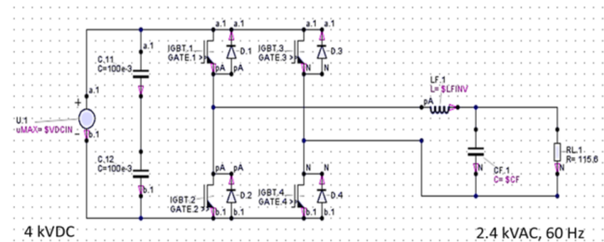


Fig 12. Simulated single stage of H-bridge inverter with a resistive load and optimized for 100kW output power.

The losses for the diodes were artificially set to zero to focus only on the losses seen by the switches. This is valid as using SiC JBS diodes have zero recovery energy, and is often omitted in simulations. In any case, using a Si-IGBT or a SiC JFET, the antiparallel diodes are considered to be SiC. For each device the simulation examined the efficiency for a range of inverter output power from 20 to 100 kW as well as in switching frequency, varying from 5 to 20 kHz. The average output power and switch losses were used to calculate the inverter efficiency for all operating points using the following simple formula:

$$Eff = \frac{P_{output}}{P_{output} + P_{Switching.Loss} + P_{Cond.Loss}}$$

Figure 13a shows the simulated losses for a few cycles for two switches for the case of the 6.5 kV SiC-JFET switching at 4 kV. Clearly the switching losses dominate as the conduction losses for SiC devices is an order of magnitude smaller. Figure 14b compares the inverter simulation efficiency for both cases of the Si-IGBT and the SiC-JFET up to 20 kHz operation, where the output power was optimized at 100kW. The SiC-JFET shows much higher efficiency, especially at higher frequencies when compared to the Si-IGBT as expected by the lower switching losses and negligible conduction losses.

The Si-IGBT shows efficiency results that are very low. This is based on the fact that all commercially available Si-IGBTs with high voltage rating also have a much higher current rating than the SiC device that was used for these simulations. The Si-IGBT suffer higher on resistance due to the threshold at low currents, therefore Si-IGBTs are typically designed for high current applications. The higher conduction losses combined with the higher switching losses of the Si-IGBT start to significantly degrade efficiency when operated in a high frequency low current application.

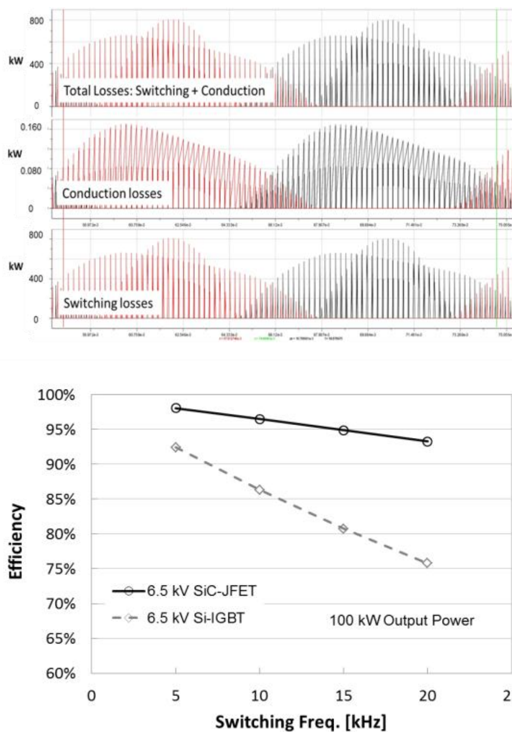


Fig. 13 Simulated results for a single stage of an H-bridge inverter where (a) shows the losses for 2 switches over a few cycles for the SiC-JFET case, and (b) the inverter output efficiencies simulated for the 6.5 kV rated SiC-JFETs and Si-IGBTs.

However, to gain the benefits on the balance of the system, the goal is to increase the DC-Link voltage, reduce the current, and increase the frequency to have a significant impact on the magnetic components. In addition, the lower losses of the SiC-JFETs relieve the cooling constraints, where elimination of the water can be achieved.

The MW class power conversion systems for storage and renewable resources will no doubt benefit from the development of medium voltage SiC switch platforms capable of high frequency operation. In particular, for industrial utility applications, where transmission lines run at 4.16 kV AC (U.S.) and 3.3 kV AC (Europe and Japan), a simple 3 level neutral point clamped (NPC) inverter can be conceived utilizing 6.5 kV rated SiC devices providing a transformerless grid-tie option for more distributed storage applications. Such an application is attractive to data centers and hospitals where power reliability and stability are key. Figure 14 depicts a simple topology where batteries are stacked to a DC-link voltage of 6 kV allowing direct grid-tie to a 4.16 kV AC industrial distribution line. If the cost of the entire power conversion system can be reduced, then the application becomes attractive to commercial companies as well as public utilities.

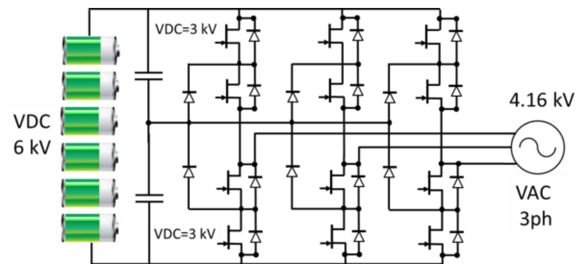


Fig. 14 Three level neutral point clamped inverter utilizing 6.5 kV rated SiC-JFETs to form a transformerless direct grid-tie from battery storage to an industrial distribution line.

Conclusion and Future Work

With the maturation of unipolar SiC devices rated at 1.2 kV, the processes and supply chain infrastructure needed for 5-10 kV devices is quickly being solidified. The SiC JFET has been demonstrated to be highly robust with superior switching characteristics to that of similarly rated Si-IGBTs. The ability to commercially deploy 6.5 kV rated SiC devices capable of high frequency operation (~20 kHz) can have a significant impact on power conversion systems by reducing complexity and the balance of the system. United Silicon Carbide is in the process of fabricating 6.5 kV normally off JFETs, which will be assembled in a half-bridge power module and results will be reported.

Acknowledgments

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