DEGRADATION MECHANISMS AND CHARACTERIZATION TECHNIQUES IN SILICON CARBIDE MOSFETs AT HIGH-TEMPERATURE OPERATION

R.J. Kaplar, S. DasGupta, M.J. Marinella, B. Sheffield, R. Brock, M.A. Smith, and S. Atcitty

Sandia National Laboratories, Albuquerque, NM, USA

Due to a number of advantages over silicon, including higher breakdown field, higher operational junction temperature, and higher thermal conductivity, silicon carbide (SiC) has generated keen interest as a material of choice for power electronic devices. Device characteristics resulting directly from SiC's superior material properties, including enhanced ability to withstand high voltage, lower on-state resistance and capacitance permitting higher switching frequency, and reduced thermal management requirements, give SiC-based power devices the potential to greatly reduce the system footprint and cost, and to increase system efficiency. Among all the possible semiconductor switches, the field-effect transistor provides very low switching loss and is thus an attractive option, especially at high switching frequency. A SiC metal-oxide semiconductor field-effect transistor (MOSFET) is now commercially available that provides a blocking voltage of 1200 volts (V), maximum DC current capability of 33 amps (A), and on-state resistance R_{on} of 80 milliohms (mΩ). However, the reliability of the silicon oxide (SiO_2) insulator on SiC at high temperature is an open question. The predominant degradation trends in this MOSFET under high-temperature overvoltage and pulsed overcurrent stress are reported in this work. We also describe the development of a microcontroller-based condition monitoring module that can track changes in the semiconductor device characteristics in order to improve real-world system availability.

SiC MOSFETs have traditionally suffered from poor oxide-semiconductor interface quality, which has led to large threshold voltage instability [1]. Fortunately, recent process improvements have mitigated this problem to a large degree. In particular, the commercially available MOSFET (or in some cases, pre-production versions of the same MOSFET) that we studied showed no signs of degradation when operated below the maximum temperature specified by the manufacturer (125 °C). However, significant degradation is evident if the temperature of the device is raised above 125 °C (Figure 1).

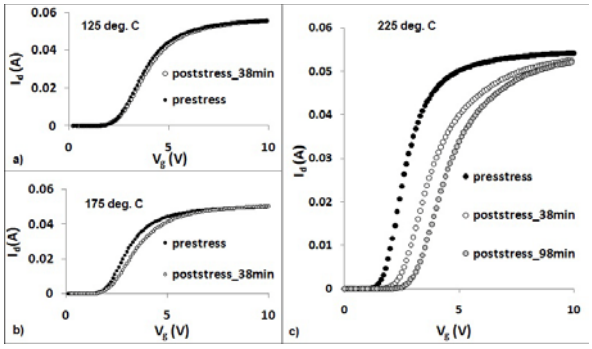

Fig. 1. I_d-V_g characteristics of SiC MOSFET stressed at various temperatures (V_g = +20 V, V_d = 0.1 V).

On the drain current versus gate voltage (I_d-V_g) curves shown, a shift in the subthreshold portion of the curve is evident after stress at 175 °C, and is much more severe after stress at 225 °C. Analysis of these curves indicates a large (on the order of 10^{12} $cm^{-2}eV^{-1}$) density of electrically active traps at the SiC/SiO_2 interface, as well as the presence of charge trapped in the SiO_2 gate [2], consistent with electron trapping. Bias under negative gate polarity (which does not turn the device on, but the device could still see negative gate pulses during off-state operation in a power electronics system) results in enhanced degradation (Figure 2) consistent with hole injection into the oxide. Varying degrees of degradation have been observed for devices exhibiting nearly identical initial characteristics, and we have identified a characteristic of the integrated free-wheeling diode that correlates with the observed degradation. For both gate stress polarities, the magnitude of threshold voltage shift increases with increasing temperature (Figure 3).

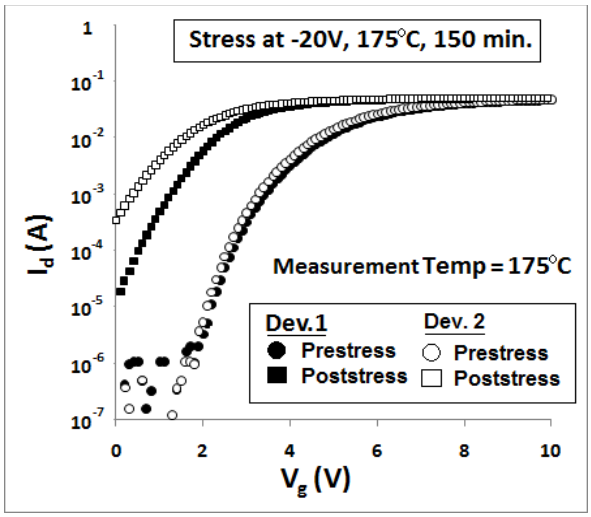

Fig. 2. Post-stress (stress: V_g = -20 V @ 175 °C for 150 minutes) degradation in I_d-V_g characteristics (V_d = 100 mV) of two nominally identical SiC MOSFETs.

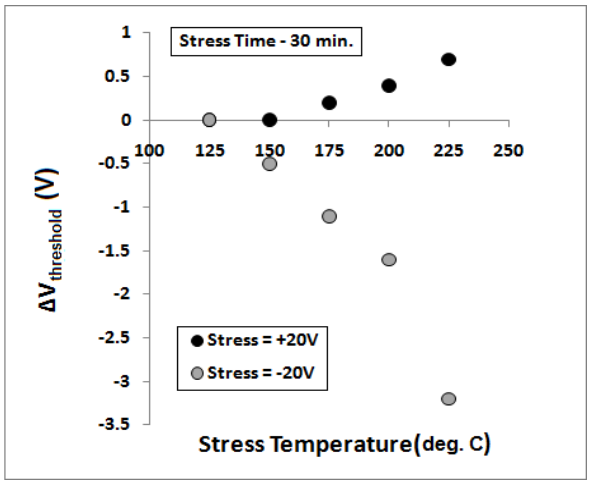

Fig. 3. $V_{threshold}$ shift due to V_g = ±20 V gate stress for 30 minutes, plotted as a function of temperature. The device is recovered exactly to the initial state at the start of each bias step.

Devices were also stressed under pulsed conditions at room temperature. Pulsed overcurrent operation (Figure 4a) showed degradation similar to what was observed under high-temperature, positive-V_g DC stress, consistent with electron injection into the oxide (Figure 1, positive voltage points on Figure 3). This may be due to transient heating of the device beyond the junction temperature specification (T_j = 125 °C). Figure 4b shows the transient current profile for a single switching cycle. The actual switching is preceded by a very high-current spike that lasts about 10 microseconds. This high-current transient is likely a significant factor in device degradation under pulsed overcurrent conditions, since for the same switching levels (V_g = +8 V, V_d = 20 V) 1-kilohertz (kHz) operation produces much faster degradation than 1-Hz operation.

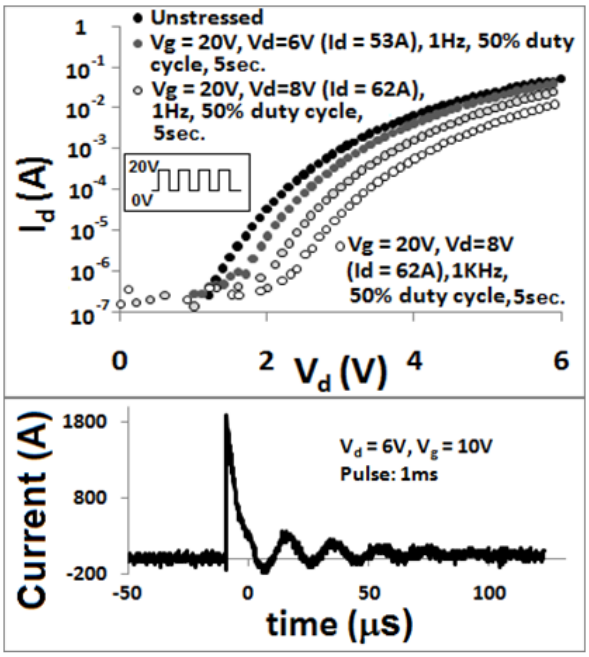

Fig. 4. (a) Degradation in a SiC MOSFET due to pulsed overcurrent conditions, similar to the effects of positive gate bias DC stress at high temperature. (b) The high transient current peaks observed during switching are likely responsible for enhanced degradation at high switching frequency.

The effects of MOSFET device degradation on system availability can potentially be mitigated through Condition Monitoring (CM) and Prognostics and Health Management (PHM). CM consists of monitoring component and/or system characteristics in situ to ascertain its health, and to detect anomalies and diagnose problems in order to flag maintenance needs. PHM goes further by not only tracking damage growth, but by also predicting time to failure (by comparing the state of the component to previously established reliability models), and by managing subsequent maintenance and operations in such a way to optimize overall system utility against cost. PHM seeks to optimize the trade-off between premature device replacement and disruptive failures. In our scenario, a well-developed method of CM and/or PHM can considerably increase the feasibility of exploiting the superior switching performance of the SiC MOSFET even before it reaches the level of technological maturity of Si-based devices (the latter

has been studied and developed since the 1940s and has a several-decades head start over all competing technologies).

We have developed a 16-bit Microchip PIC [3]-based system to monitor the characteristics of the device while it is in operation. A current sense circuit uses a resistive network to perform a current-to-voltage conversion and communicates with the microcontroller through an opto-coupler (which is utilized to provide electrical isolation between the microcontroller and the power device). The setup has a built-in gate control circuit that uses the pulse-width-modulated (PWM) signal from the controller to provide a variable output to the gate. Figure 5 shows the output of our monitoring setup resulting from a slow voltage ramp applied to the gate of a SiC MOSFET biased at V_d = 5 V. The output current and threshold voltage match the device characteristics measured with standard laboratory equipment, showing a successful implementation of the most basic and vital block of the CM module. Measurements of this curve as the device is stressed, as well as efforts to increase the compactness and portability of the system, are currently in progress.

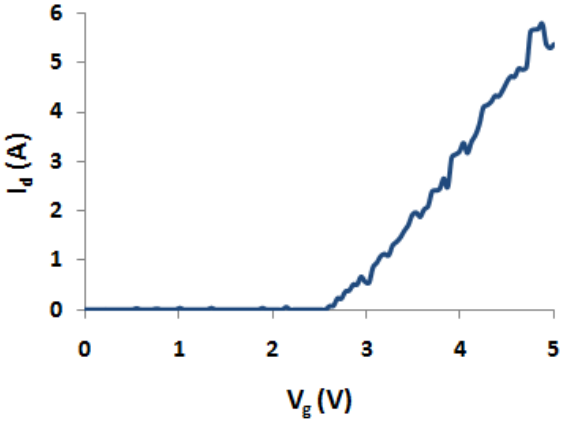

Fig. 5. I_d-V_g curve of a SiC MOSFET, biased at V_d = 5 V, measured using our prototype microcontroller-based CM setup.

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REFERENCES

[1] A.J. Lelis, D. Habersat, R. Green, A. Ogunniyi, M. Gurfinkel, J. Suehle, and N. Goldsman, "Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements," *IEEE Trans. Electron Devices* **55**, 2008, pp. 1835-1840.

[2] S. DasGupta, R. Brock, R.J. Kaplar, M.J. Marinella, M.A. Smith, and S. Atcitty, "Extraction of trapped charge in 4H-SiC metal oxide semiconductor field effect transistors from subthreshold characteristics," *Appl. Phys. Lett.* **99**, 2011, pp. 023503-023505.

[3] Microchip 16-bit Digital Signal Controller Product Datasheet, available online at http://ww1.microchip.com/downloads/en/DeviceDoc/70593B.pdf.

BIOGRAPHICAL NOTE

Conference presenter: Robert Kaplar received a B.S. degree in Physics from Case Western Reserve University, Cleveland, Ohio (1994), and M.S. and Ph.D. degrees in Electrical Engineering from Ohio State University, Columbus, Ohio (1998 and 2002). From 2002 to 2005 he was a Post-Doctoral Researcher at Sandia National Laboratories (SNL), Albuquerque, New Mexico. Since 2005 he has been a Senior Member of the Technical Staff at SNL. His current work focuses on semiconductor device characterization, reliability, and physics for Very Large Scale Integration (VLSI) and power device applications.