DEGRADATION MECHANISMS AND CHARACTERIZATION TECHNIQUES IN SiC MOSFETs AT HIGH TEMPERATURE OPERATION

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Due to a number of advantages over silicon, including higher breakdown field, higher operational junction temperature, and higher thermal conductivity, silicon carbide (SiC) has generated keen interest as a material of choice for power electronic devices. Device characteristics resulting directly from SiC's superior material properties, including enhanced ability to withstand high voltage, lower on-state resistance, lower capacitance permitting higher switching frequency, and reduced thermal management requirements give SiC-based power devices the potential to greatly reduce power conversion system footprint and cost, and to increase system efficiency. Among all the possible semiconductor switches, the field-effect transistor provides very low switching loss and is thus an attractive option, especially at high switching frequency. A SiC Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is now commercially available that provides a blocking voltage of 1200 V, maximum DC current capability of 33 A, and ON-state resistance R_{ON} of 80 mΩ. However, the reliability of the SiO_2 insulator on SiC at high temperature is an open question. The predominant degradation trends in this MOSFET under high-temperature over-voltage and pulsed over-current stress are reported in this work. We also describe the development of a microcontroller-based condition monitoring module that can track changes in the semiconductor device characteristics in order to improve real-world system availability.

Prior to discussing the details of our studies on SiC MOSFETs, some background material on power electronics in the context of energy storage systems is reviewed, which provides motivation for the use of SiC-based switching devices in such systems. Energy storage systems (e.g. batteries) are typically DC and require power electronics to interface with the grid. This is illustrated schematically in Figure 1 below. In this example, the power electronics converts the DC power provided by the energy storage unit to AC. The AC is then stepped-up to the grid voltage by the transformer.

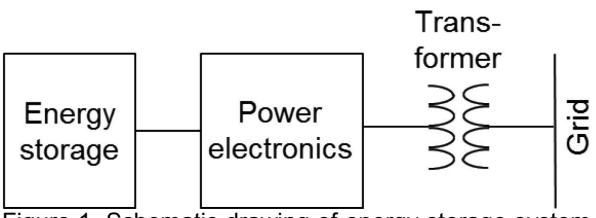

Figure 1. Schematic drawing of energy storage system and electric utility grid, illustrating how power electronics links the two.

A typical power electronics circuit is shown in Figure 2. This is a single-phase H-bridge that converts DC (i.e. the energy storage) to AC. Note the four semiconductor switches shown in the figure. In the figure these are illustrated as MOSFETs, although other types of switches are often used in practice, such as Insulated-Gate Bipolar Transistors (IGBTs) and Thyristors [1]. Note that each semiconductor switch has a free-wheeling diode in parallel with it, in order to provide a path for transient current flow when an inductive load is present. A DC bus capacitor is also utilized to smooth the voltage ripple across the DC source. The load is connected between the mid-points of each leg of the "H" and AC voltage is achieved by alternately switching the top-left and bottom-right switches ON (with the other two switches off), followed by switching the top-right and bottom-left switches ON (with the other two switches off), which creates alternating polarity across the load. In practice, a simple square wave is not utilized, since it is not easily filtered to extract the fundamental sine-wave that is required for the grid; rather, a Pulse-Width-Modulation scheme is employed to enhance the amplitude of the fundamental frequency compared to higher-order harmonics. The PWM switching frequency is typically on the order of 10 kHz. The PWM switching scheme is illustrated in Figure 3. Note the fundamental-frequency sine wave superimposed on the PWM square wave.

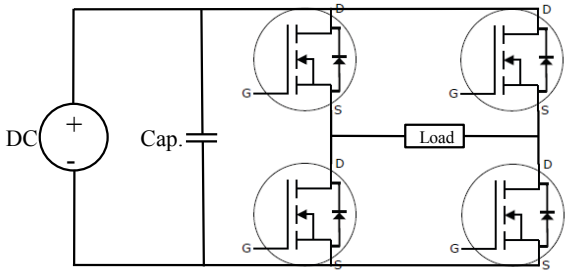

Figure 2. Typical power electronics circuit utilizing semiconductor switches.

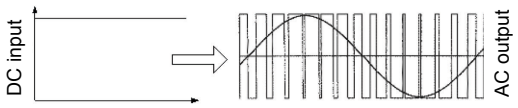

Figure 3. Illustration of PWM switching and filtering to extract a sine wave from a DC voltage.

The semiconductor switches utilized are the heart of the power conversion system and are the major factor that determines the performance, reliability, and cost of the overall system. Factors such as on-state loss, switching loss (determined by the turn-on and turn-off times of the switches), and the ability to withstand high voltage in the OFF-state are critical. Reliability is also key. The devices are subjected to various electrical and thermal stresses during operation. They alternate between the high-voltage, low-current OFF state and the low-voltage, high-current ON state. Additionally, during the switching transient they are subjected to a brief period of both high voltage and high current (i.e. high power), and may need to operate in high temperature environments (which tends to degrade their lifetime). The high currents experienced during the ON-state generate a large amount of heat, which may

degrade device reliability if it is not dissipated efficiently.

The vast majority of power semiconductor switches in use today (2011) are constructed from Silicon. However, emerging wide-bandgap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) have properties that make them theoretically superior to Si for power switching applications. The remainder of this paper will discuss SiC, particularly the characterization of a commercially available SiC MOSFET that has recently (January 2011) come on to the market from a major SiC manufacturer. While GaN devices will not be discussed in detail here, we note that they are a competing technology and they have various advantages and disadvantages compared to SiC-based devices.

A graph showing five physical properties of SiC is shown below in Figure 4. In the figure, the red pentagon represents the properties of Si, normalized to 1. The grey region shows the corresponding properties of SiC on a logarithmic scale, read radially outward from the center of the figure. We see that SiC has a wide bandgap, which limits the extrinsic carrier concentration and thus allows the semiconductor to operate at high temperature; it has a high breakdown field, which limits avalanche breakdown (runaway carrier multiplication) and thus permits the material to withstand high voltage; it has a low dielectric constant, which limits parasitic capacitance and permits faster switching; it has high electron saturation velocity (endpoint of the linear region of the electron velocity vs. electric field curve), also allowing high-frequency operation, as well as high current density; and high thermal conductivity, which facilitates efficient heat dissipation. All of these properties are superior to those of Si in terms of application to power switching devices.

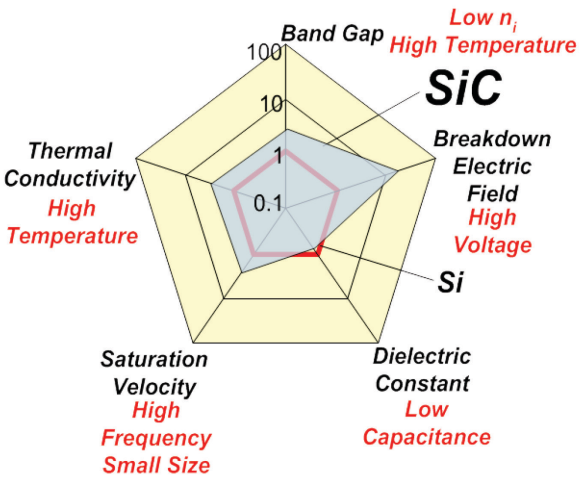

Figure 4. Diagram illustrating relative magnitudes of five properties of SiC relative to Si (figure courtesy of Professor Dieter K. Schroder, Arizona State University).

A second way to look at the properties of SiC (as well as GaN) compared to Si is shown in Figure 5. In this figure, the specific on-state resistance (i.e. the on-state resistance normalized to unit area) vs. breakdown voltage is shown. The solid curves are calculated for the three materials, assuming bulk material (i.e. a resistor), and thus do not take into account novel device designs. Nevertheless, variants of this chart are ubiquitous in the power electronics community since it clearly illustrates the advantages of SiC (and GaN) compared to Si. Low on-state resistance and high breakdown voltage are desired for a power switching device; thus, points in the lower-right portion of the chart are preferred. It is evident that the curve for SiC is shifted down and to the right, compared to the curve for Si (the GaN curve is shifted in the same direction even further). Thus, in theory SiC can provide a device that has lower on-state resistance and higher breakdown voltage than Si device. Also shown on the plot are several devices that have been reported by various groups. Note that the Si device shown surpasses the theoretical Si "limit" due to clever device design and advanced processing; on the other hand, the SiC- and GaN-based devices are rather far from the theoretical limit. This illustrates the fact that Si-based devices have essentially reached maturity, while SiC-based devices are still in development and have much unfulfilled potential.

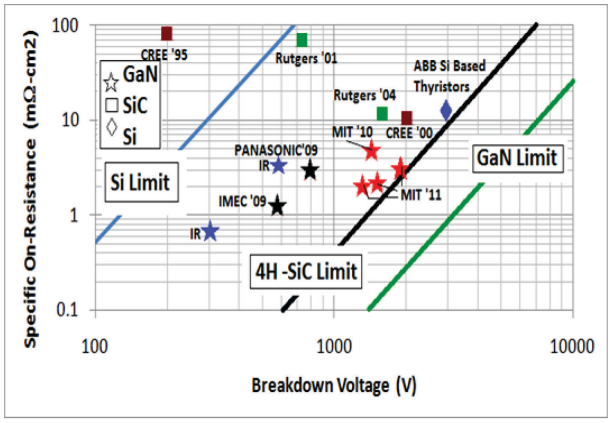

Figure 5. Specific on-state resistance vs. breakdown voltage for bulk material. Theoretical curves for Si, SiC, and GaN are show, as well as various devices reported in the literature.

While SiC has theoretical advantages compared to Si, in practice many hurdles need to be overcome for it to be competitive with Si. Si is an extremely mature technology with a huge industrial base behind it, in addition to over half a century of research; Si (and its native oxide SiO_2) is undoubtedly one of the most-studied materials in history. One factor that is not well understood regarding SiC (or more specifically, the SiC-SiO_2 system; as it is for Si, SiO_2 is the native oxide on SiC, which is one reason that SiC is an attractive material for power electronics) is the stability of the SiC MOSFET threshold voltage V_T. While various definitions of the threshold voltage exist [1], essentially it is the voltage that must be applied to the SiO_2 gate (relative to the drain) in order for a conducting layer of electrons to be induced in the semiconductor. Thus, the threshold voltage is the voltage that must be applied to the gate to induce current flow. Clearly, circuit designers need to know what the threshold voltage is, and it needs to be stable. One consequence of threshold voltage instability is illustrated in Figure 6.

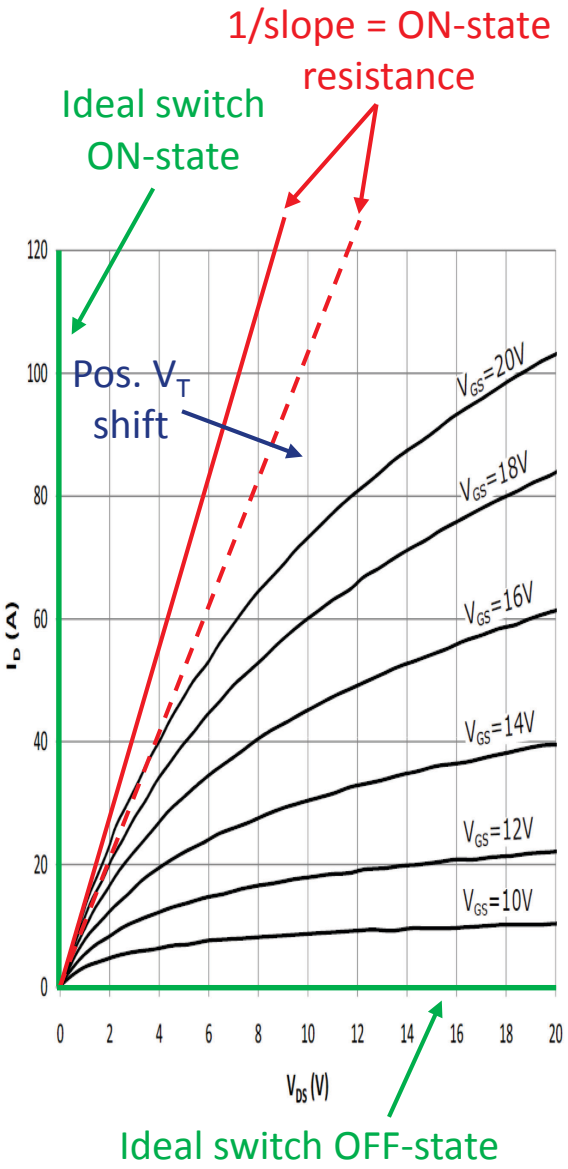

Figure 6. Current-voltage (I_D vs. V_{DS}) curves of a MOSFET. Also shown are ideal switch characteristics, and the effect of a positive shift in threshold voltage on the on-state resistance of the device (device I_D-V_{DS} curves from Cree CFM2012D data sheet).

Drain current (I_D) vs. drain-to-source voltage (V_{DS}) for various values of the gate-to-source voltage (V_{GS}) are shown in the figure for a power MOSFET. Also shown are the desired characteristics of an ideal switch: a short circuit for the ON-state, and an open circuit for the OFF-state. Of course, no real device can achieve these idealizations. For the ON-state, a line tangent to the I_D-V_{DS} curves passing through the origin may be drawn, the inverse of the slope of which is defined as the ON-state resistance R_{ON}. Clearly, the steeper the slope (i.e. the lower the resistance), the closer is the device to the ideal case. Note that the ON-state resistance varies with V_{GS}, since each value of V_{GS} produces a different I_D-V_{DS} curve. For lower values of V_{GS}, R_{ON} is larger (intuitively speaking, for lower values of V_{GS}, the device is less "turned on"). The I-V curves shown are for a fresh device, with a fixed value of the threshold voltage V_T. The charge induced in the semiconductor channel, and hence the current through the device, is in fact dependent not only on V_{GS} but rather on the gate drive $V_{GS} - V_T$ [1]. Thus, a positive shift in V_T with V_{GS} fixed is equivalent to lowering V_{GS} with V_T fixed, and a positive shift in V_T will tend to increase the ON-state resistance of the MOSFET, as illustrated in Figure 6. Increasing the ON-state resistance increases the power loss while the device is turned on, which is obviously undesirable. A SiC-based device subjected to such a V_T shift may in fact be inferior to a comparable Si device if this shift is not taken into account.

Note that a negative V_T shift may also occur. Based on Figure 6, one might conclude that this is a good thing, effectively decreasing R_{ON}. However, a sufficiently large negative V_T shift will tend to increase the leakage current thought the device, since the device may be partially on at zero gate voltage. The threshold voltage may even become negative in such a situation, indicating that a negative voltage would need to be applied to the gate to turn the device off. These effects would tend to increase the power loss experienced during the device's OFF-state. *Generally speaking, any shift in threshold voltage away from the designed value for the device is undesirable.* Circuit designers assume that V_T is fixed at the value specified by the device manufacturer, and any deviation from this value results in decreased power conversion efficiency.

The MOSFET studied is a so-called double diffused (or implanted) MOSFET, or D-MOSFET, so-named because the source region is compensated (i.e. it contains both donors and acceptors; for an n-channel device such as the one examined in this study, the donor concentration is greater than the acceptor concentration). A schematic of a power D-MOSFET is shown below in Figure 7. This is not claimed to represent the details of the specific SiC MOSFET under study (the details of the design and processing are proprietary) but is simply meant to illustrate the general structure of the device.

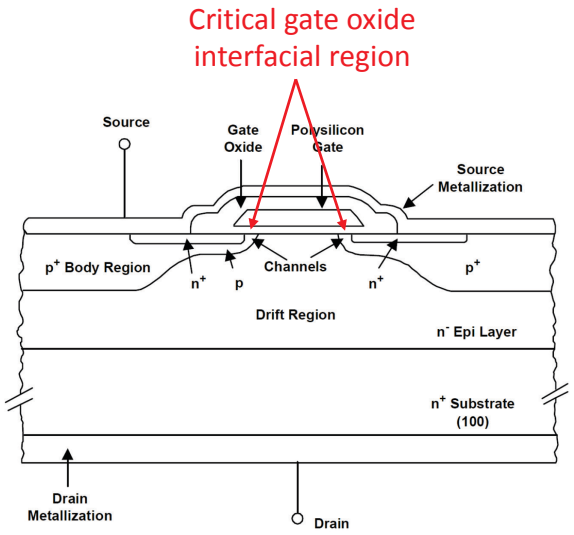

Figure 7. Schematic cross-sectional drawing of power D-MOSFET, illustrating the critical gate oxide interfacial region (figure from International Rectifier, "Power MOSFET Basics").

The D-MOSFET is a vertical device, which means that the charge carriers (electrons) originate in the source, pass through the channel induced by the applied gate voltage, and then pass into the drift region, where they flow vertically from the top of the device to the drain at the bottom of the wafer. The drift region contributes to R_{ON}, and also supports the large voltage applied drain-to-source during the OFF-state. Also indicated in the figure is the gate oxide interface above the channel. This region is critical in determining the V_T of the device; factors such as the oxide thickness and the work function difference between the gate and channel materials influence this. Also of critical importance is the quality of the SiO_2 and the SiO_2/SiC interface. Generally speaking, the oxide and interface quality is much poorer for the SiO_2/SiC system than it is for the SiO_2/Si system. Large amounts of charge may become trapped in the SiO_2 and at the SiO_2/SiC interface during operation, leading to a V_T shift. During ON-state operation, electrons in the channel may be injected into bulk states in the SiO_2 as well as into states at the SiO_2/SiC interface. Negative charge is well-known to cause a positive V_T shift in the MOS system [2], resulting in the effects shown in Figure 6. In the SiO_2/SiC system, this problem is further exacerbated by one of the desirable properties of SiC, namely its wide bandgap. As is illustrated in Figure 8 below, the wide bandgap of SiC results in a small conduction band offset between SiO_2 and SiC. Thus, the band offset is much smaller than in a comparable SiO_2/Si MOS device. Since electron transport over and through the barrier is for some mechanisms thermally activated, the small conduction band offset tends to accelerate charge trapping in the SiO_2 and at the semiconductor-oxide interface at high temperature, resulting in poorer reliability. This is particularly a problem for SiC, since one of its appealing features is that the SiC itself (taking no account of the oxide) is well-suited for making high-temperature devices [3].

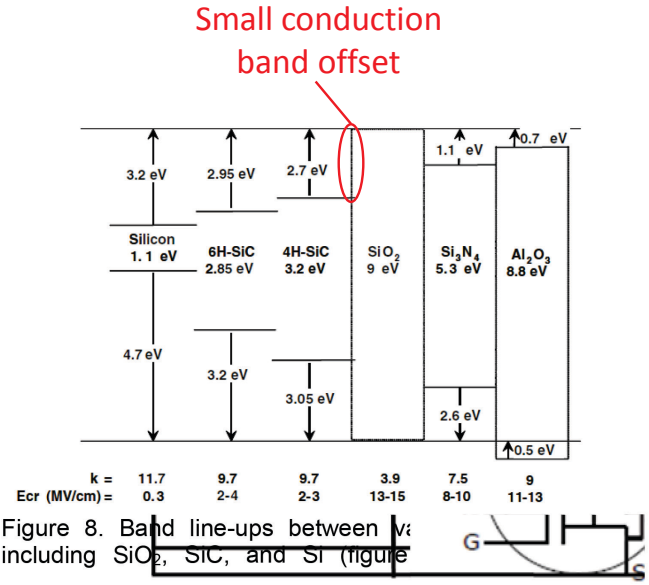

Figure 8. Band line-ups between various materials including SiO_2, SiC, and Si (figure

SiC MOSFETs have traditionally suffered from poor oxide-semiconductor interface quality, which has led to large threshold voltage instability, as noted above [4].

Fortunately, recent process improvements have mitigated this problem to some degree. In particular, the commercially available MOSFET (or in some cases pre-production versions of the same MOSFET, both in a TO-247 plastic package) that we studied showed no signs of degradation when operated below the maximum temperature specified by the manufacturer (125°C). However, significant degradation is evident if the temperature of the device is raised above 125°C, as shown in Figure 9 below.

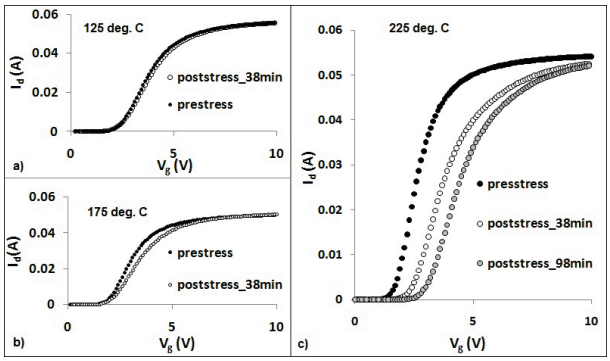

Figure. 9. I_D-V_{GS} characteristics of SiC MOSFET stressed at various temperatures (V_{GS} = +20 V, V_{DS} = 0.1 V).

On the drain current vs. gate voltage curves shown (I_D-V_{GS} for fixed V_{DS}; note that this is a complimentary curve to the type shown in Figure 6), a shift in the sub-threshold portion of the curve is evident after stress at 175°C, and is much more severe after stress at 225°C. Analysis of these curves indicates a large density (on the order of 10^{12} $cm^{-2}eV^{-1}$) of electrically active traps at the SiO_2/SiC interface, as well as the presence of negative charge trapped in the SiO_2 gate [5]. Bias under negative gate polarity (the device could see negative gate pulses during OFF-state operation in a power electronics system) results in degradation consistent with hole injection into the oxide (Figure 10). Varying degrees of degradation have been observed for devices exhibiting nearly identical initial characteristics, and we have identified a characteristic of the integrated free-wheeling diode that correlates with the observed degradation. For both gate stress polarities, the magnitude of threshold voltage shift increases with increasing temperature (Figure 11).

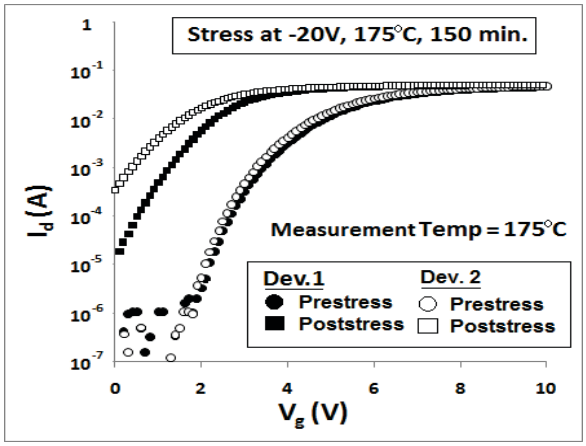

Figure 10. Post-stress degradation in I_D-V_{GS} characteristics (V_{DS} = 0.1 V) of two nominally identical SiC MOSFETs.

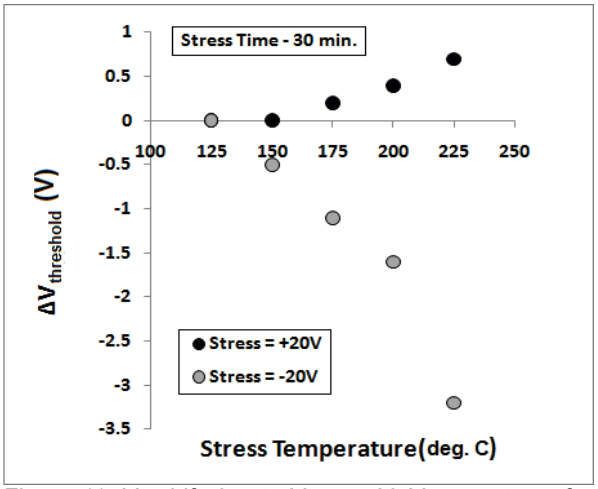

Figure 11. V_T shift due to V_{GS} = ±20 V gate stress for 30 minutes, plotted as a function of temperature. The device is recovered exactly to the initial state at the start of each bias step.

Devices were also stressed under pulsed conditions at room temperature. Pulsed over-current operation (Figure 12a) showed degradation similar to what was observed under high-temperature, positive-V_{GS} DC stress, consistent with electron injection into the oxide. This may be due to transient heating of the device beyond the junction temperature specification. Figure 12b shows the transient current profile for a single switching cycle. The actual switching is preceded by a very high current spike that lasts about 10 μs. This high-current transient is likely a significant factor in device degradation under pulsed over-current conditions, since for the same switching levels (V_{GS} = 20 V, V_{DS} = 8 V), 1 kHz operation produces faster degradation than 1 Hz operation.

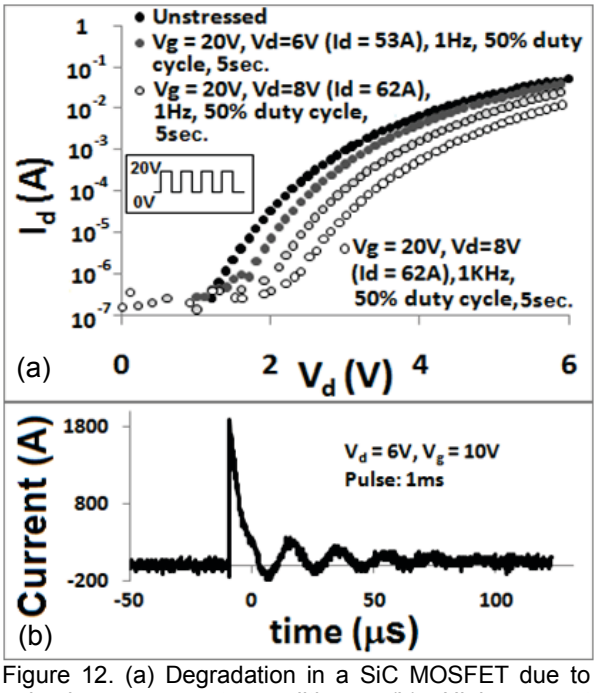

Figure 12. (a) Degradation in a SiC MOSFET due to pulsed over-current conditions. (b) High current switching transient.

The effects of MOSFET device degradation on system availability can potentially be mitigated through Condition Monitoring (CM) and Prognostics and Health Management (PHM). CM consists of monitoring component and/or system characteristics *in situ* to ascertain its health, and to detect anomalies and diagnose problems in order to flag maintenance needs. PHM goes further by not only tracking damage growth, but by also predicting time-to-failure (by comparing the state of the component to previously established reliability models), and by managing subsequent maintenance and operations in such a way to optimize overall system utility against cost. PHM seeks to optimize the trade-off between premature device replacement and disruptive failures. In our scenario, a well-developed method of CM and/or PHM can considerably increase the feasibility of exploiting the superior switching performance of the SiC MOSFET before it reaches the level of technological maturity and reliability of comparable Si-based devices.

We have developed a 16-bit Microchip PIC [6] based system to monitor the characteristics of the device while it is in operation. A current sense circuit uses a resistive network to perform a current-to-voltage conversion and communicates with the microcontroller through an opto-coupler (which is utilized to provide electrical isolation between the microcontroller and the power device). The set-up has a built-in gate control circuit which uses the PWM signal from the controller to provide a variable output to the gate. A prototype circuit was first constructed on a breadboard, which was followed by a more integrated version with all of the circuitry fitting onto a printed circuit board approximately 3”×3” square. The latter version is a first approximation to a board that could be put inside a working power electronics system.

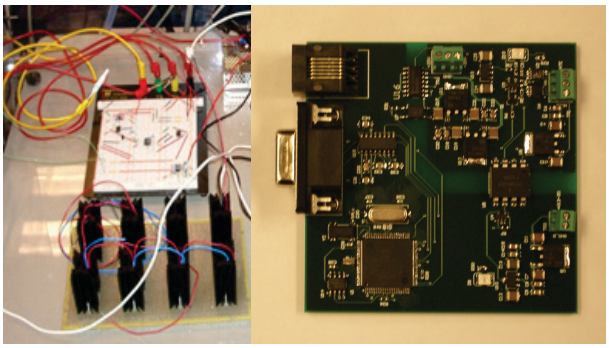

Figure 13. Photographs of CM circuits. Left: Prototype circuit on breadboard. Right: Components integrated onto 3”×3” printed circuit board.

Figure 14 shows the output of our CM set-up resulting from a slow voltage ramp applied to the gate of a SiC MOSFET biased at V_{DS} = 5 V. The output current and threshold voltage match fairly well the device characteristics measured with standard laboratory equipment, showing a successful implementation of the most basic and vital block of the CM module. The noise in the curve is believed to be due to a mismatch between an RC time constant in the circuit and the PWM frequency (this is currently being investigated). Measurements of this curve as the device is stressed, as well efforts to increase the compactness and portability of the system, are currently in progress.

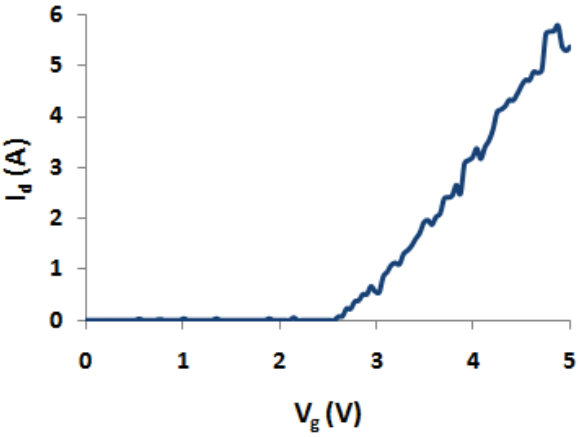

Figure 14. I_D-V_{GS} curve of a SiC MOSFET, biased at V_{DS} = 5 V, measured using our prototype microcontroller-based CM set-up.

In summary, several properties of SiC make it a promising candidate out of which to construct switching devices in grid-level power electronics systems for energy storage and other applications. However, the reliability of real SiC-based devices must be demonstrated before such devices become competitive with well-established Si technology. In particular, the threshold voltage instability of a commercially available SiC MOSFET in a TO-247 plastic package has been studied. While stable up to the manufacturer-rated temperature of 125°C, V_T shifts were observed at higher temperatures under DC stress. Further, pulse gate stress at room temperature produced positive V_T shifts, possibly due to transient heating effects. Finally, we have implemented a prototype condition monitoring circuit based on an inexpensive microcontroller. We are currently working on a second version that has all of the components integrated onto a single PC board. Our condition monitoring circuit is suitable for in-situ prognostics and health management.

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