Large Area Silicon Carbide GTO Thyristor Development
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Abstract
This paper is focused on the development of high voltage (>6 kV), high current (>100 A) Silicon Carbide (SiC) based Gate-Turn-Off (GTO) thyristors. Bipolar devices like GTO thyristors have been shown to offer over 3 orders of magnitude faster switching speeds as compared to Silicon (Si) based bipolar devices. In addition, the possibility of >40 kV devices in SiC may potentially enable high power hardware not presently conceived. A comparison on various power device technologies in Si and SiC shows that SiC GTOs offer high on-state performance in the 6-40 kV range. Calculations presented here also show that a high current density may be obtained from bipolar SiC GTO Thyristors as compared to SiC based MOSFETs and IGBTs. Analysis presented here also shows that the thermal dissipation capability of contemporary device packaging technology needs to be advanced in order to achieve high current densities in these devices. Yield calculations are also presented to understand the limitations towards the achievement of high current levels in these devices. The design of SiC GTOs involves the epitaxial design of voltage blocking layers, 2D-device simulation design, layout design and fabrication sequence design.

Introduction
Advanced high power electronic components enable precise reactive compensation, control, and tuning of all circuits, promising unprecedented increases in the efficiency and cost-effectiveness of electricity infrastructure. For electricity providers, they represent a critical enabling technology for improving power systems performance, offering value added services to customers, and succeeding in a deregulated, competitive marketplace. By increasing AC/DC conversion efficiency, advanced interconnection technologies widen the practical end use of fuel cells, photovoltaics, wind power, batteries, superconducting magnetic storage, adjustable speed drives, and efficient power supplies. The use of SiC GTO technology will offer improvements in power system efficiency and distribution for future Navy combatants. The availability of these devices will also result in the realization of compact high energy weapon systems, railguns and Electro-Magnetic Arrest and Launch Systems (EMALS) for the next generation aircraft carriers.

SiC as a material of choice for SiC GTO Thyristors
A strong interest exists in the energy storage for utility applications for the development of a high voltage, high current, high frequency Silicon Carbide based switch. These applications demand pulse width modulation (PWM) control with an order to magnitude higher power levels at an order of magnitude higher frequency as compared to what is achievable with contemporary power devices. Because SiC devices have the capability to increase the voltage beyond that of Silicon into the 6 kV through 15 kV range (see Figure 1) with much higher switching speed for a given blocking voltage, they provide the revolutionary potential to extend high frequency PWM switching power conversion into the relatively large volume area of utility energy storage power conversion applications. SiC offers advantages for the realization of >6 kV devices because:

- Its wide bandgap (3.2 eV) results in a low intrinsic carrier concentration (~10^5 cm^-3), which theoretically allows the realization of devices with extremely high blocking voltage capability (>40 kV). This property also allows a 3-4X higher junction temperature before the intrinsic carrier concentration reaches the doping level of the voltage blocking layer. In conjunction with a 3X higher thermal conductivity, this allows a wider thermal excursion and a higher power dissipation margin for a power device.
- Its higher breakdown field strength allows the voltage blocking layer to be 10-50X smaller and 10X higher doped than those needed in Si based devices for a similar voltage rating. This translates into correspondingly faster bipolar device like SiC GTO Thyristors.

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As in Si, SiC power devices may be broadly classified into majority carrier devices (e.g., MOSFETs), which primarily rely on drift current during on-state conduction; and minority carrier (or bipolar) devices, which primarily rely on diffusion current during on-state operation. On the other hand, bipolar devices like IGBTs and GTOs offer low forward voltage drops at high current densities. Majority carrier devices are purely resistive with their on-state voltage drop increasing uniformly with the current passing through them. This resistance increases with increasing operating temperature. Bipolar devices have a lower current than MOSFETs until the 3 V barrier is overcome, but then the current level increases dramatically due to diffusion of minority carriers. The locus of the cross-over point between MOSFET, IGBTs and GTO Thyristor shown in Figure 2 proves that highest operating current densities may be obtained in GTOs due to the double injection of carriers in these devices. This is in contrast to IGBTs, which have only a single injecting junction. Gate Turn-Off Thyristors (GTO) offers low conduction losses in >10 kV SiC ratings.

### Material defects, Yield and Current rating considerations

The most prominent defect in SiC is the micropipe, and many commercial wafers are graded according to this specification. SiC suffers from a peculiar material defect called the micropipe. A device made on top of a micropipe suffers from catastrophic breakdown. A micropipe is a thermodynamically stable hollow core screw.
dislocation [1], which shows as a hole through a wafer within a +/-15° off the c-axis of the wafer and is close to 1 μm diameter in size. It has been shown that a SiC device with a micropipe in its active area cannot support significant electric field [1], and hence any significant power level. The micropipe densities in commercial wafers are steadily decreasing as material growth techniques mature, and presently it is possible to purchase wafers with a micropipe density of 5 – 10 cm⁻². However, it is imperative that this ‘killer defect’ be eliminated in the future for the realization of high current power devices. Besides micropipes, there are many material defects commonly observed in present-day SiC, as shown in Figure 3. These defects can be broadly classified into wafer-level defects and epitaxial defects. The yield of devices with the device size is shown in Figure 4.

![Figure 4: The ideal yield of power devices as a function of device area and micropipe density.](image)

One way to achieve high current devices is by operating high-yielding, small devices at high current densities. If devices are capable of operating higher current densities, the current yield obtained can be improved, as shown in Figure 5. This curve shows that even for a 100 Ampere device operating at 350 A/cm², an ideal yield of 75% may be expected. Hence, there is a strong motivation for pursuing bipolar devices like SiC GTO Thyristors, if high current ratings are to be achieved from SiC devices.

![Figure 5: Micropipe defects in SiC require pushing towards higher current density operation in order to obtain high device fabrication yields (per chip).](image)

![Figure 6: Schematic design of a SiC GTO using junction termination extension (JTE) termination used to accomplish >10 kV blocking voltage.](image)
Design of SiC GTO Thyristors
The achievement of high voltage is critically dependent on proper epitaxial design of the low-doped p-type voltage blocking layer. The detailed on-state, switching and doping/spacing parameters must be analyzed using 2D device simulations. Thereafter, layout design needs to be accomplished in order to meet the device specifications required for these devices.

Epitaxial Design
The epitaxial structure plays a key role in determining the NPN and PNP transistor gains that allow a GTO to be latched. The structure of the GTO Thyristors being pursued in this study is shown in Figure 6. The epitaxial design curves for the achievement of >6 kV devices is presented in Figure 7. The ideal breakdown voltage obtainable from a given epitaxial layer thickness and doping provides an optimistic estimate for the doping and thickness of the voltage-blocking epitaxial layer. This curve shows that lower doping in the voltage-blocking p-epitaxial layer leads to higher breakdown voltage, as long as a corresponding increase in epitaxial thickness is also chosen. A 20% over-design is necessary from the doping and thickness considerations.

Figure 7: Ideal breakdown voltage as a function of epitaxial layer thickness and voltage blocking doping level.

2D-Device Simulation Design
2D device simulations are required to analyze the behavior of devices in detail. These simulations allow a designer to quantify the on-state and switching characteristics of a device. Preliminary structure of the SiC GTO Thyristor has been set up as shown in Figure 8. The analysis of the SiC GTO Thyristor under rated current conditions show a high level of current crowding near the Base-Emitter junction of the device, as shown in Figure 9. Such high current density in a portion of the device can lead to high on-state voltage drop due to a localized high current density. This simulation experiment suggests that a shorter Anode length might be more appropriate for the set of device parameters chosen for this condition, in order to mitigate the current crowding in the present design of the GTO Thyristor.
Conclusions
This paper shows objectives and preliminary work performed under this project. The rationale behind pursuing SiC based GTO Thyristor for Energy storage applications is analyzed. Calculations show that SiC GTO thyristors compete very well in the >6 kV device ratings. Analysis presented here also shows that the thermal dissipation capability of contemporary device packaging technology needs to be advanced in order to achieve high current densities in these devices. Yield calculations are also presented to understand the limitations towards the achievement of high current levels in these devices.

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