Ripple Current and Temperature Distribution in Ceramic Capacitors for DC Link Applications

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Introduction

Multi-layer ceramic capacitors (MLCCs) with lead lanthanum zirconium titanate (PLZT) dielectrics are well-suited to the needs of power conversion circuits with modern wide bandgap semiconductor devices.

- Max permittivity at rated DC voltage
- Low parasitic inductance, high ripple current capability
- High operating temperature

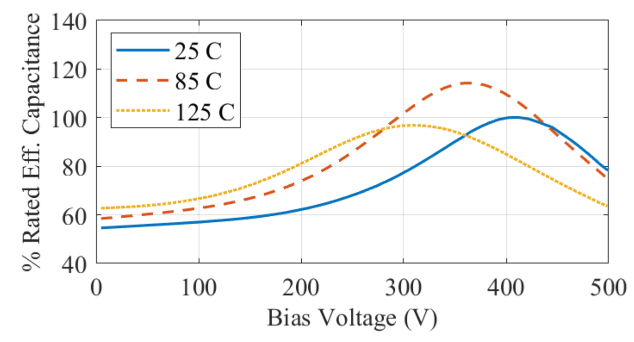
Like all MLCCs, the capacitance of PLZT capacitors is relatively low. A DC link circuit composed of PLZT MLCCs invariably requires multiple parallel elements to build sufficient capacitance.

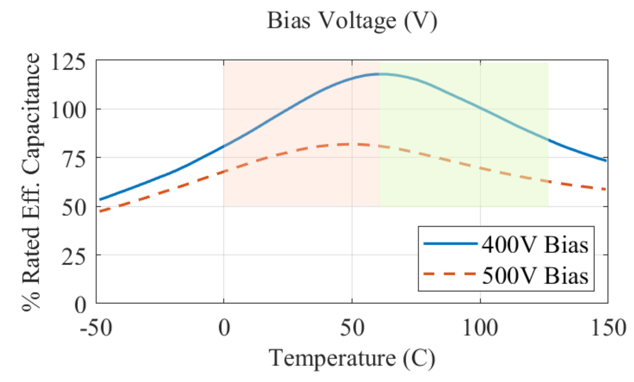
The impedance characteristics of PLZT are complex and depend strongly on DC bias voltage, frequency, and temperature.

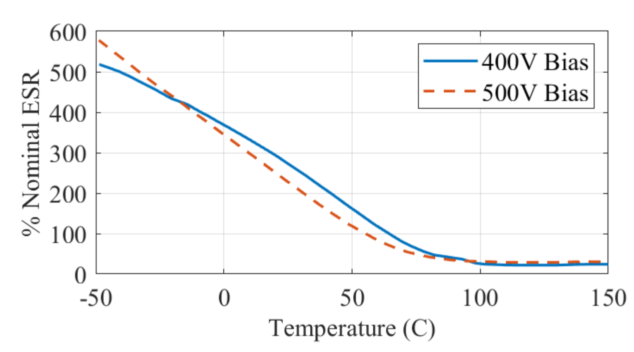
In a DC link circuit, these complex behaviors affect the distribution of high-frequency ripple currents between parallel elements, and ultimately affect the thermal stresses experienced by the components.

Project Objective: Determine the extent to which variations in capacitance with temperature exacerbate or alleviate stresses on PLZT MLCCs in a practical power conversion circuit.

Part Capacitance and Ripple Current Distribution





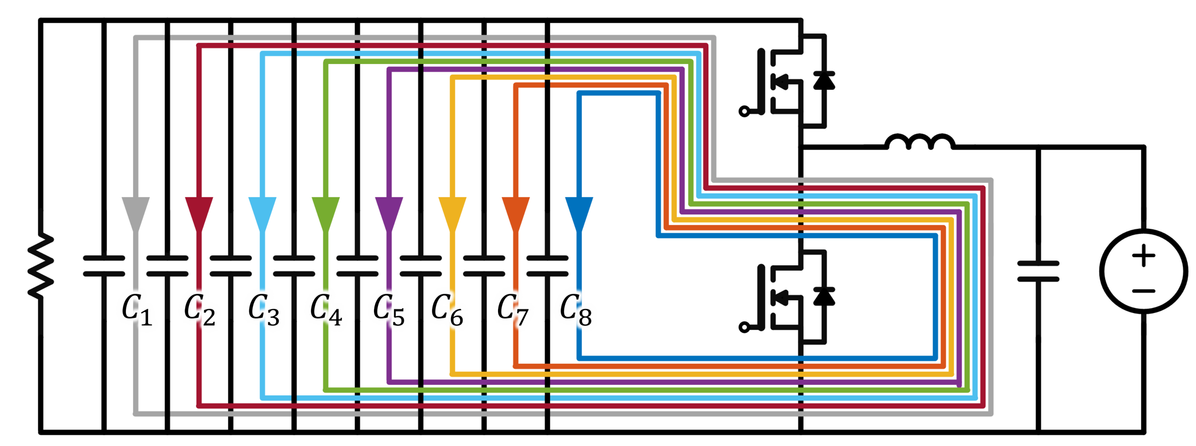


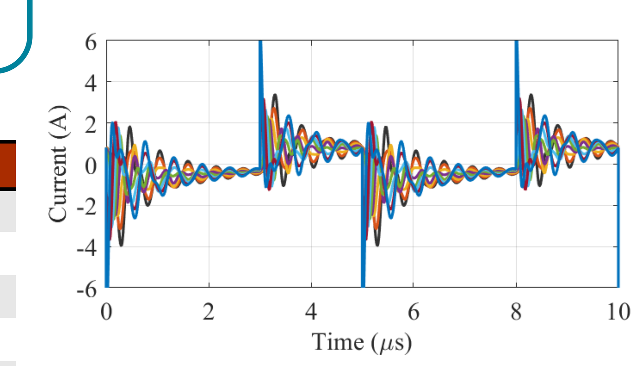
Two distinct regimes at target operating voltage (400V):

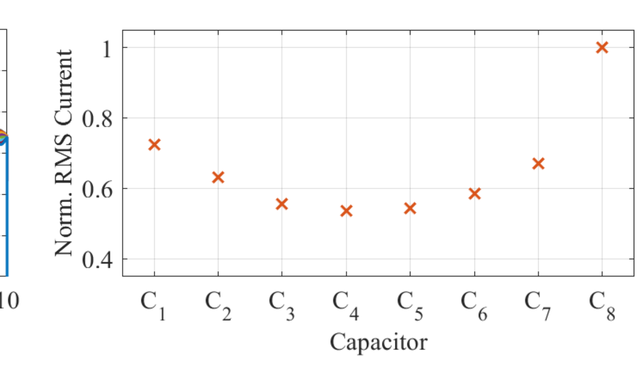
1. Capacitance *increasing* with temperature (T < ~60°C)
2. Capacitance *decreasing* with temperature (T > ~60°C)

ESR is decreasing below ~100°C

Devices Under Test	
Manufacturer	TDK
Product Link	CeraLink
Part Number	B58031I5105M062
Rated Voltage	500V
Rated Capacitance	1μF
Effective Capacitance	0.6μF
Equiv. Series Resistance	12mΩ at 25°C
Equiv. Series Inductance	3nH
Max Operating Temp.	150°C



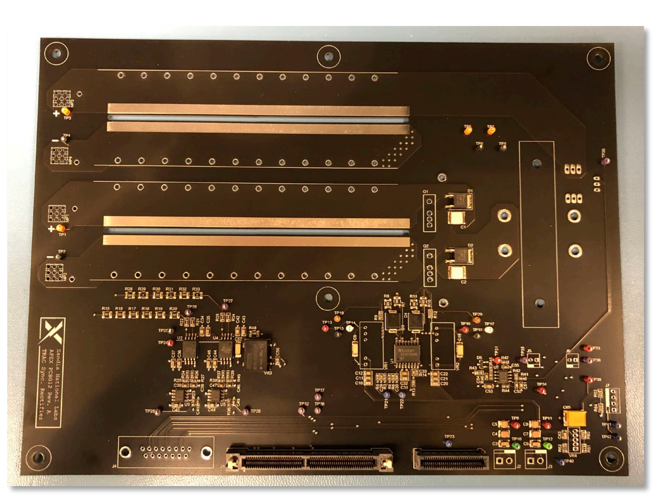


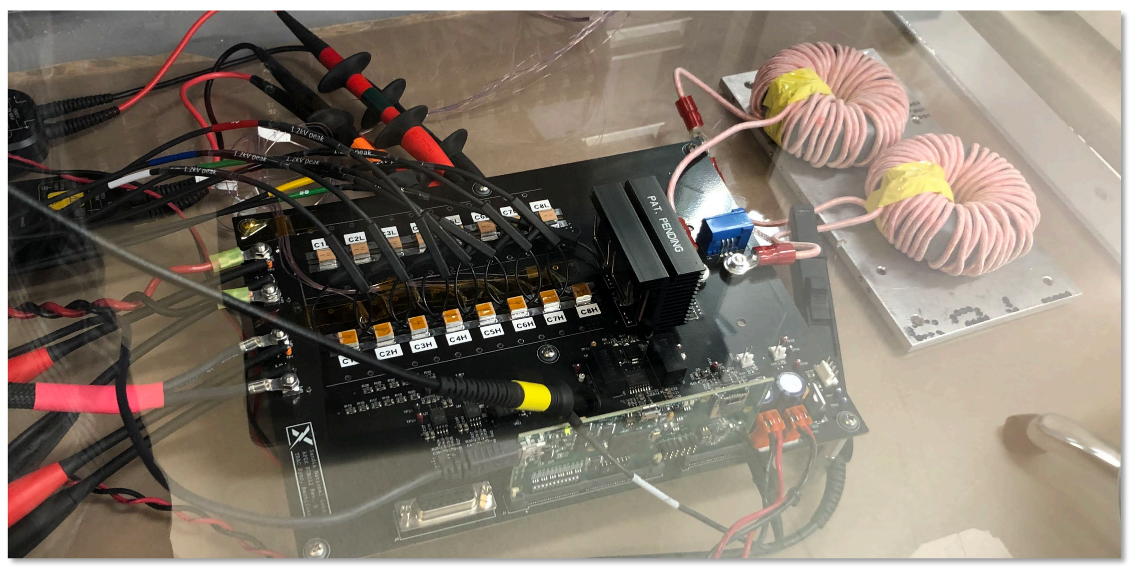


- Circuit parasitics cause unequal ripple current distribution
- Capacitor closest to switching devices takes highest fraction of ripple current, experiences highest internal and external heating
- If capacitor impedance increases significantly with temperature, ripple currents self-balance

Converter Platform

Converter Specifications	
Input Voltage	300V
Output Voltage	500V
Rated Power	4kW
Efficiency	~98%
Switching Frequency	200kHz
Dead Time	500ns
Input Bus Capacitance	24.6μF
Output Bus Capacitance	3.6uF
Boost Inductance	230uH





Converter is designed to support device-level instrumentation.

PCB is slotted beneath DC link, providing clearance for Rogowski coils to encircle individual DC link capacitors.

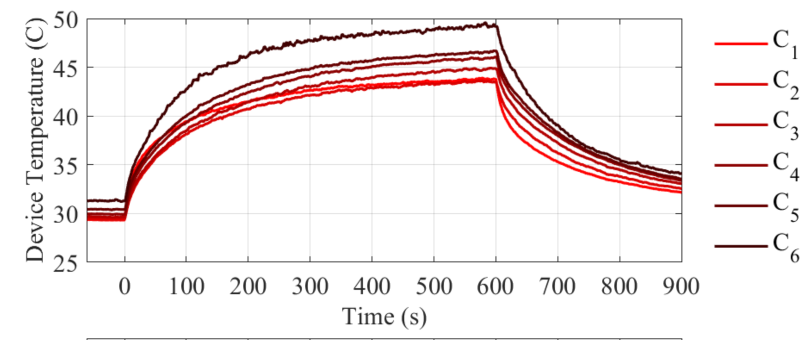
During experiments, converter operates with closed-loop voltage control at high-voltage terminals, regulated by on-board DSP.

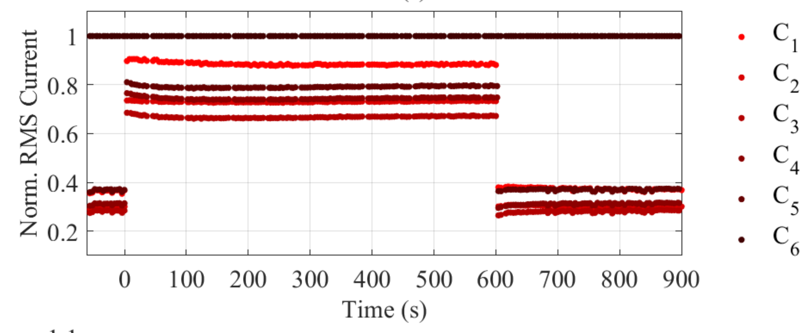
Load is a fixed resistance (10 kΩ) in parallel with programmable current source (Chroma 63224A-1200-960).

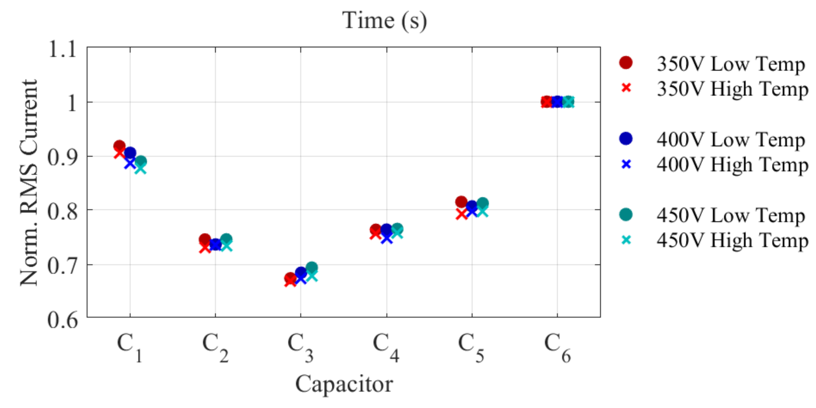
Experimental Results

Experiment Set 1: Unforced Temperature

- No external heating mechanism, temp. rise driven purely by internal heating
- 10 minute excitation period
- 3 output voltage levels: 350V, 400V, 450V
- 2 loading conditions: 5A, 7.5A





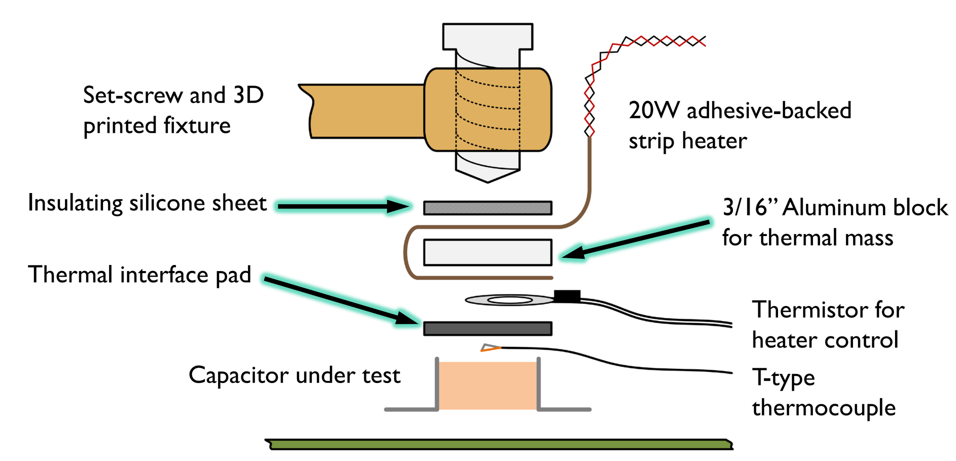


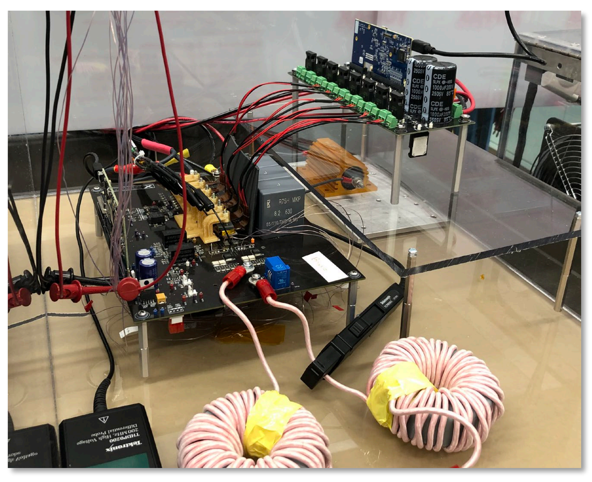
Outcomes:

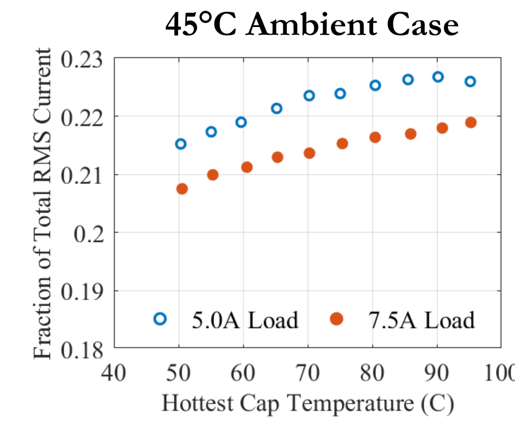
- No significant change in ripple current distribution observed
- Self-heating produces insufficient temperature gradient to cause unequal impedance variation

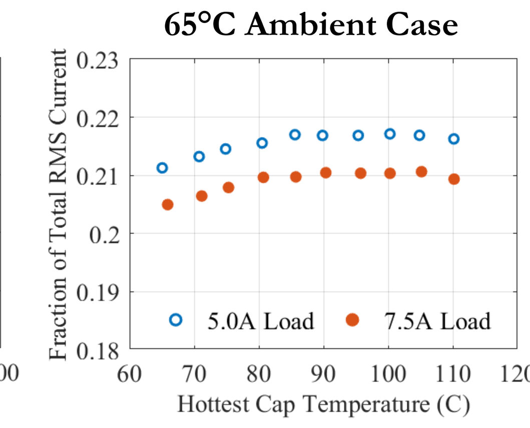
Experiment Set 2: Device Temperatures Controlled via External Heating Mechanism

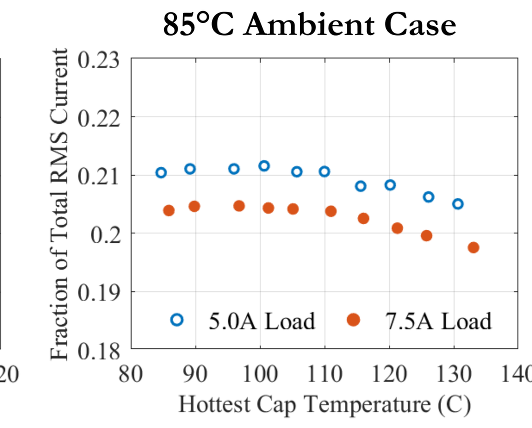
- Heater board and custom heater assemblies provide closed-loop control over capacitor temperatures and enable application of arbitrary heat distribution profiles
- Ripple current distribution measured for same voltage/loading conditions as initial experiments, but with forced temperature emulating hot-spot conditions
- 3 initial "ambient" temperatures considered (45°C, 65°C, 85°C), increasing hot-spot device temperature up to +50°C in 5°C increments











Outcomes:

- Change in part capacitance with temperature affects current through hottest capacitor, but only produces beneficial balancing effect at highest temperature range
- Significant temperature gradient (+50°C change over a few cm) produces only modest improvement to ripple current balancing

Conclusion

Changes in part impedance with temperature were found to alter the distribution of AC ripple currents through parallel branch capacitors of a DC link circuit.

In some cases, especially at the upper end of devices' temperature range, these changes have the desirable effect of reducing ripple current through the hottest capacitor.

However, the difference in temperature required to substantially alter circuit impedance characteristics limits this beneficial balancing effect to a small subset of potential power conversion applications.

References

[1] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters—An Overview," IEEE Trans. on Ind. Appl., vol. 50, no. 5, pp. 3569–3578, 2014.

[2] CeraLink Capacitors Technical Guide," TDK Electronics AG, Munich, Germany, 2017.

[3] K. Klein, E. Hoene, and K.-D. Lang, "Comprehensive AC Performance Analysis of Ceramic Capacitors for DC Link Usage," in PCIM Europe, 2017, pp. 1–7.

[4] S. Coday and R. C. N. Pilawa-Podgurski, "Characterization and Modeling of Ceramic Capacitor Losses Under Large Signal Operating Conditions," IEEE Open J. Power Electron., vol. 4, pp. 24–33, 2023.

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