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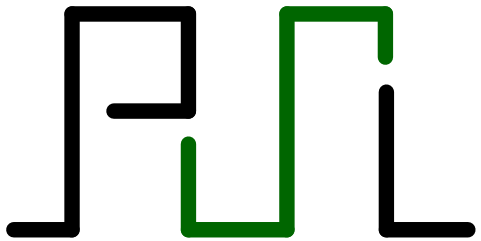

POWER SWITCH LAB

Advancing High Voltage Power Module Packaging: Strategies for Partial Discharge Mitigation

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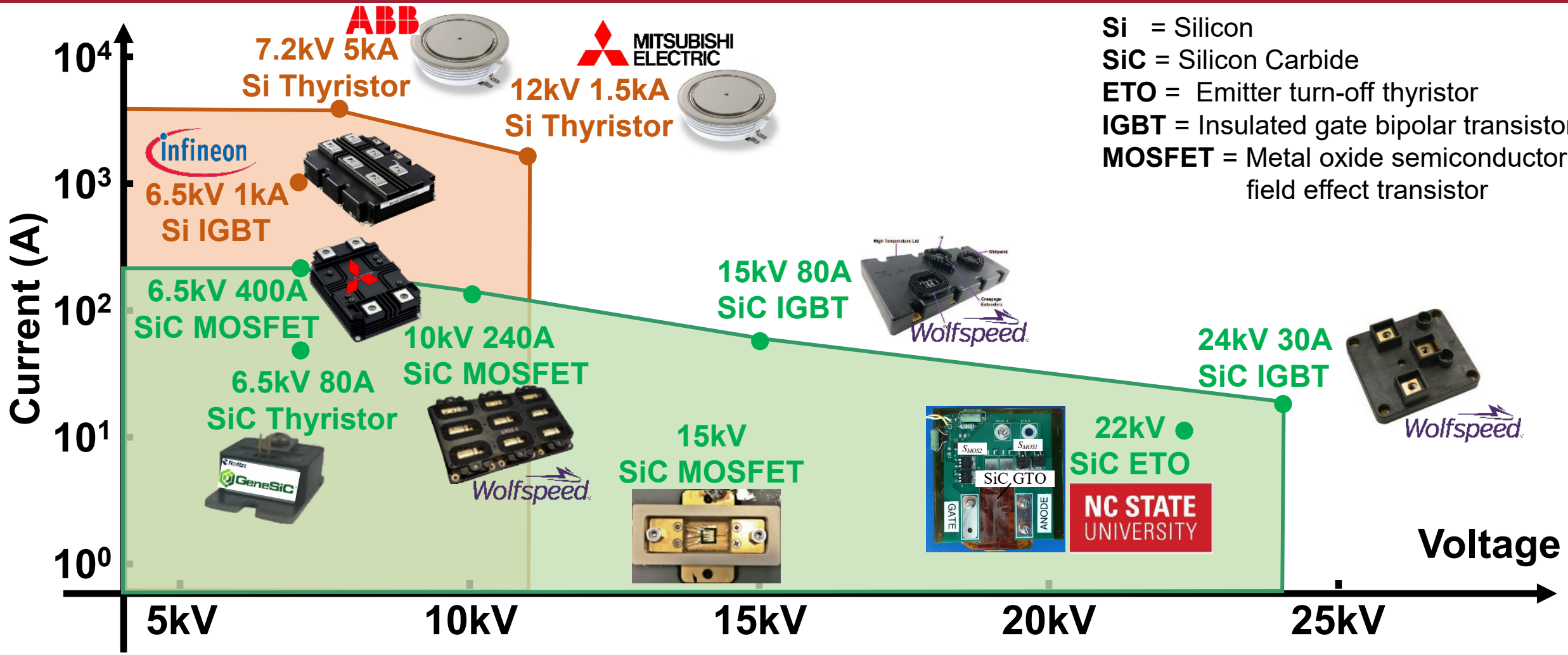
July 16, 2025

2025 Power Electronics & Energy Conversion Workshop

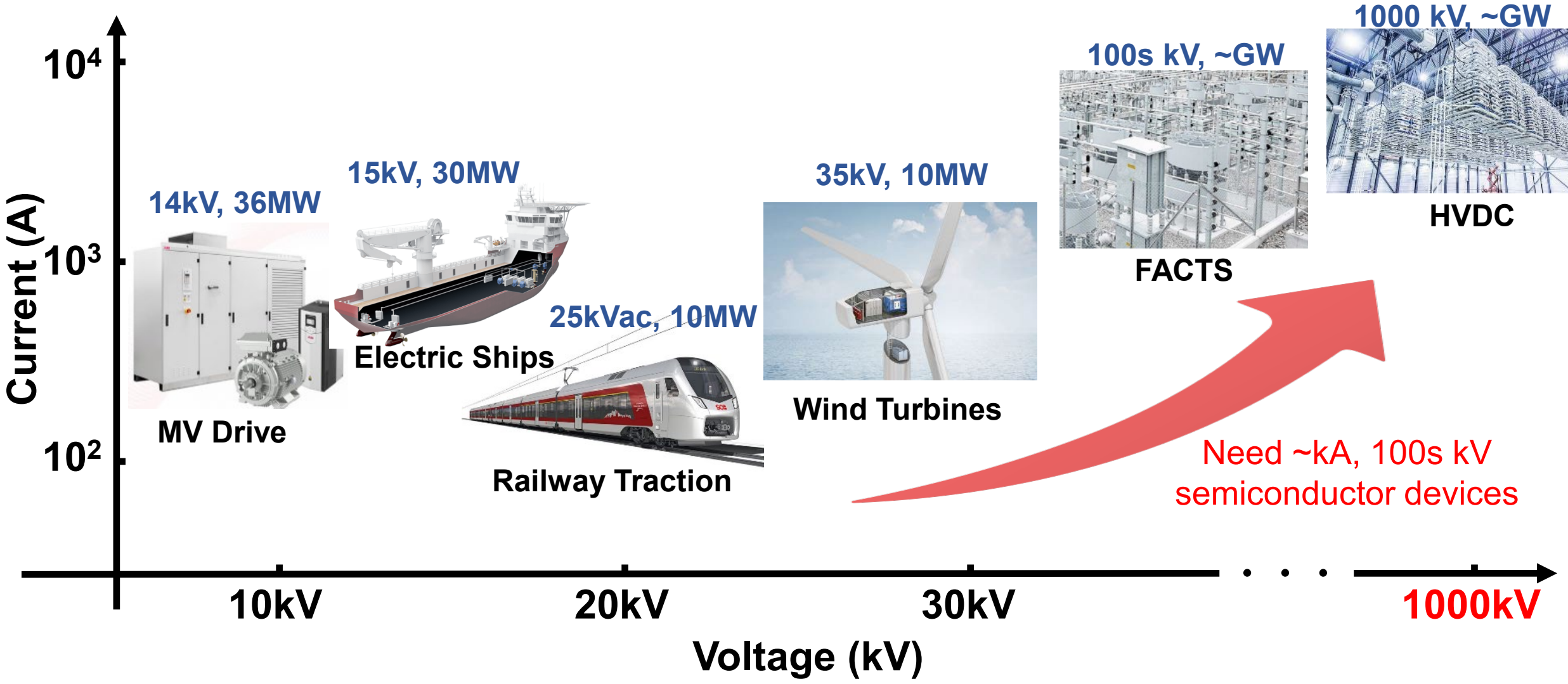
High Voltage Power Devices — Status

Si = Silicon
SiC = Silicon Carbide
ETO = Emitter turn-off thyristor
IGBT = Insulated gate bipolar transistor
MOSFET = Metal oxide semiconductor field effect transistor



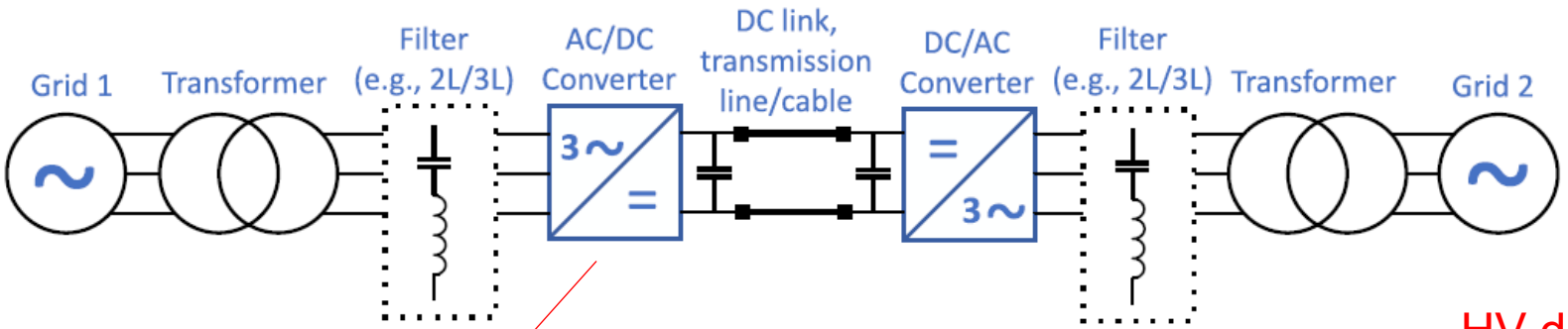
- **Si: Current up to ~kA, but voltage limited to ~10kV**
- **SiC: Voltage up to ~20kV, but current limited to ~ 10s A**

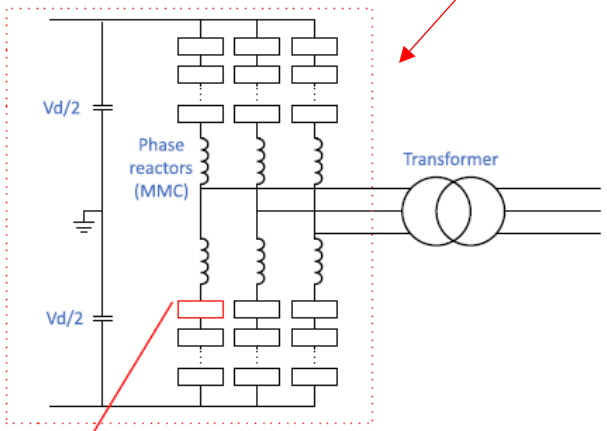
High Voltage Power Devices — Applications

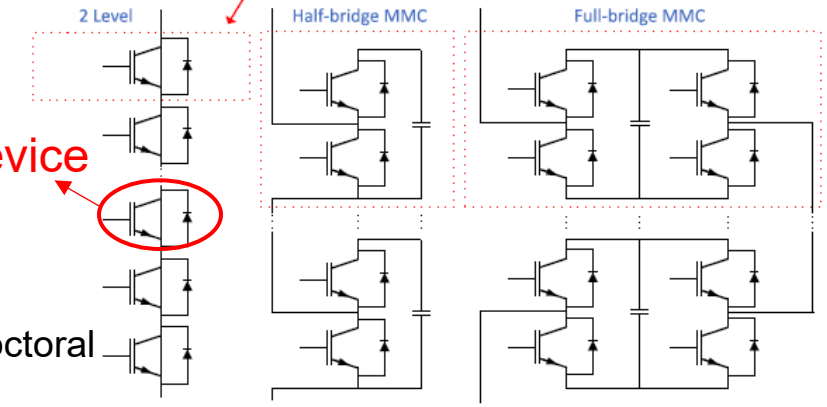


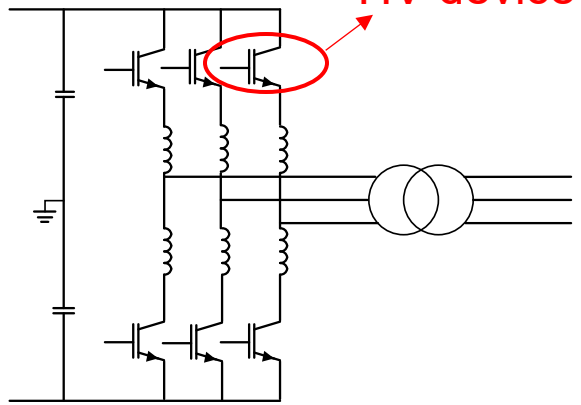
Big Gap between Semiconductor Ratings and Converter Ratings!

Benefits of HV Devices: An HVDC Example









- Simplified circuit realization
- Higher efficiency
- Higher power density
- Higher reliability

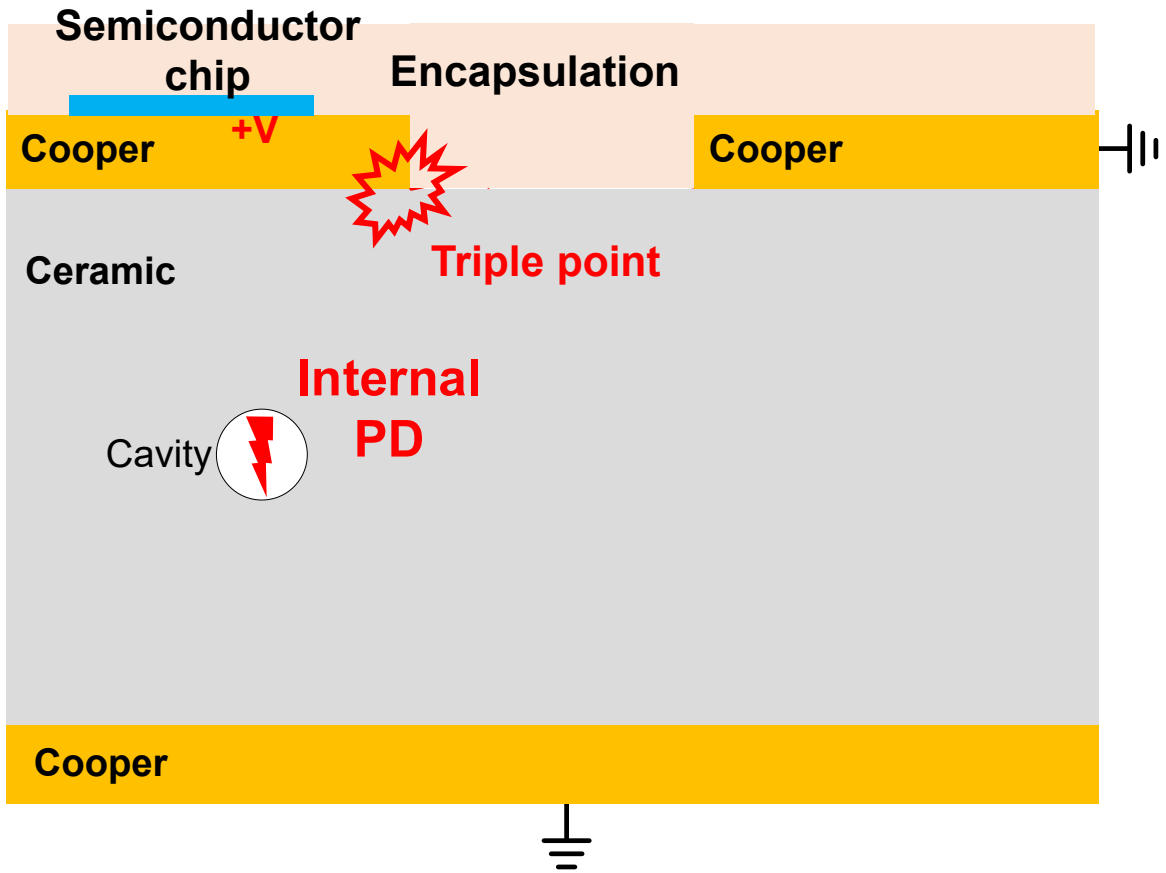
D Johannesson, Doctoral Thesis, KTH, 2021

High Voltage WBG Power Devices — Limitations

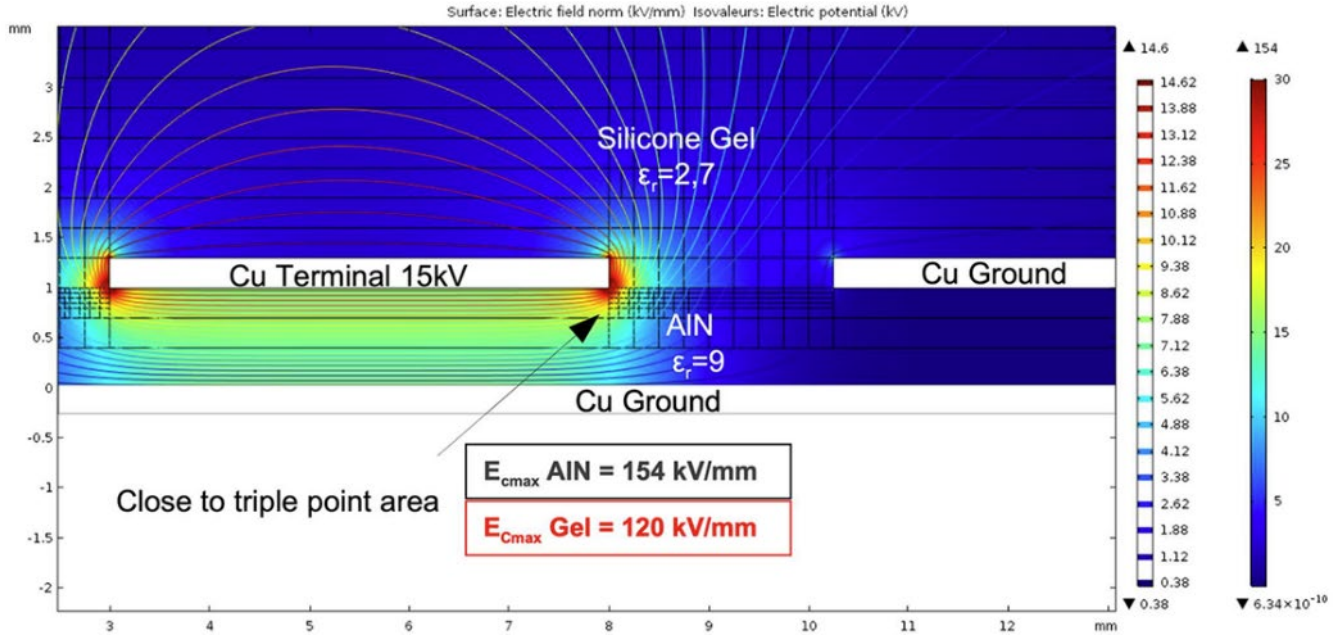
- **Limited Voltage and Current Ratings**
  - Voltage ratings remain low (< 30kV)
  - Current capability restricted to ~10s Amperes
- **Low Commercial Availability**
  - High cost
  - No commercially available devices >10 kV
- **Reliability Concerns**
  - Unstable epitaxial growth
  - Thermal management issues
- **High Voltage Module Packaging Challenges**
  - Voltage insulation - Partial discharge
  - Electromagnetic interference (EMI)

10 kV/ 60 A Half Bridge SiC MOSFET Module Packaged at UA

Partial Discharge in HV Power Module Packaging



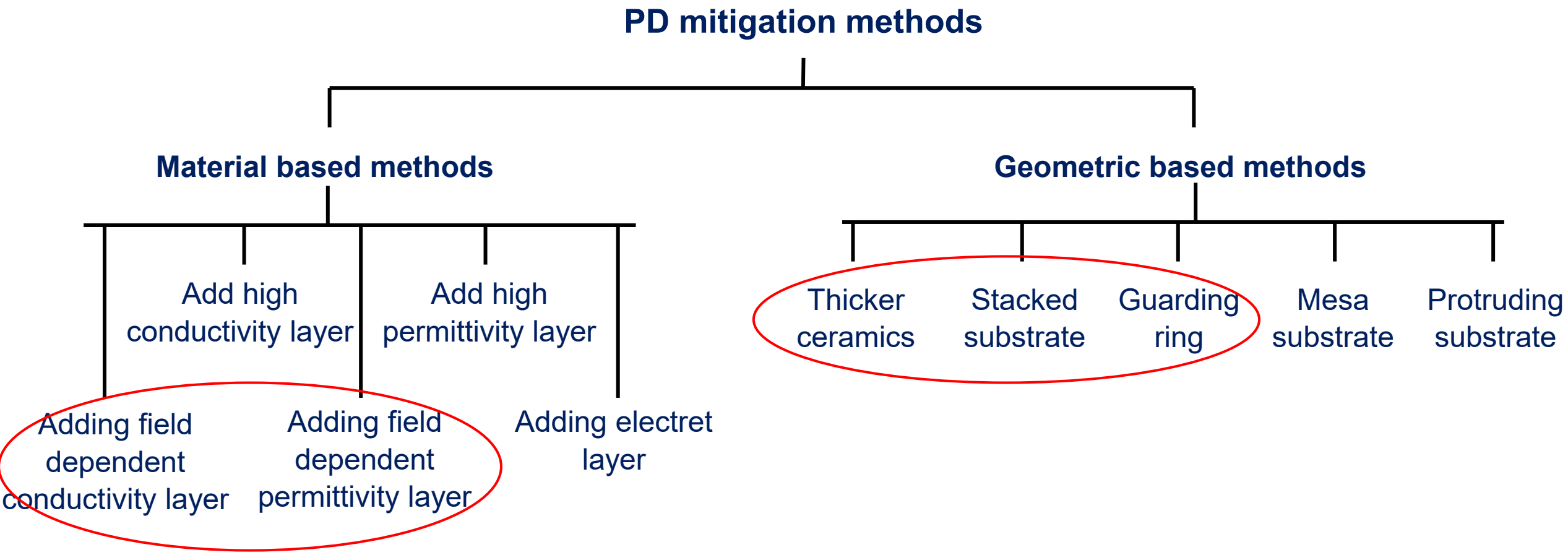
E-field distribution based on FEA simulation



Hourdequin, Eur. Phys. J. Appl. Phys. 87, 20903

- Partial Discharge (PD) is self-sustaining **electron avalanches** that occur in regions of **local** high electric field strength
- PD → accelerated dielectric material aging → device failure

PD Mitigation Techniques In Power Module Packaging



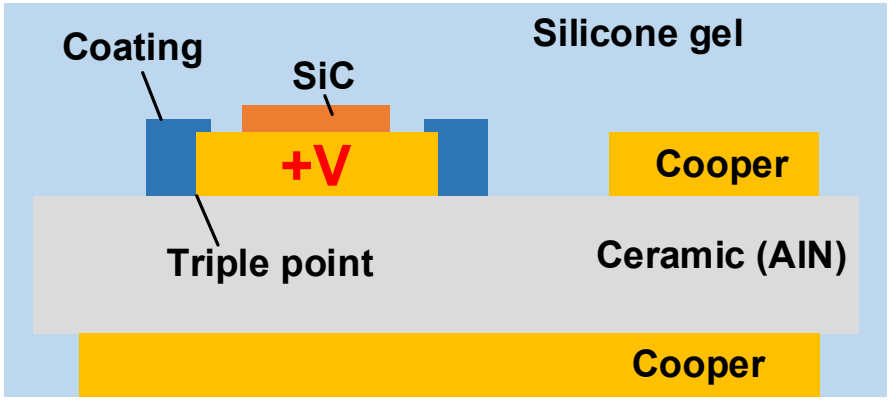
Material Base Method – Modify Encapsulation Conductivity/ Permittivity

Sponsor:
U.S. DEPARTMENT OF ENERGY | Office of Science

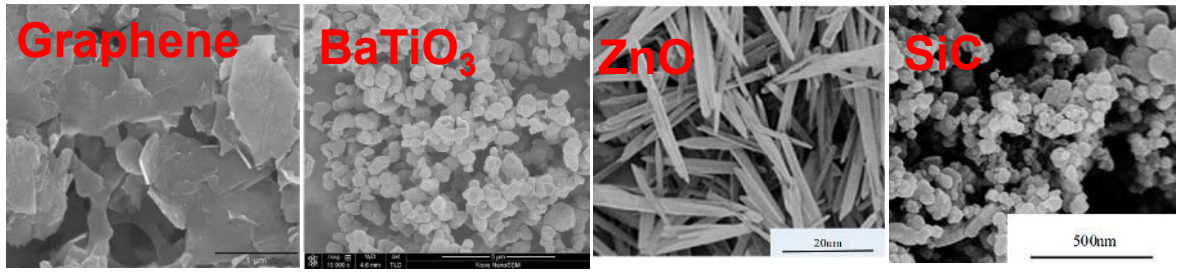
Collaborate with Chemical Engineering Prof. Walters

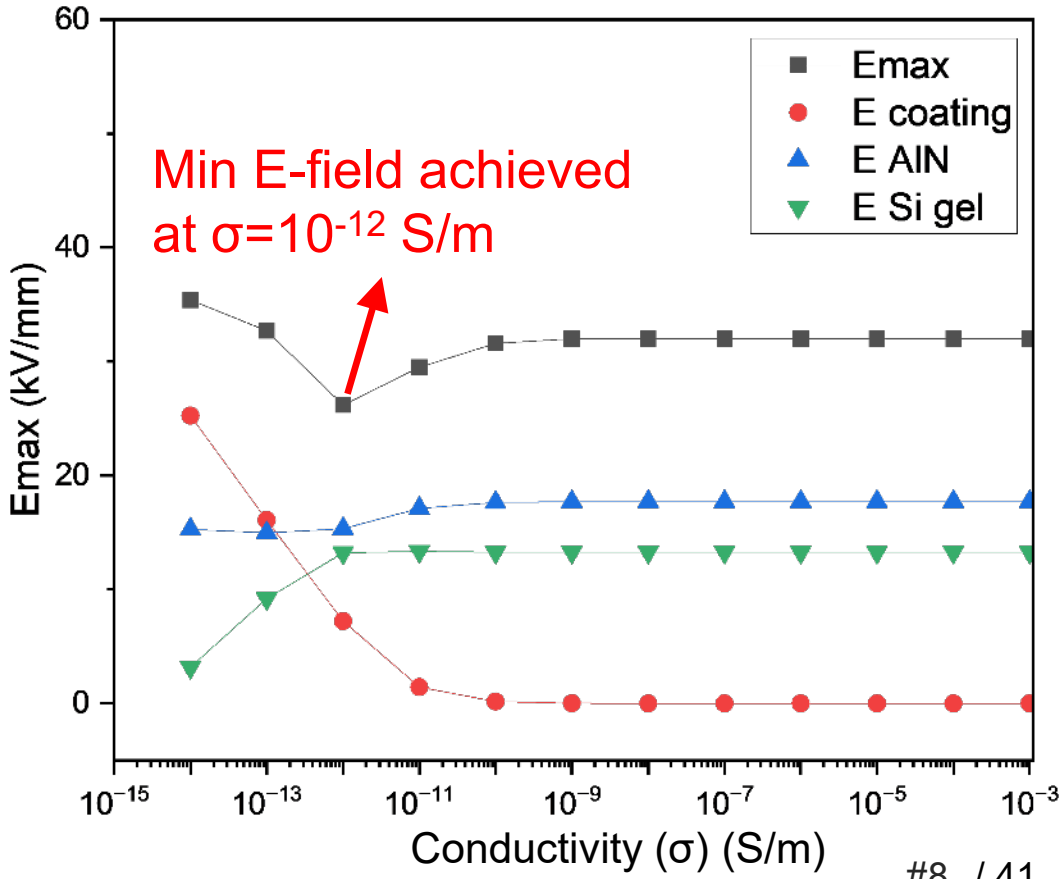
- Modify encapsulation conductivity and/or permittivity
  → Reduced E-field

- Coating layer with modified conductivity or permittivity

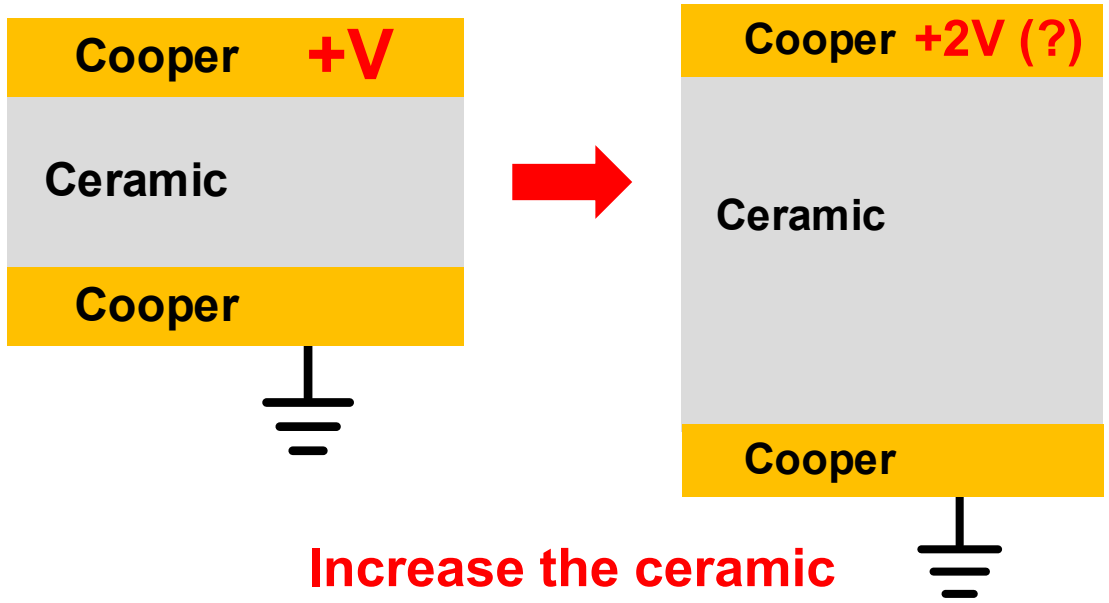


- Nano particles added to the coating layer

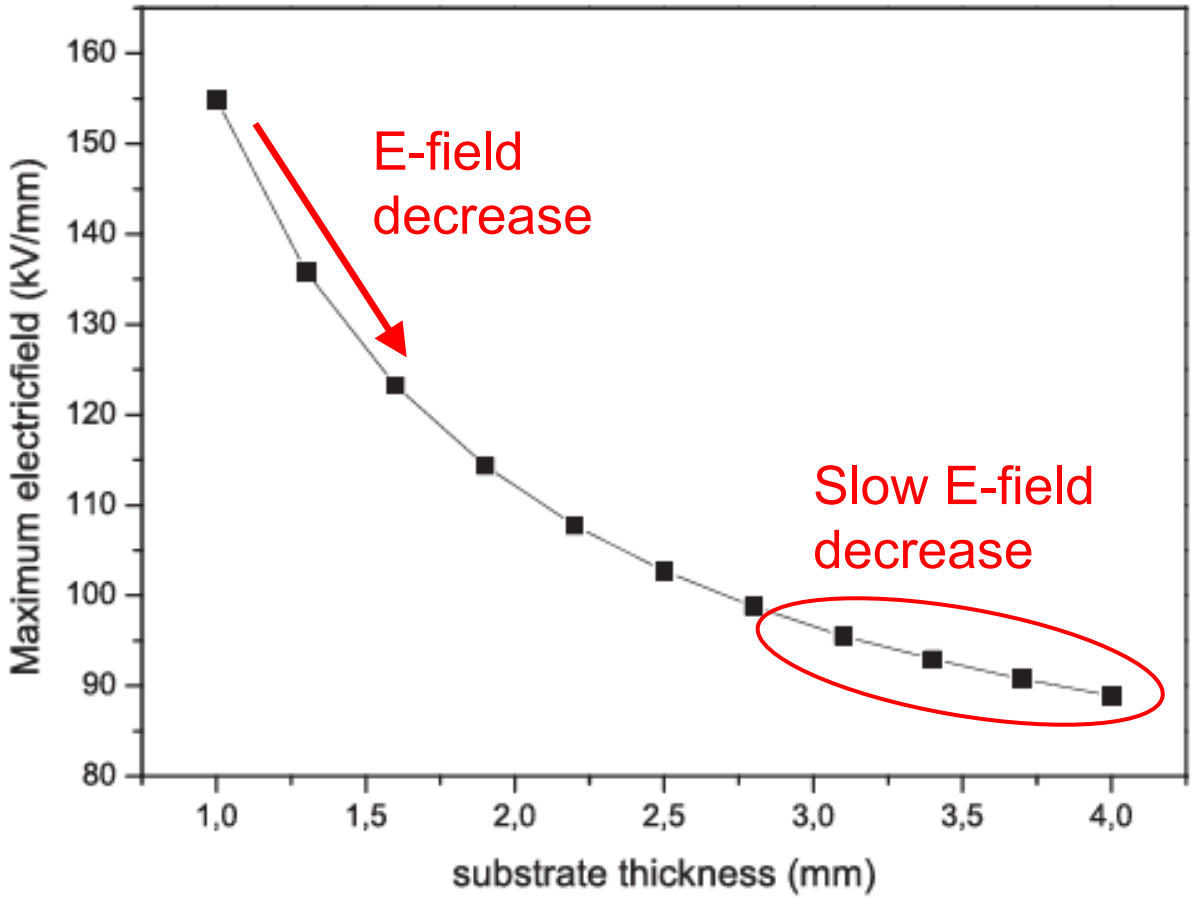




Geometric Design Method #1 – Thicker Substrate



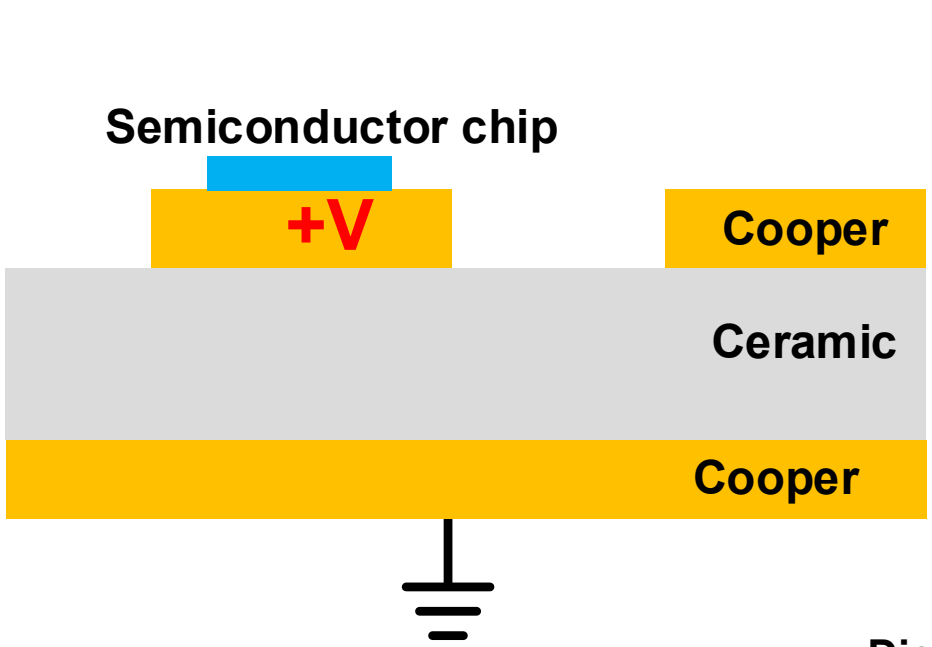
Increase the ceramic layer thickness



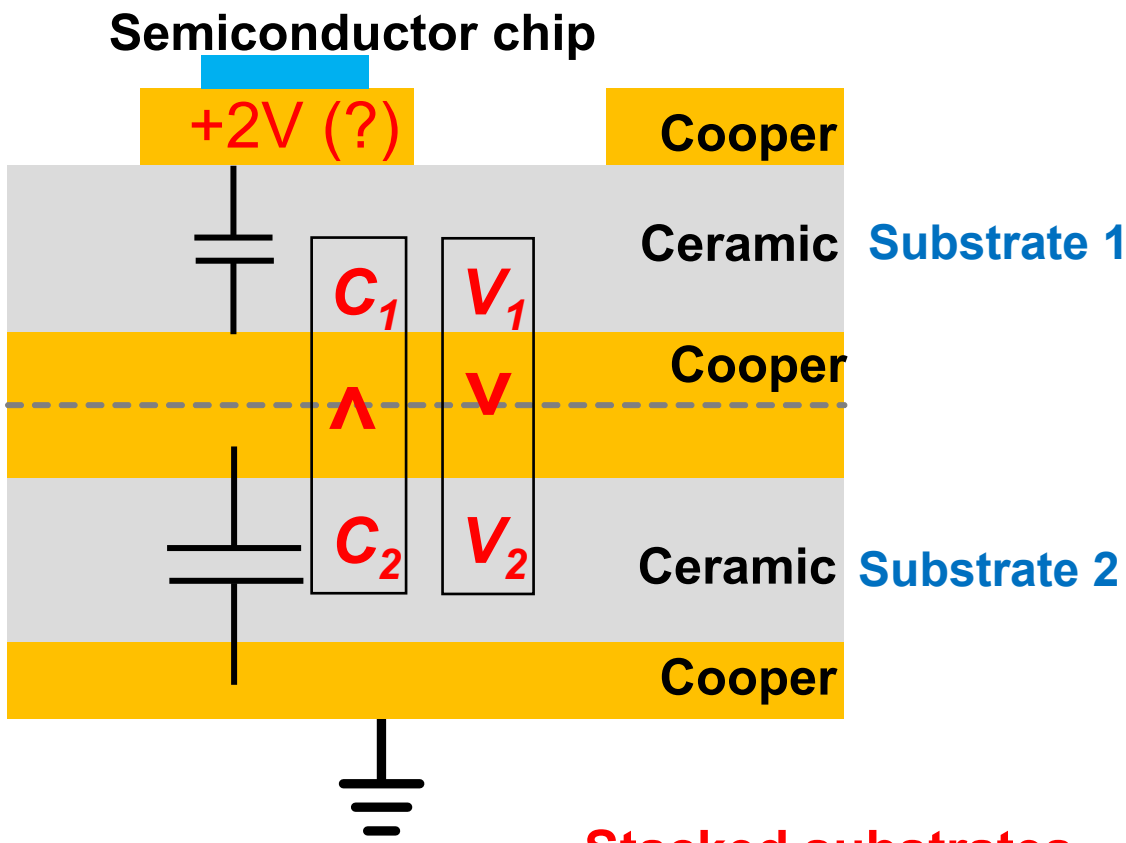
Hourdequin, Eur. Phys. J. Appl. Phys. 87, 20903

- **Increasing ceramic layer thickness → Reduced E-field**
- **E-field trends to stable with thick enough ceramic layer**

Geometric Design Method #2 – Stacked Substrate



Single substrate



Stacked substrates

Dielectric constant

Area

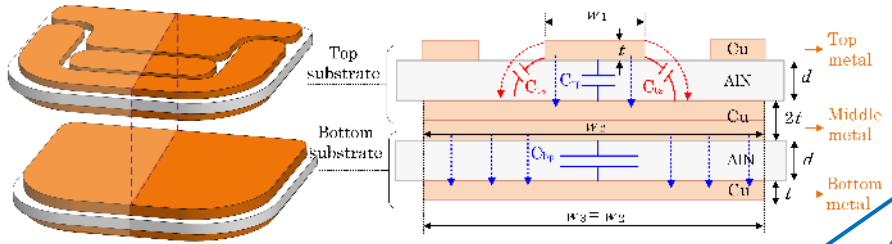
Capacitance $C = \frac{\epsilon_0 A}{d}$

Distance

Directly stacking of substrates fails to reduce electric field due to unbalanced voltage sharing.

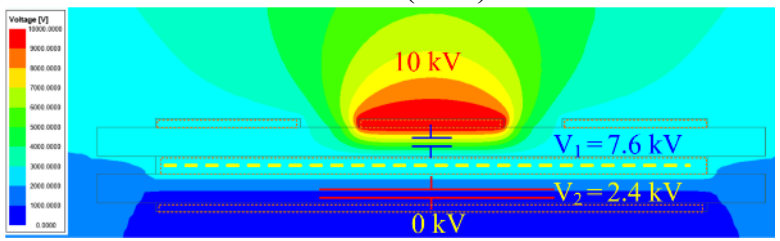
Geometric Design Method #3 – Patterned Mid-layer Stacked Substrate

❖ Solid Middle-layer Stacked Substrates

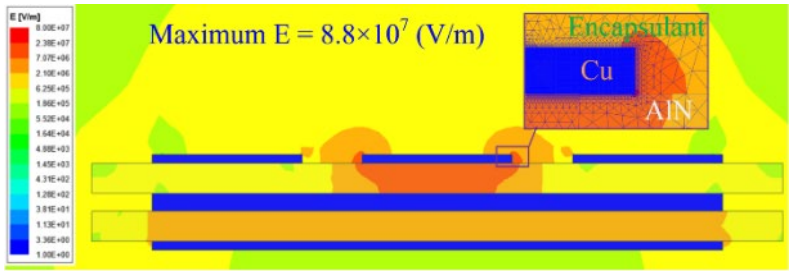


$$\frac{V_{con\_t}}{V_{con\_b}} = \frac{\frac{\varepsilon_{rc}\varepsilon_0 A_{w2}}{d}}{\frac{\varepsilon_{rc}\varepsilon_0 A_{w1}}{d} + 2\int_0^t \frac{2\varepsilon_{rm}\varepsilon_0}{\pi(l+d)}dl} \approx \frac{A_{w2}}{A_{w1}}$$

Conventional

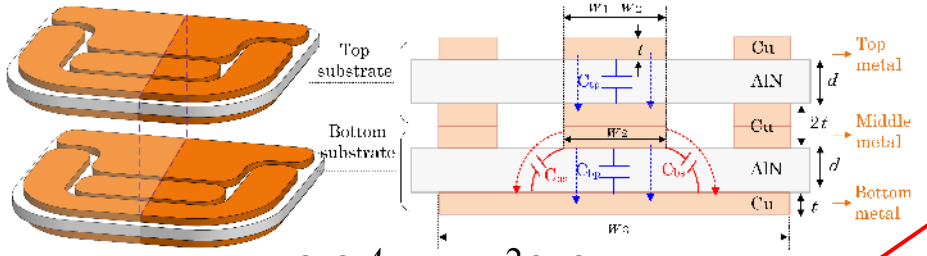


Voltage sharing: top 7.6 kV and bottom 2.4 kV



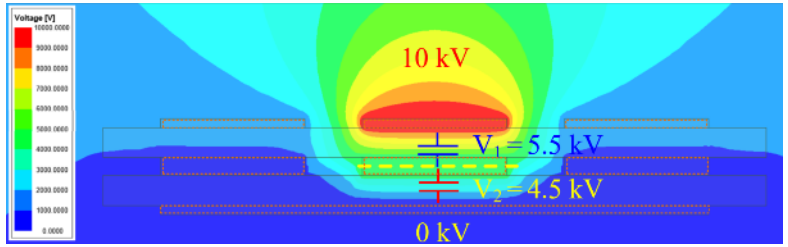
E-field distribution

❖ Patterned Middle-layer Stacked Substrates

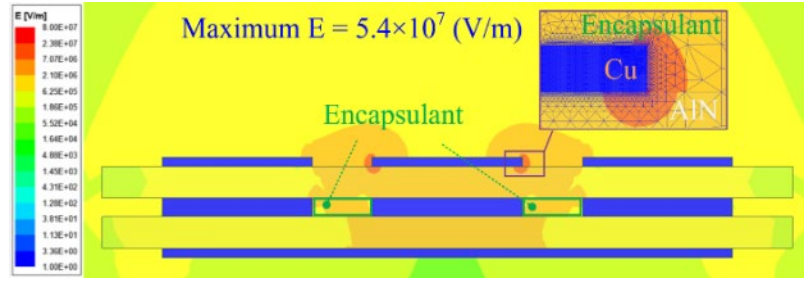


$$\frac{V_{pat\_t}}{V_{pat\_b}} = \frac{\frac{\varepsilon_{rc}\varepsilon_0 A_{w1}}{d} + 2\int_0^t \frac{2\varepsilon_{rm}\varepsilon_0}{\pi(l+d)}dl}{\frac{\varepsilon_{rc}\varepsilon_0 A_{w1}}{d}} \approx 1$$

Proposed



Balanced voltage sharing: top 5.5 kV and bottom 4.5 kV.



Electric field distribution **E-field reduction 38.6%**

Patterned mid-layer → balanced voltage sharing between two stacked substrates

Summary and Future Work

- Material based PD mitigation methods
  - Easy to apply
  - Effective in E-field reduction
- Geometric PD mitigation methods
  - More complicated to fabricate
  - Achieves more effective E-field reduction

- Future research topics
  - More advanced PD mitigation methods
  - PD modeling in encapsulation materials
  - PD online detection and lifetime prediction
  - …

Thank you!