



| Inverter-dominated Transmission Systems – Protection and Stability

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Operator challenges with high renewable integration

Power Balance

Generation meets load

Power Transfer

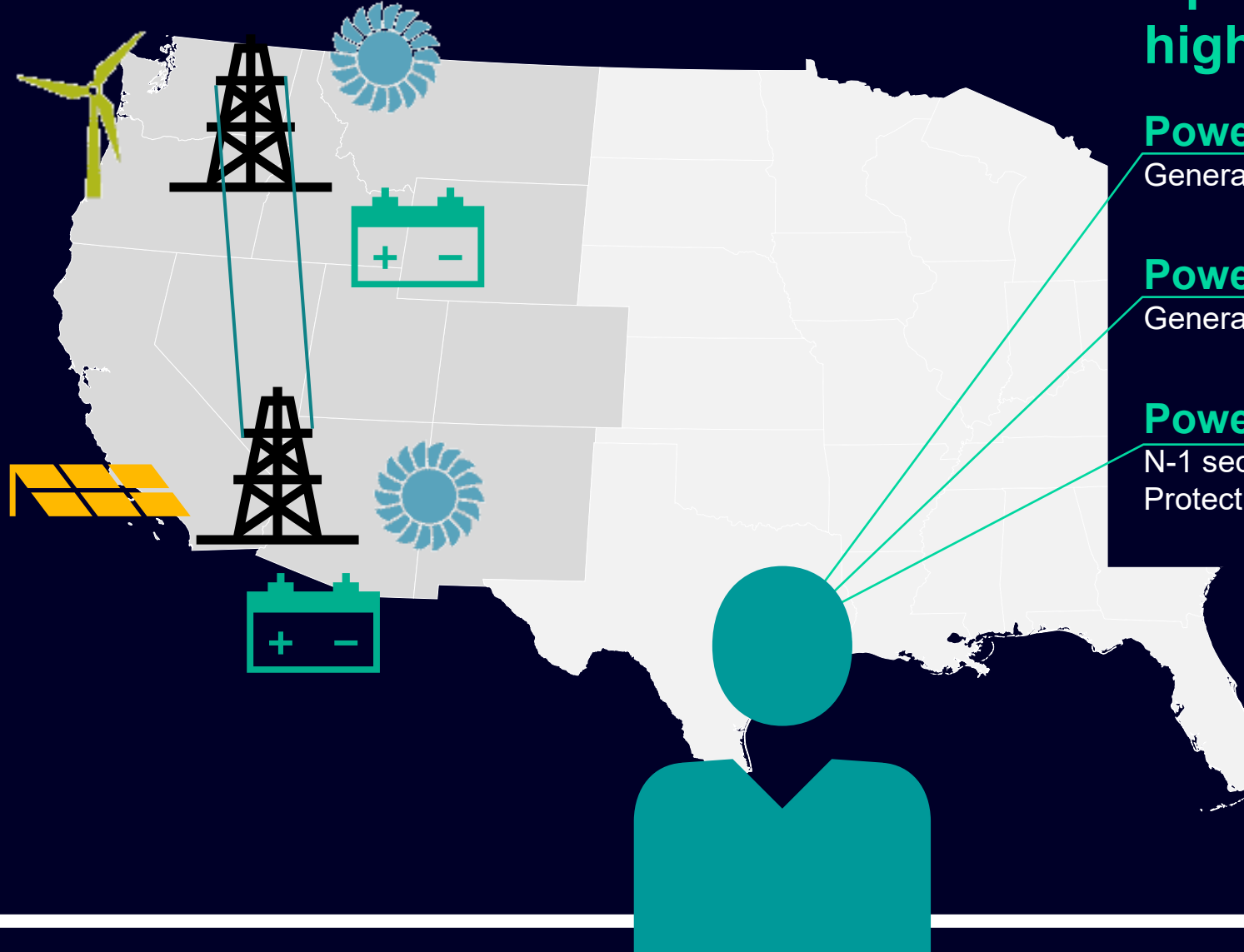
Generation far from load

Power System Stability

N-1 security

Protection schemes

Focus today



Protection of IBR-dominated transmission systems is a widely open R&D space

Gap analysis has been published by Siemens Technology, Sandia National Lab, and EPRI

<https://energy.sandia.gov/wordpress/wp-content/uploads/2024/05/SandReport-CP-gap-analysis-for-IBRs-and-protection-devices.pdf>

20+ Expert interviews

- Utilities
- Consultants
- Vendors
- National labs
- Academia

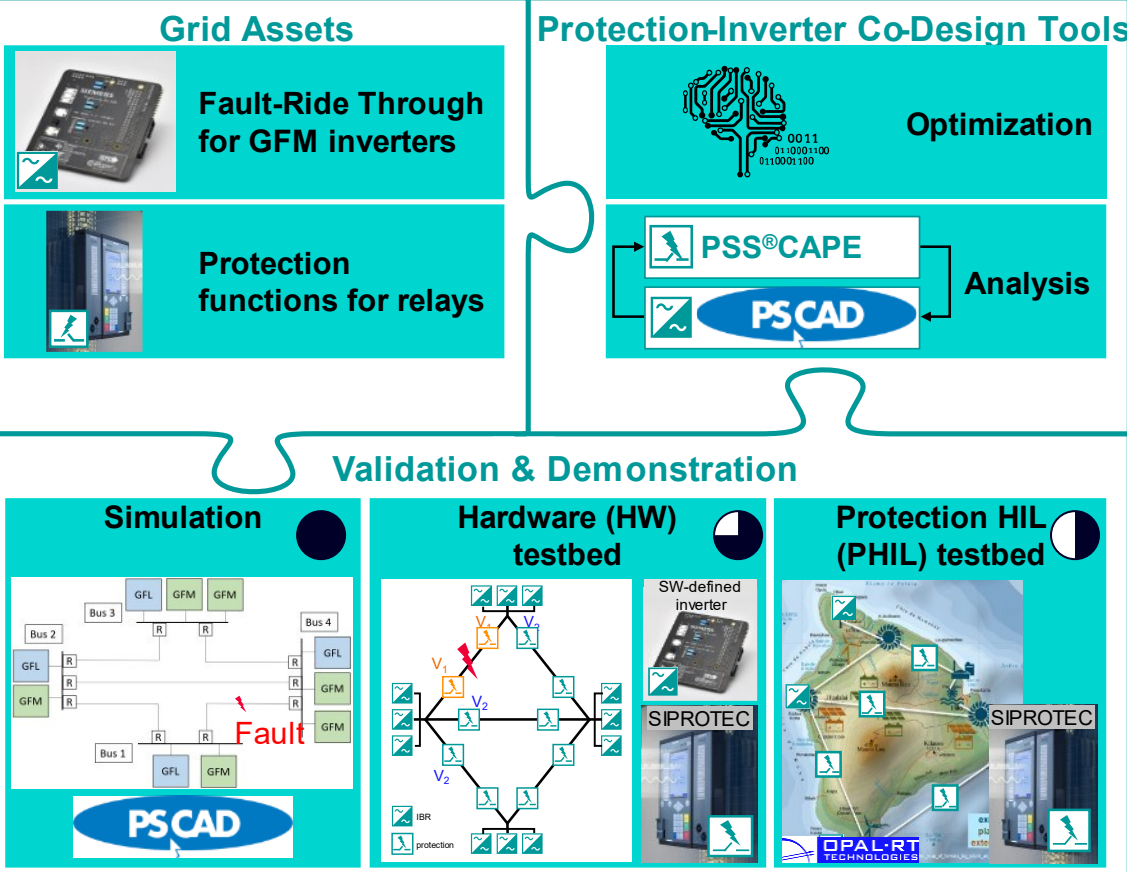
Available Literature

- FRT for GFL IBR
- FRT for *single* GFM IBR

Challenges

- **Non-sinusoidal** fault currents
- **Oscillations** after fault clearance
- **Vendor proprietary FRT** functions
- No system-level protection analysis
- Standards focus on GFL
- **White spot in the community**

PICO: Protection-Inverter Co-Design



IBR: Inverter-based Resource; FRT: Fault-Ride Through; GFM: Grid-Forming; GFL: Grid-Following; HIL: Hardware-in-the-Loop; C&P: Control and Protection

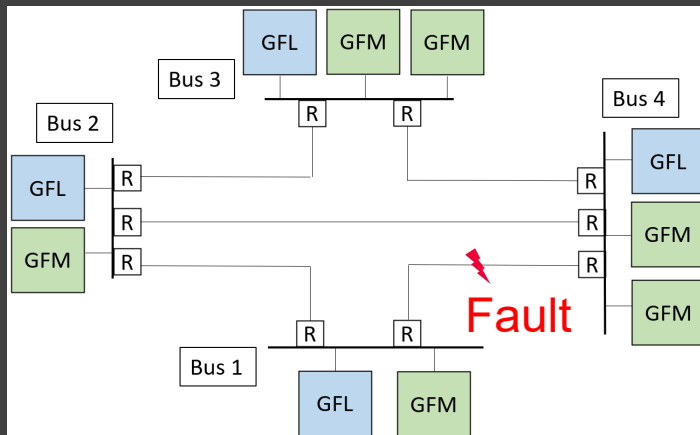


We are evaluating candidate FRT and PF functions in testbeds of increasing complexity

Focus today

● Analysis in Simulation

- PSCAD
- Generic IBR models



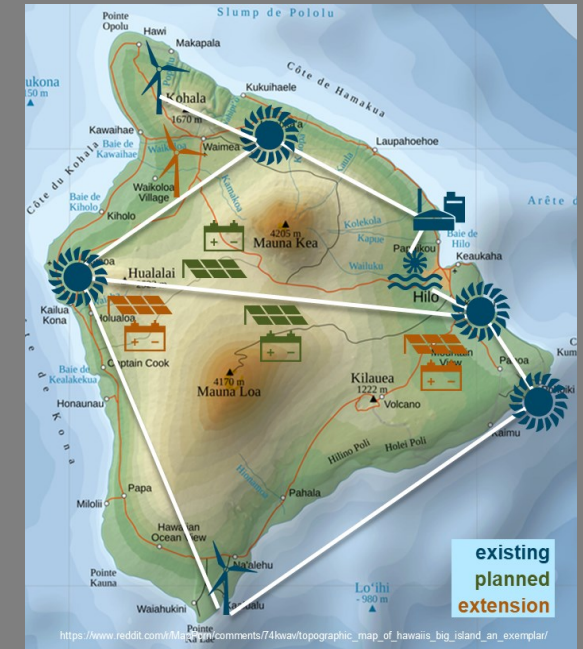
Analysis in HW testbed

- 10x 5kW, 400V IBR
- 6x Siprotec relays



Analysis in PHIL testbed

- OPAL-RT
- Siprotec



IBR: Inverter-based Resource; PHIL: Protection Hardware-in-the-loop;
FRT: Fault-Ride Through; PF: Protection Function

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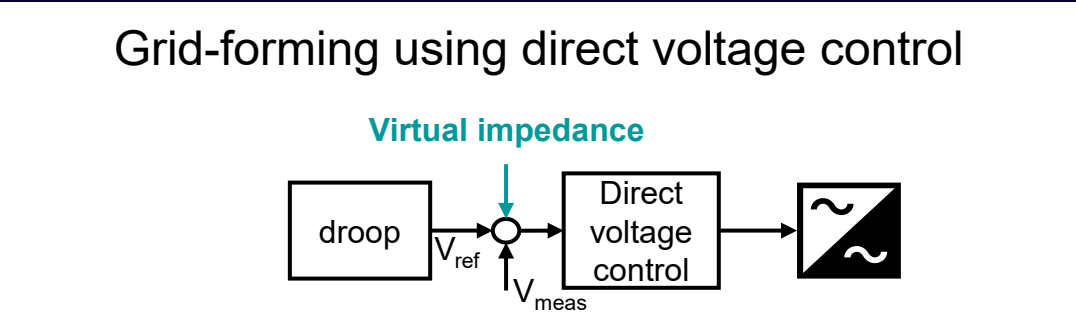
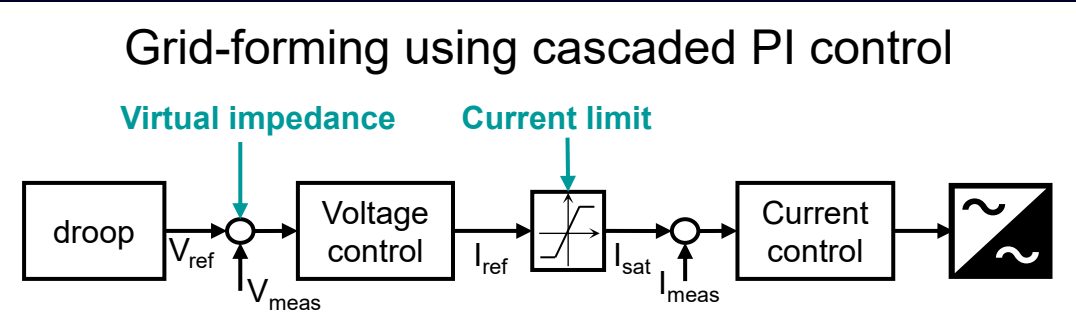
OPAL-RT
TECHNOLOGIES



**Hawaiian
Electric**

**SIEMENS**

We evaluate different Fault-Ride Through (FRT) functions for Grid-forming (GFM) Inverters



	Current limit	Virtual impedance
FRT1	+	-
FRT2	-	+
FRT3	+	+
FRT4	-	+

Fault-Ride Through 1-3 reduce fault currents in cascaded PI Grid-forming controllers using current limiter, virtual impedance, and a combination of both

1 Current saturation (FRT1)

1a Prioritizes active or reactive currents via P,Q priorities

1b For asymmetrical faults, $I_{1,lim} = I_{max}$ and $I_{2,lim} = 0$

2 Virtual impedance (FRT2)

2a Increase virtual impedance until current below limit

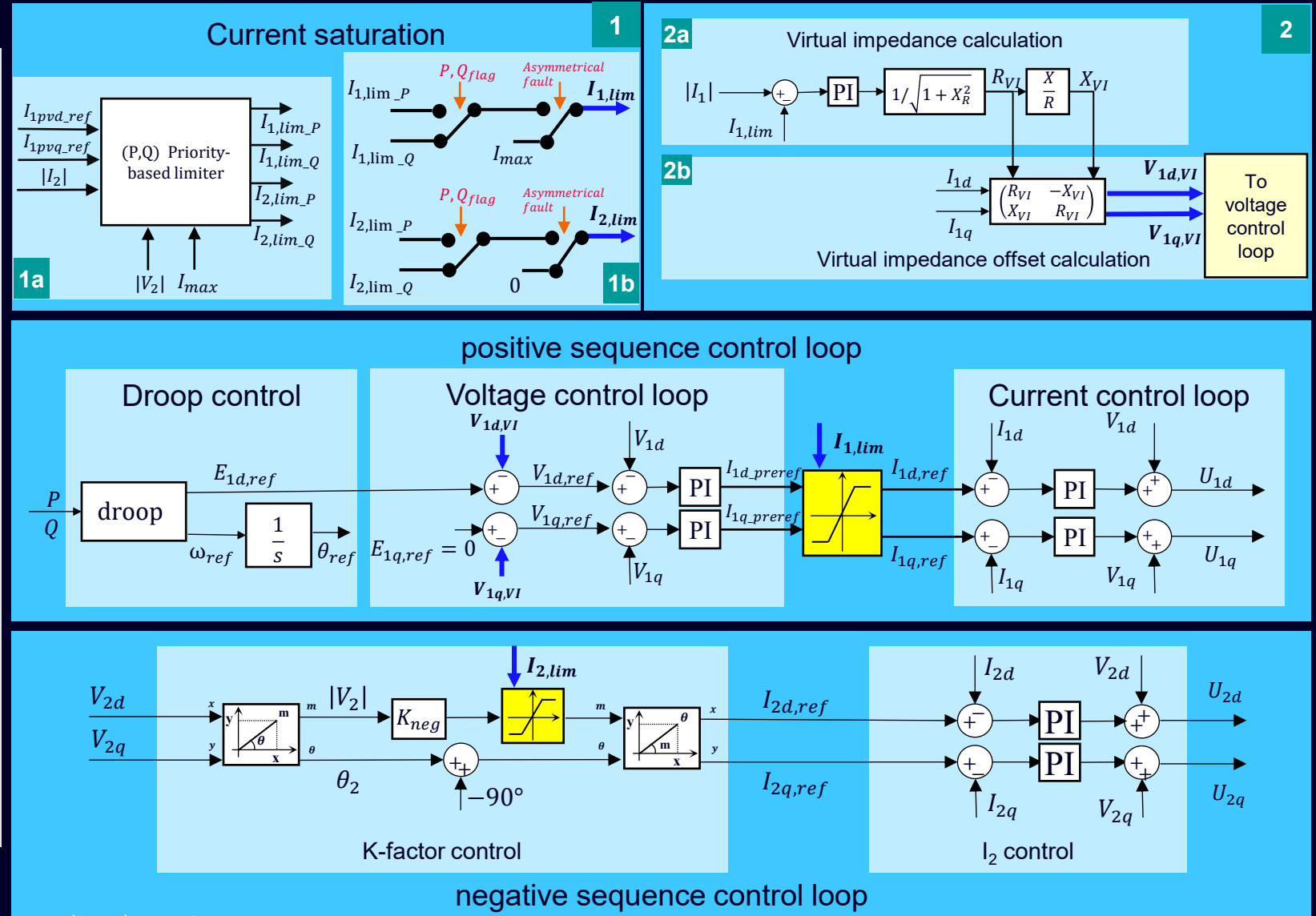
2b Calculate voltage offset due to virtual impedance

3 Hybrid (FRT3)

- Combines FRT1 and FRT2

Negative sequence FRT

- K-factor control
- Always active for negative sequence



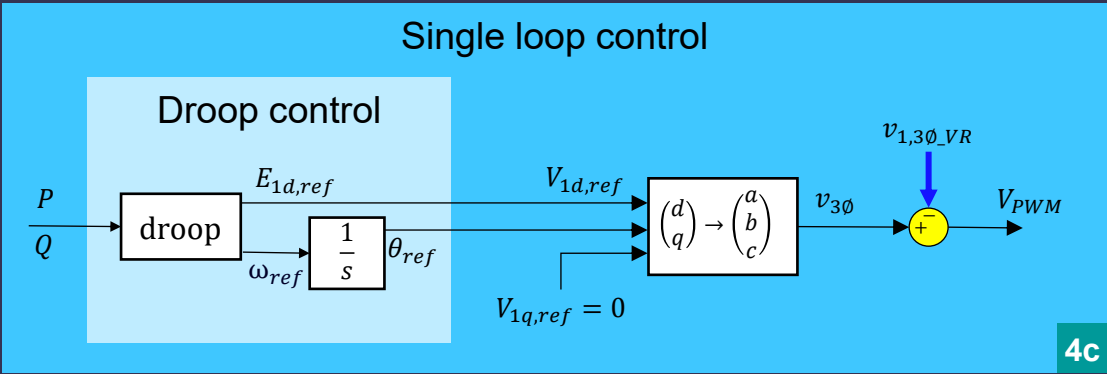
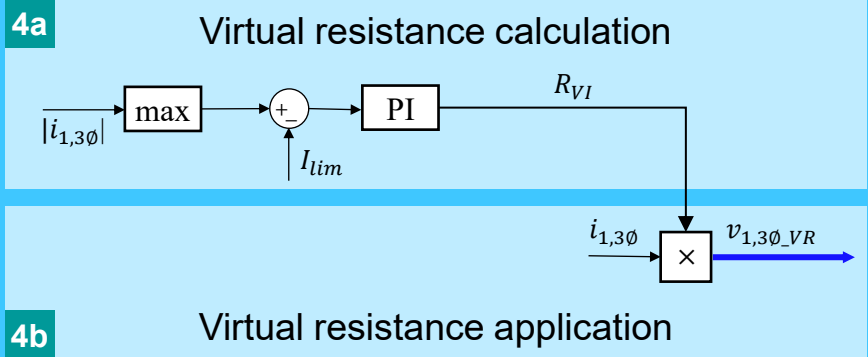
V_{1, I_1} : positive sequence voltage/current, V_{2, I_2} negative sequence voltage/current

GFM: Grid-forming; PI: Proportional Integral; FRT: Fault-Ride Through

Fault-Ride Through 4 reduces fault currents in direct voltage GFM controllers using a single loop virtual resistor

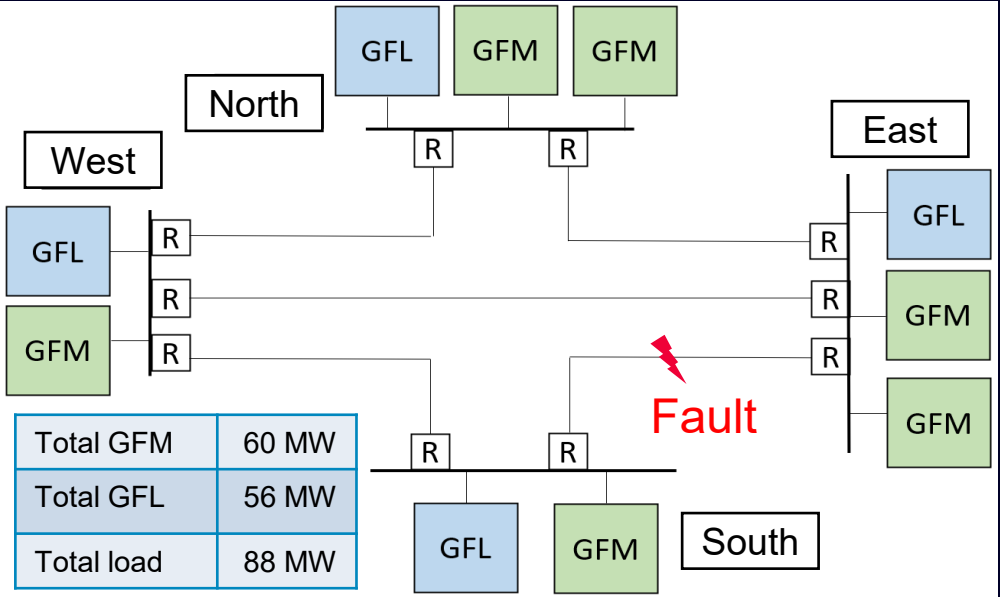
4 Single Loop Virtual Resistor (FRT 4)

- 4a Calculate virtual resistance
- 4b Calculate voltage offset due to virtual resistance
- 4c Apply voltage at PWM stage



V_1, I_1 : positive sequence voltage/current, V_2, I_2 negative sequence voltage/current; GFM: Grid-forming; FRT: Fault-Ride Through; PWM: Pulse-Width Modulation

We are evaluating 4 different FRT and 4 protection relay functions in a PSCAD model with 60 different faults & 17 non-fault cases totaling 1,232 simulations

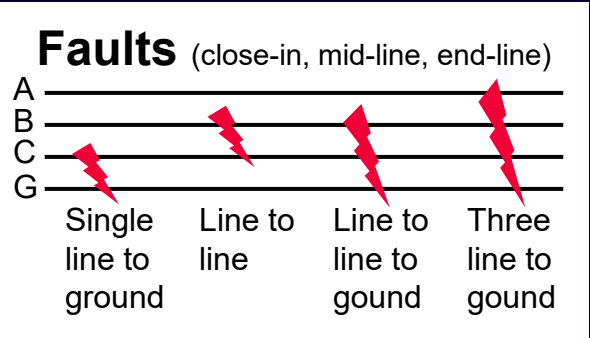


Fault-Ride Through

Grid-forming using cascaded PI control

Grid-forming using direct voltage control

	Current limit	Virtual impedance
FRT1	+	-
FRT2	-	+
FRT3	+	+
FRT4	-	+



Protection

PF1 (overcurrent)
PF2 (distance)
PF3 (POTT)
PF4 (differential)

	FRT1	FRT2	FRT3	FRT4
PF1 (overcurrent)	●	●	●	●
PF2 (distance)	●	●	●	●
PF3 (POTT)	●	●	●	●
PF4 (differential)	●	●	●	●

Exemplary A-G Midline Fault simulation on South-West Line shows successful fault clearance

Relay at bus 1, monitoring line 1-2

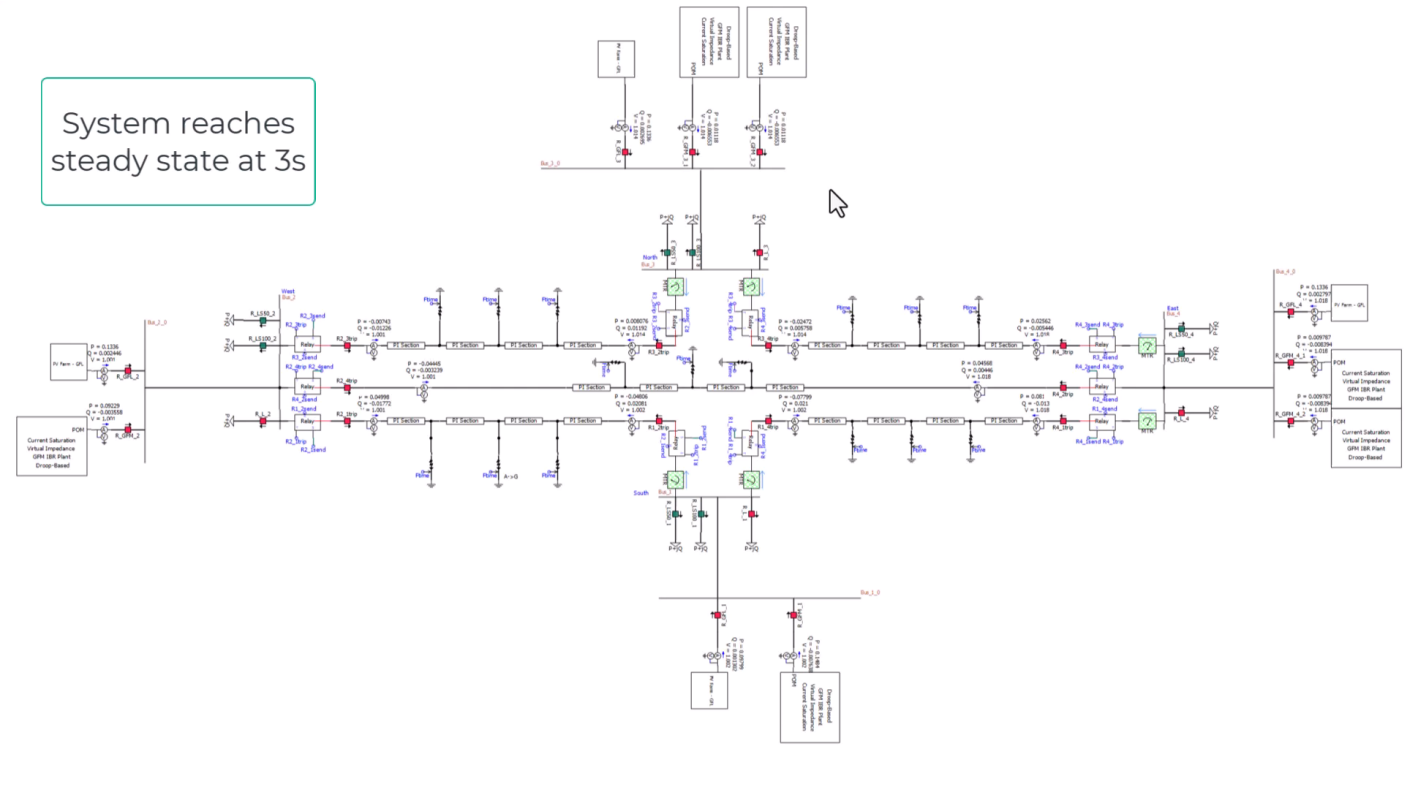
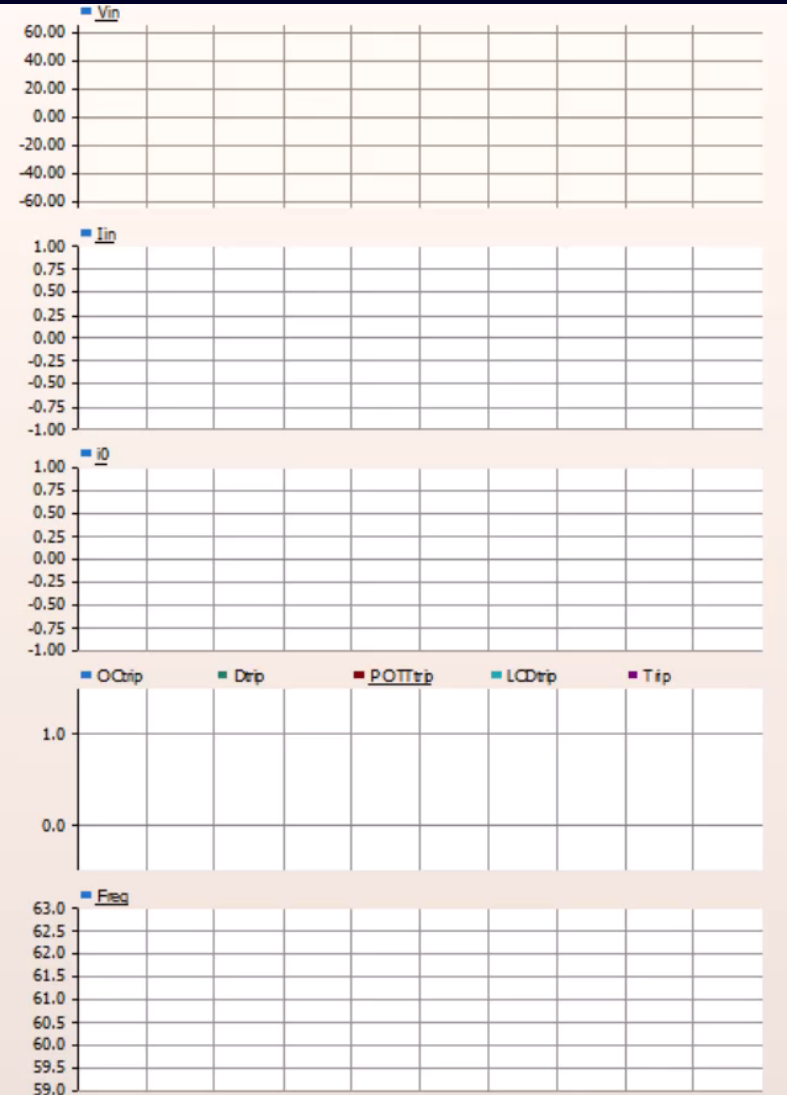
Phase Voltage

Phase Current

Zero Sequence Current

Trip per Relay Mode

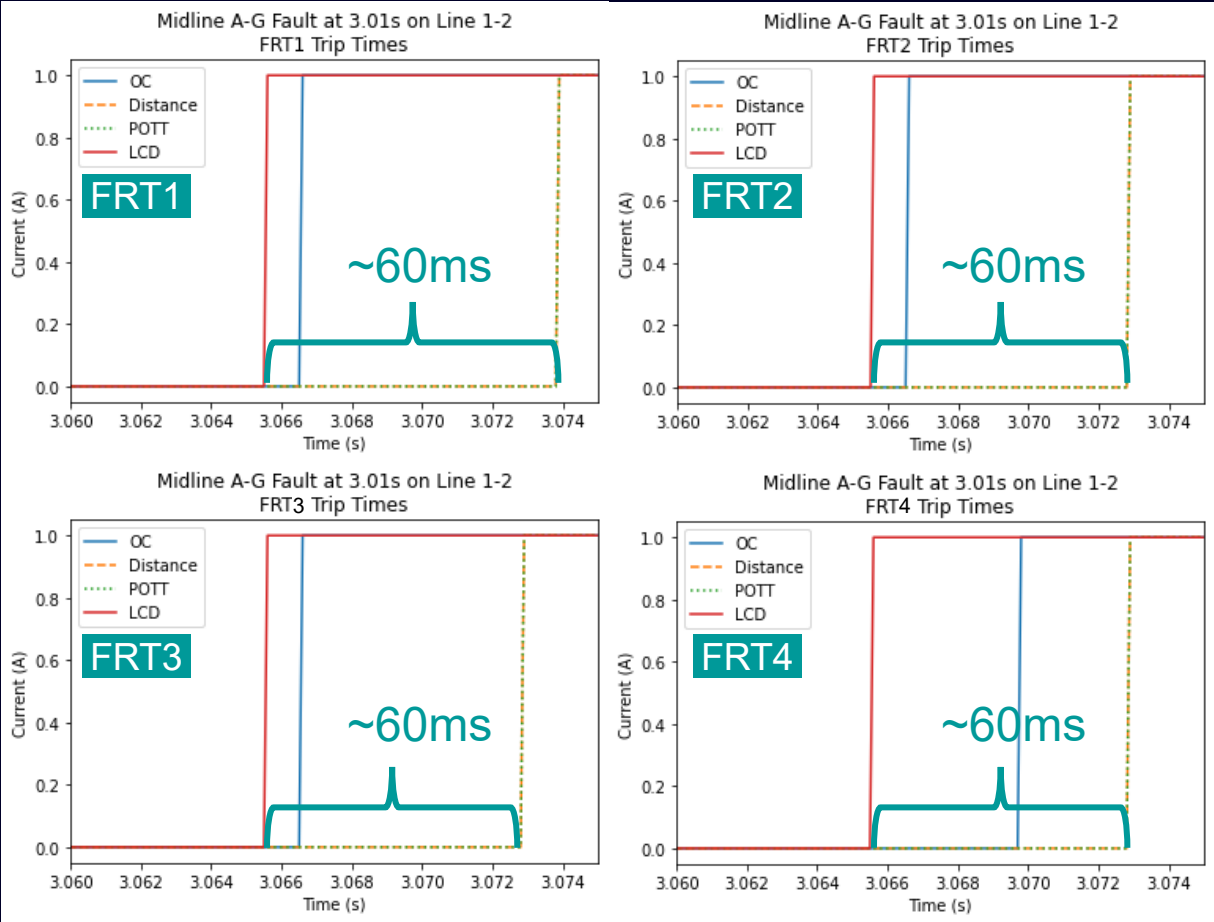
Frequency



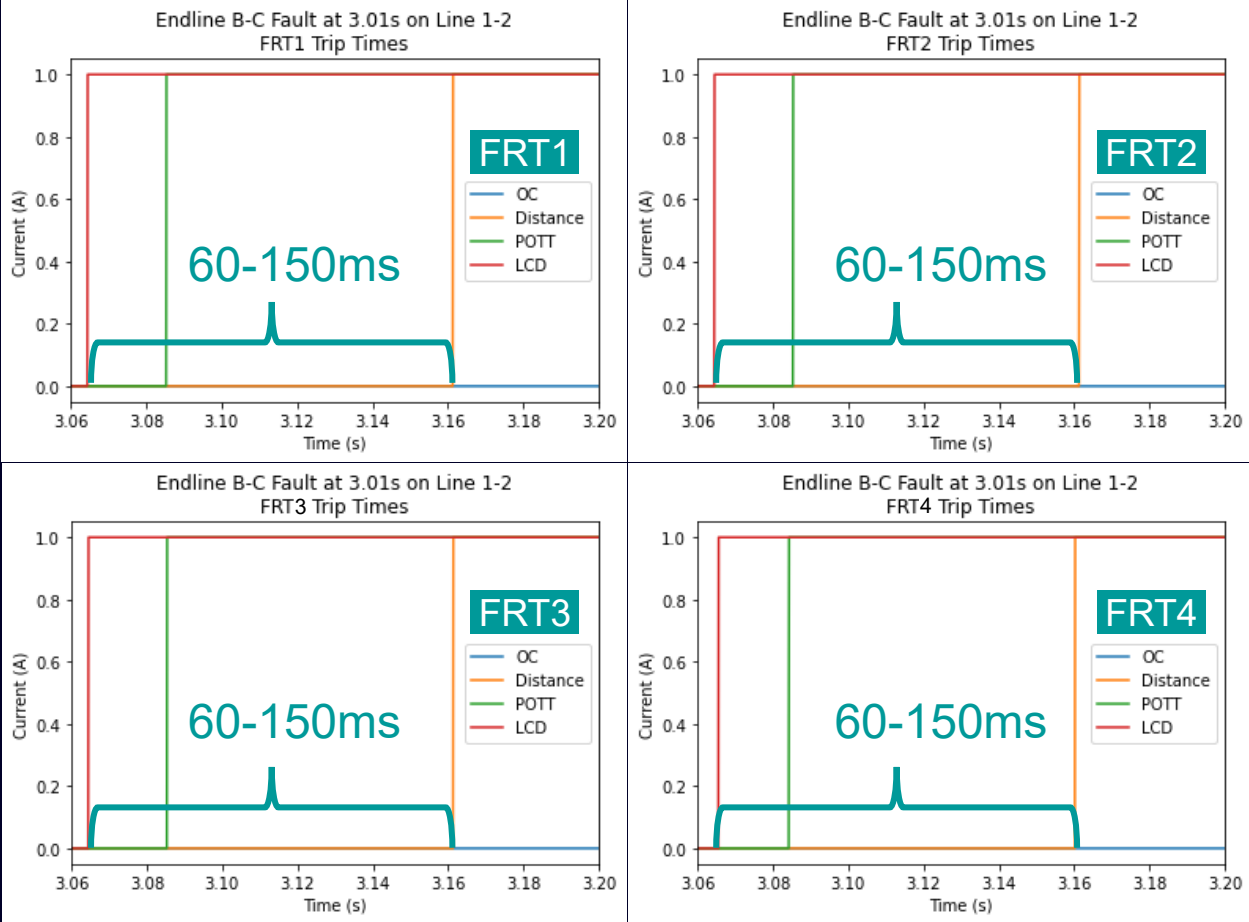
Zoom waveforms around fault

Observation: Fault clearing times of different protection relay functions are homogeneous for midline faults (left) and heterogenous for endline faults (right) irrespective of FRTs

Relay 1-2 trip signals for A-to-G **midline fault** at 3.01s



Relay 1-2 trip signals for B-C **endline fault** at 3.01s



We have defined KPIs for protection evaluation based on IEEE standards and guidelines from Power System Relaying committees to analyze ~1200 simulations

KPIs		Target value
Dependability		
1	% of Faults cleared	100%
Security		
2	% of Faults with mis-operations (incorrect relay)	20% misops
3	% of Faults with mis-operations (incorrect element)	20% misops
4	% of False trips (non-fault scenarios)	10%
Selectivity		
5	% of Faults cleared by the correct relay ¹	80%
Fast fault clearance		
6	Average Fault Clearing Time	5 cycles (83.3 ms)
7	# of breaker operations after 5 cycles	20%
System stability		
8	Time for voltage/active power recovery after fault is cleared	1s after fault
9	Frequency Range (only for non-fault events)	57.8 - 61.5 Hz
10	ROCOF	less than 5Hz/s

KPI evaluation based on

- 960 fault simulations
- 272 non-fault simulations (load and generator steps)

Metrics	FRT 1 Current Limiter + Distance Protection
Average Fault Clearing Time	92 ms
% of Faults with mis-operations	2%
# of operations after 5 cycles	39

Take away #1: High protection dependability, security, selectivity, and fast fault clearance for all FRTs and protection functions except OC

Dependability + security + selectivity + fast fault clearance

- ++ Line Current Differential (LCD)
- ++ Permissive Over-reaching Transfer Trip (POTT)
- + Distance protection
 - Slow clearing for end-line faults
- Over-current protection

Protection	Fault Ride Through	Average Op. Time (ms)		% Cases Op. > 5 cycles (83ms)	% Cases with Misoperation ¹		% Cases with Correct Relay Clearance	% Faults cleared
OC	FRT1	101		27	Incorrect Relay	12	43	55
					Failed Op	45		
	FRT2	99		30	Incorrect Relay	15	40	55
					Failed Op	45		
	FRT4	102		27	Incorrect Relay	12	43	55
					Failed Op	45		
	FRT3	99		27	Incorrect Relay	12	43	55
					Failed Op	45		
Distance	FRT1	Overall	92	57	Incorrect Relay	0	100	100
		Mid	67		Failed Op	0		
		Close/End	104		Incorrect Zone	10		
	FRT2	Overall	92	60	Incorrect Relay	0	100	100
		Mid	67		Failed Op	0		
		Close/End	104		Incorrect Zone	7		
	FRT4	Overall	89	57	Incorrect Relay	0	100	100
		Mid	67		Failed Op	0		
		Close/End	106		Incorrect Zone	10		
	FRT3	Overall	88	47	Incorrect Relay	0	100	100
		Mid	67		Failed Op	0		
		Close/End	98		Incorrect Zone	7		
POTT	FRT1	70		5	Incorrect Relay	0	100	100
					Failed Op	0		
					Incorrect Zone	5		
	FRT2	69		0	Incorrect Relay	0	100	100
					Failed Op	0		
					Incorrect Zone	0		
	FRT4	68		2	Incorrect Relay	0	100	100
					Failed Op	0		
					Incorrect Zone	2		
	FRT3	69		2	Incorrect Relay	0	100	100
					Failed Op	0		
					Incorrect Zone	2		
LCD	FRT1	54		0	Incorrect Relay	0	100	100
					Failed Op	0		
	FRT2	54		0	Incorrect Relay	0	100	100
					Failed Op	0		
	FRT4	55		0	Incorrect Relay	0	100	100
					Failed Op	0		
	FRT3	54		0	Incorrect Relay	0	100	100
					Failed Op	0		

OC: Over-Current; POTT: Permissive Over-Reaching Transfer Trip; LCD: Line Current Differential

Take away #2: Post-clearance system stability and system stability in non-fault cases is achieved for all FRTs and protection functions except OC

Post-fault clearance metrics show good response for Distance, POTT, and LCD

Protection	Fault Ride Through	% Cases where Voltage does not Recover within 5% of pre-fault	Avg. Voltage Recovery Time (ms)	% Cases where Active Power does not recover within 5% of pre-fault	Avg. Power Recovery Time
OC	FRT1	37	216	33	179
	FRT2	37	151	42	172
	FRT4	43	172	42	232
	FRT3	32	219	35	200
Distance	FRT1	0	238	0	119
	FRT2	0	196	0	141
	FRT4	17	348	0	150
	FRT3	3	234	3	142
POTT	FRT1	0	192	0	110
	FRT2	0	162	0	129
	FRT4	5	294	2	139
	FRT3	3	202	3	135
LCD	FRT1	0	169	0	103
	FRT2	0	144	0	115
	FRT4	3	247	0	119
	FRT3	0	186	0	123

Non-fault analysis shows good dynamic response except for ROCOF violations after very high load/generation steps

Protection	Fault Ride Through	% Cases with Misop	% Cases with Nadir Violations	Nadir Avg. (Hz)	% Cases with ROCOF Violations	Max ROCOF Avg. (Hz/s)	% Cases with Max Freq. Violations	Max Freq Avg (Hz)
OC	FRT1	0	6	59.44	29	7.09	6	60.06
	FRT2	0	6	58.09	29	21.08	6	60.06
	FRT4	0	6	59.12	47	8.57	6	60.06
	FRT3	0	6	59.47	29	6.16	0	60.06
Distance	FRT1	6	6	59.39	29	8.60	6	60.06
	FRT2	0	6	58.09	29	21.08	6	60.06
	FRT4	6	6	59.05	47	14.44	12	60.06
	FRT3	0	6	59.47	29	6.16	0	60.06
POTT	FRT1	6	6	59.39	29	8.60	6	60.06
	FRT2	0	6	58.09	29	21.08	6	60.06
	FRT4	6	6	59.05	47	14.44	12	60.06
	FRT3	0	6	59.47	29	6.16	0	60.06
LCD	FRT1	0	6	59.44	29	7.09	6	60.06
	FRT2	0	6	58.09	29	21.08	6	60.06
	FRT4	0	6	59.12	47	8.57	6	60.06
	FRT3	0	6	59.47	29	6.16	0	60.06

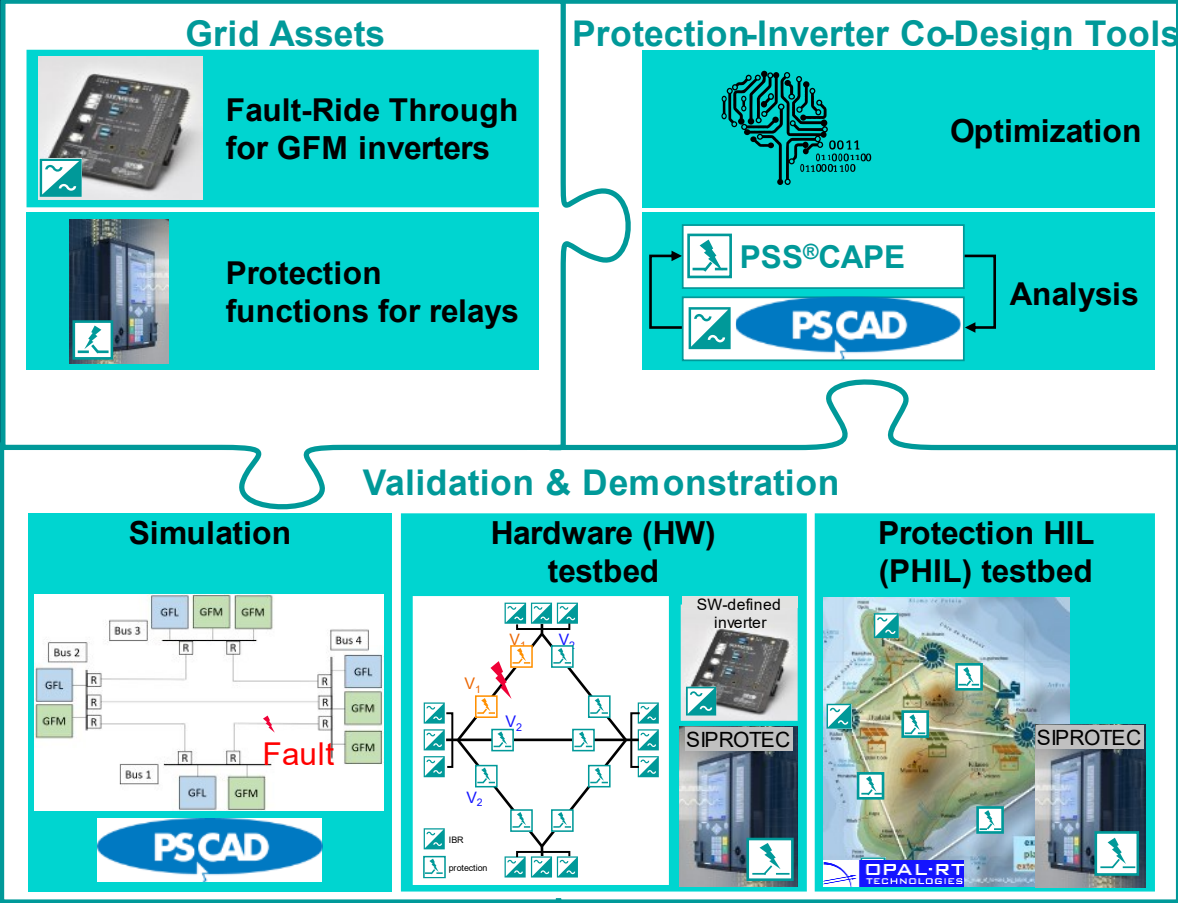
PI-Co Design: Protection-Inverter Co-Design for power system with 100% IBR

Take home messages

- Protection of IBR-dominated transmission systems is a **white spot in the R&D landscape**
- 1,200+ Simulation results indicated that Distance, POTT, and LCD show **high protection dependability & security** in IBR-dominated systems and **good system stability** after fault clearance and during non-fault events with appropriate FRT functions

Outlook

- Validation in HW and PHIL testbeds to harden our simulation results



IBR: Inverter-based Resource; FRT: Fault-Ride Through; Distance Protection; LCD: Line Current Differential
POTT: Permissive Over-reaching Transfer Trip; PHIL: Protection Hardware in the Loop;

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