

Technical Area I: Chips: Materials, Devices and Circuits

Moderator:

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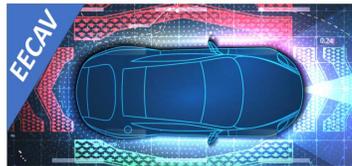
(HPE, now Forschungszentrum Jülich/RWTH Aachen)

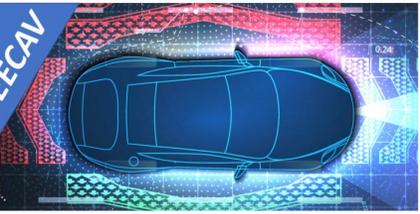
Team Members for TA 1

Wei Lu (Univ of Michigan), Matt Marinella (Sandia), Alec Talin (Sandia), Ian Young (Intel)

Workshop on Energy Efficient Computing for Automated Vehicles (EECAV)

May 11 - 12, 2021



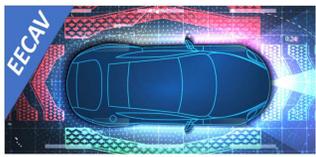


Technical Area I: Chips: Materials, Devices and Circuits

Why This Area?:

- The “supply” of compute capability at high energy efficiency starts with the Chip
 - Materials/Devices/Circuits offer the core building blocks for an energy-efficient chip architecture
- The “demand” in computation is captured in other Technical Areas
 - Includes Algorithms, Data, and Sensor processing

Technical Area I focusses on lower level aspects of chips, taking into account operation in the demanding automotive environment, the computational demands of the larger system, and the need for a path to volume manufacturing



EECAV R&D Problems Identified for Technical Area I

Highest Priority Characteristics of Interest:

1) Reliability

- Temperature robustness (transient and hard faults)
- Mechanical, radiation robustness
- Failure tolerance

2) Performance (latency and energy efficiency)

3) Compatibility & Manufacturability

4) Supply chain vulnerability

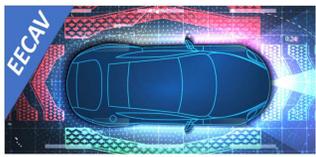
5) Security

Other Characteristics We Considered:

Reconfigurability, Functionality

Facilitate Algorithm-System-Device co-design (e.g., providing compact models)

Ability to rapidly construct platforms (system testbeds)



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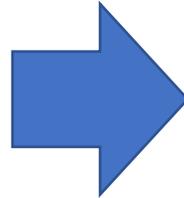
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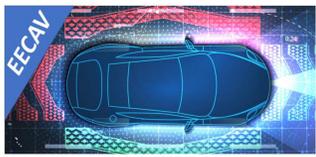
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Ability to rapidly construct platforms (system testbeds)



Associated R&D Problems:

- New, or augmented, **materials and processing for increased thermal/mechanical/radiation robustness** for automotive environments and long life-span
- **Low-latency and low-power devices and circuits**
- **New computing circuits and devices simultaneously optimized for reconfigurability and high performance**



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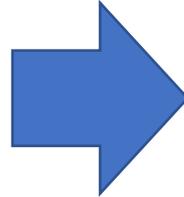
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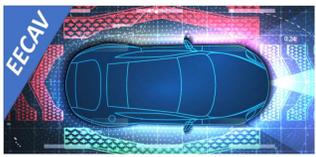
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Are there high priority areas that we missed?



Tech Area I: Detailed Feedback on Specific R&D Problems

R&D Problem 1:

“New, or augmented, materials and processing for increased thermal/mechanical/radiation robustness for automotive environments and long life-span”

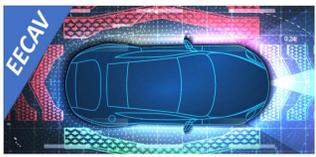
Note: needs to be semiconductor manufacturing compatible.

Potential Research Areas:

- Failure points are typically at interfaces – improve robustness to thermal/mechanical/radiation stress through new treatments and materials, particularly compatible with existing processes
- Interconnects – new and/or augmented interconnects for automotive environment
 - IC wiring, packaging interposers, heterogeneous integration technologies

Questions:

- How high a priority are such materials and processing improvements for R&D funding?
- What environmental threats do you see from the automotive environment?
- Are there associated “measurement science” problems to overcome in making automotive grade chips?
- Do existing (funded) efforts already cover this sufficiently?
- What are we missing?



Tech Area I: Detailed Feedback on Specific R&D Problems

R&D Problem 2:

“Low latency and low power devices and circuits for AV computing needs”

Potential research areas:

- Enable non-von Neumann architectures to reduce energy and latency
 - In-memory devices and circuits: memory and logic/compute are integrated
- Automotive-compatible beyond-CMOS logic devices – e.g., Tunnel-FET, Negative Capacitance FET, Spintronics, graphene, etc
- Automotive-compatible, improved memory technologies (Flash, Ferroelectric, ReRAM, etc)
- Computing with lower-power analog circuits
 - Auto-environment especially challenges temp drift/stability, variability, precision, A-D conversion, etc
- Asynchronous and event-driven circuits

Questions:

- How high a relative priority should we assign to materials/circuit R&D to enable low-latency/low-power systems?
- What other areas of chip operation can be improved to minimize latency and required energy?
- What are we missing?



Tech Area I: Detailed Feedback on Specific R&D Problems

R&D Problem 3:

“New computing circuits and devices simultaneously optimized for reconfigurability and high performance”

Potential research areas:

- Devices, materials and circuits that can improve the speed and reduce the cost of Field Programmable Gate Arrays (FPGA)
- Devices and circuits for Coarse-Grained Reconfigurable Architectures (CGRA)
- Given the target workloads/algorithms (e.g., computer vision), find efficient computing models (e.g., cellular networks) that offer ease of reconfigurability and high performance
- Brain-inspired approaches merging the energy efficiency of biological brains, and with learning/reconfiguration on much slower time-scales

Questions:

- How high a priority is this R&D area for funding?
- Do existing (funded) efforts already cover this sufficiently?
- What are we missing?

Thank You for Your Feedback
on Tech Area I!

