Classifying the Potential Functional Behaviors of Superconducting Circuit Elements in the Ballistic Asynchronous Reversible Computing (BARC) Paradigm

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Abstract. In recent years we have been exploring a novel *asynchronous, ballistic* physical model of reversible computing, variously termed ABRC (Asynchronous Ballistic Reversible Computing) or BARC (Ballistic Asynchronous Reversible Computing). In this model, localized information-bearing pulses propagate bidirectionally along nonbranching interconnects between I/O ports of stateful circuit elements, which carry out reversible transformations of the local digital state. The model appears suitable for implementation in superconducting circuits, using the naturally quantized configuration of magnetic flux in the circuit to encode digital information. One of the early research thrusts in this effort involves the enumeration and classification, at an abstract theoretical level, of the distinct possible reversible digital functional behaviors that primitive BARC circuit elements may exhibit, given the applicable conservation and symmetry constraints in superconducting implementations. In this paper, we describe the motivations for this work, outline our research methodology, and summarize some of the noteworthy preliminary results to date from our theoretical study of BARC elements for bipolarized pulses, and having up to three I/O ports and two internal digital states.

Keywords: theoretical models of reversible computation, asynchronous ballistic reversible computing, reversible superconducting circuits.

1 Extended Abstract

One longstanding motivation for the exploration of reversible computation in a classical computing context has been the desire to improve the energy efficiency of general digital computing hardware, with the goal of eventually circumventing the Landauer limit and approaching true physical (*i.e.*, thermodynamic) reversibility [1]. Most design schemes for implementing classical reversible computation in hardware in a manner that could potentially approach physical reversibility rely on the concept of carrying out synchronous, adiabatic transformations of the machine's digital state under control of externally applied power-clock waveforms (*e.g.*, see [2,3]). To approach physical reversibility requires these waveforms to be provided using high-quality resonant circuit elements to recover and reuse the signal energy. But the design of extremely high-quality resonant circuits presents significant engineering challenges [4].

One potential alternative to the adiabatic approach to reversible computing is represented by *ballistic* schemes for reversible computing, the archetypal example of which is Fredkin's billiard ball model [5]. In ballistic approaches, the energy required to carry out logical state transitions is carried along with the digital information in a compact, ballistically-propagating entity (such as an idealized billiard ball), and interactions (such as elastic collisions) between these entities carry out reversible logical operations, while locally conserving the signal energy. However, classic concepts for ballistic reversible computing required precise synchronization between independent ballistic signals, which is not physically realistic; real-world implementations would typically suffer from chaotic instabilities that degrade the signal trajectories, requiring dissipative processes to restore the degraded signal.

These well-known difficulties with synchronous ballistic reversible computing motivated the development of the novel reversible computing paradigm known as *asynchronous* ballistic reversible computing (abbreviated ABRC, or henceforth BARC). In BARC, the ballistically-propagating energy- and information-bearing entities (which we typically call "pulses") are guided along one-dimensional, non-branching interconnects, and interact *one at a time* with stationary circuit elements or "devices" bearing an internal digital state. Due to the temporal separation of pulse arrivals, the physical dynamics of this class of systems is expected to be much less prone to dynamical instability, requiring only relatively occasional signal restoration to ensure that the pulses' kinetic energies and arrival times remain within broad tolerances.

The BARC model was first introduced in 2017 [6], along with a proof of its computation universality, and in 2018 [7] and 2019 [8] we described some preliminary results from a present effort at Sandia to develop a physical implementation of this new scheme in superconducting circuits. In the current effort (called "BARCS", for BARC in Superconductors), the pulses are physically embodied by quantized solitons of magnetic flux or *fluxons* propagating along long Josephson junction transmission lines, and the devices are also implemented as Josephson junction circuits. In these types of circuits, there is a natural digital representation of information in terms of the polarization and location of the magnetic flux quanta present in the circuit; the physics of superconductors results in a natural stability of digital information encoded in this way.

A major goal of the BARCS effort is to demonstrate a computation-universal subset of the possible asynchronous reversible devices. The engineering side of this work is ongoing, but one of the important theoretical steps on the way to this goal is to thoroughly characterize the possible digital functional behaviors of such devices. We wish to thoroughly understand the full space of design possibilities, to facilitate our efforts as we search both for workable physical implementations of useful devices, and also for simplified schemes for constructing computational circuits of arbitrary complexity out of potentially implementable primitive circuit elements.

In this paper, we will summarize the major results to date that have emerged from the theory side of this effort, which include the classification of the possible asynchronous reversible behaviors for devices having up to three bidirectional I/O ports and two internal states, in the context of a variety of applicable conservation and symmetry constraints.

A simple Python program was developed to assist us in classifying the most complex category of devices studied in this effort so far, consisting of all the three-port flux-conserving elements that support two flux-neutral internal states and respect a basic flux-negation symmetry constraint. This program generated an enumeration of 600 nontrivial function descriptions at a representational level, and grouped them into 45 distinct equivalence classes, such that the members of each class transform to each other via some subset of several other natural mutually commuting symmetry transformations that function descriptions in this family may support, such as symmetry under simple reorderings of the I/O ports and internal states. The 11 largest equivalence classes correspond to the most "irregular" possible reversible device behaviors, each of which exhibits only a minimal set of self-symmetries that are already known to be required. Each such behavior has 24 essentially equivalent representations, which are arrayed across the entire composite symmetry group consisting of all 24 possible combinations of the various optional symmetry transformations.

In the full paper, in addition to describing this classification program and summarizing the results obtained to date, we will also elaborate further on our motivation and methods. We will conclude by summarizing the status of our hardware implementation efforts to date and discussing useful next steps for this line of work.

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