Sandia National Laboratories

Modeling Asynchronous Ballistic Reversible Computing (ABRC) Primitive Elements Using Superconducting Circuits

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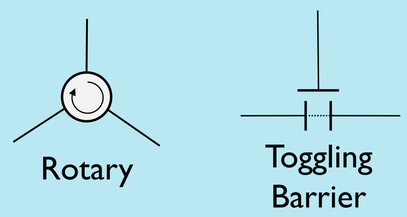
I. Motivation

- Improve superconducting logic & memory styles
  - In terms of energy, area, delay related efficiency
- Extreme energy efficiency requires *reversible computing*, but typical *adiabatic* reversible logic styles require relatively slow speeds and impose an area overhead for clocking.
  - Can do better with a *ballistic* reversible logic family?
- *Synchronous* ballistic reversible logic imposes additional energy costs for synchronization.
  - Can we do *asynchronous* ballistic reversible computing?
- **Problem Statement:** *Investigate whether/how asynchronous ballistic reversible computing (ABRC) can be implemented in SCE using single flux quanta* (SFQ).

II. Abstract Model (2017)

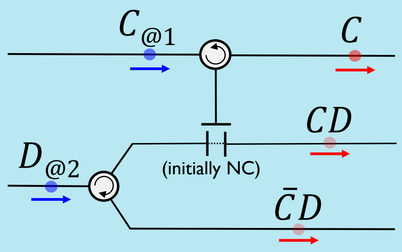
- Frank (ICRC 2017) introduced *Asynchronous Ballistic Reversible Computing* (ABRC), the first *general* theoretical circuit model of asynchronous, universal reversible computation.
  - Data pulses propagate ballistically and asynchronously between devices
  - Local device state updates reversibly on pulse arrival
- **Research Question:** *Can the abstract ABRC model be implemented using ballistically-propagating flux quanta (fluxons) as the signal pulses, and stationary (but mutable) trapped fluxons to register the internal device state?*
  - *While dissipating much less than the fluxon energy per scattering/state-update event?*

Unary ABRC primitives:



(First set of ABRC primitives proved to be computation universal)

Example ABRC logic construction:

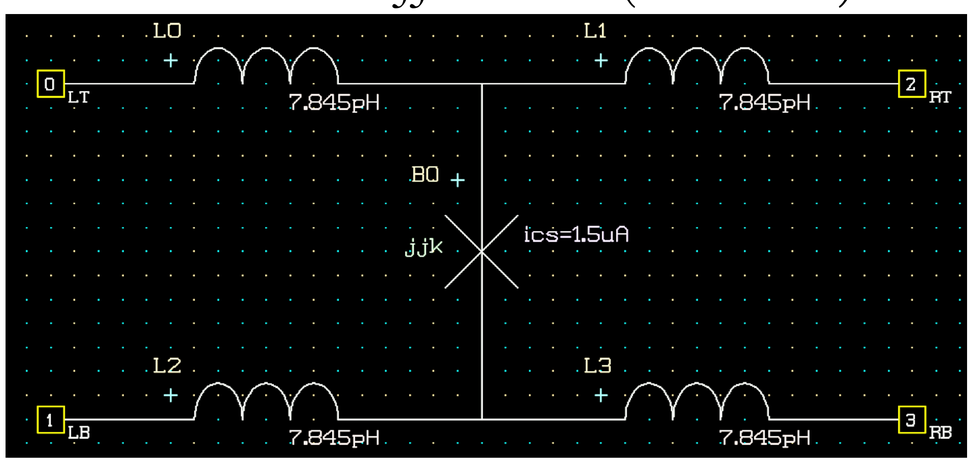


(AND from toggling switch gate)

III. Ballistic Interconnects (2018)

- We are studying **Long Josephson Junction (LJJ)** transmission lines for SFQ transport
  - Support a topological *flux soliton* (***fluxon***) mode which maintains pulse coherence / limits pulse spreading
    - Fluxons can be accelerated via a bias current density
- Our initial investigation is focusing on **discretized LJJ (dLJJ)** structures to facilitate simulations

- XIC schematic for dLJJ unit cell (ASC 2018):



- JJ model in XIC's `model.lib` file:

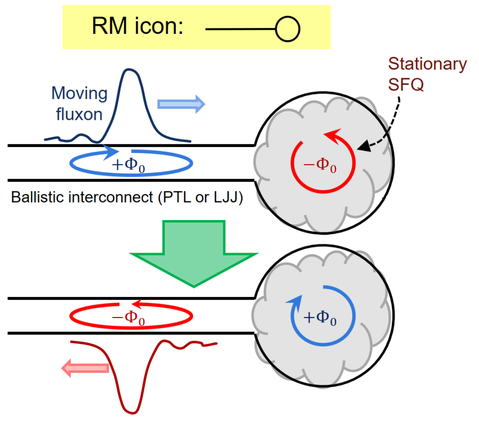
```
.model jjk jj(rtype=0, vg=2.8m,
+              icrit=1.5u, cap=60f)
```

IV. Simple Device Concept (2018)

- We identified the simplest useful, nontrivial ABRC function for binary (polarized) pulses:
  - The one-port, two-state *Reversible Memory* (RM) cell.

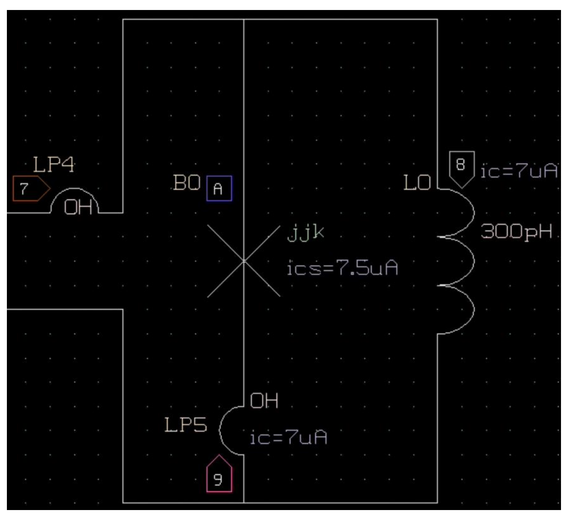
RM Transition Table

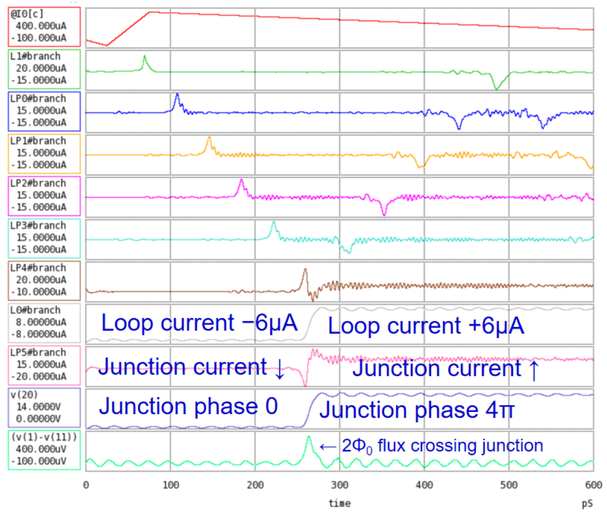
Input Syndrome		Output Syndrome
+1(+1)	→	(+1)+1
+1(−1)	→	(+1)−1
−1(+1)	→	(−1)+1
−1(−1)	→	(−1)−1



V. First Working Implementation (2019)

- It turns out a simple SFQ storage cell does the job!
  - Critical current of JJ ≈ ½ peak current of LJJ fluxon





VI. Conclusion & Future Work

- We now have the first concrete demonstration that the ABRC model makes sense physically.
  - This can be the start of a new variety of digital SCE.
- Some next steps:
  - Refine the present RM circuit to improve elasticity.
  - Lay out, fabricate and empirically test the design.
  - Design a more complete set of ABRC circuit elements.

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