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Semi-Automated Design of Functional Elements for a New Approach to Digital Superconducting Electronics:

Methodology & Preliminary Results

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Outline of talk

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- **Context:** The *Asynchronous Ballistic Reversible Computing* (ABRC) model of physical reversible computation
  - Motivation & Overview
- **Current project** at Sandia to implement ABRC in SCE:
  - **Review** of last year's study of ballistic fluxon propagation in LJJs.
  - **This year's goal:** Implement the *simplest* nontrivial ABRC function.
  - **Preliminary results:** A working implementation! (In simulation)
  - **Looking forwards:** Automate the circuit discovery process.
- **Conclusion**

- ***Collaborators:*** *Rupert **Lewis**, Nancy **Missert**, David **Henry**, Matt **Wolak**, Erik **DeBenedictis** (all at Sandia)*
  - ***Also with:*** *Rudro **Biswas** (Purdue), Karpur **Shukla** (Flame U.)*
    - ***Thanks also to:*** *K. **Osborn**, L. **Yu** (LPS)*

Why do we need a new reversible computation paradigm for SCE?

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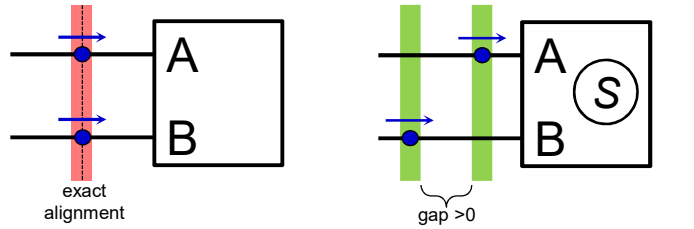
- In general, we'd like improved, more *efficient* SC logic families.
  - Cost-efficient in terms of various cost measures—energy, area, delay…
- Improving *energy* efficiency by extreme amounts absolutely requires the application of *reversible computing* principles…
  - This is guaranteed by fundamental physics (Landauer's Principle).
- However, most existing *adiabatic* schemes for reversible computing require that every digital transition must be driven by a (typically externally-supplied) clock/power signal…
  - Distributing these signals throughout a chip imposes area overheads
  - Also, adiabatic transitions tend to be *slow* (vs. relaxation timescale)
- An alternative vision of *ballistic* reversible computing could potentially be faster and simpler than adiabatic approaches…
  - But traditional models of ballistic computing were *synchronous*—thus, still required pervasive clocks, and/or dissipative synchronization mechanisms!
- **Research challenge:** Develop a new technology for *asynchronous* ballistic reversible computing in superconducting electronics.

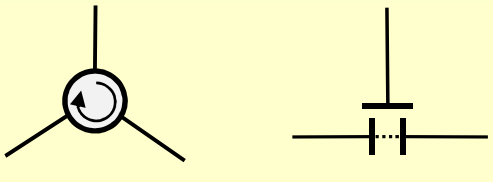
Asynchronous Ballistic Reversible Computing

in Superconducting Electronics (LDRD at Sandia)

- **Problem:** Conservative (dissipationless) dynamical systems generally tend to exhibit chaotic behavior…
  - This results from direct nonlinear *interactions* between multiple continuous dynamical degrees of freedom (DOFs)
    - *E.g.*, positions/velocities of ballistically-propagating pulses
- **Core insight:** In principle, we can greatly reduce or eliminate this tendency towards dynamical chaos…
  - We can do this by *avoiding* any direct interaction between continuous DOFs of different ballistically-propagating signals
- Require localized pulses to arrive *asynchronously*—and furthermore, at clearly distinct, non-overlapping times
  - Device's dynamical trajectory then becomes *independent* of the precise (absolute *and* relative) pulse arrival times
    - As a result, timing uncertainty per logic stage can now accumulate only *linearly*, not exponentially
      - Only occasional re-synchronization will be needed
  - For devices to still be capable of doing logic, they must now maintain an internal discrete (digitally-precise) state variable
- No power-clock signals, unlike in adiabatic designs
  - Devices simply operate whenever data pulses arrive
  - The operation energy is carried by the pulse itself
    - Most of the energy is preserved in outgoing pulses
      - Signal restoration can be carried out incrementally
- **Goal of current project:** Demonstrate ABRC principles in an implementation based on fluxon dynamics in SCE

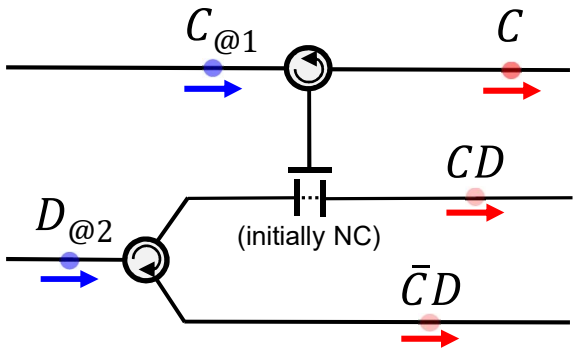


Synchronous Ballistic Asynchronous Ballistic



Rotary (Circulator) Toggled Barrier

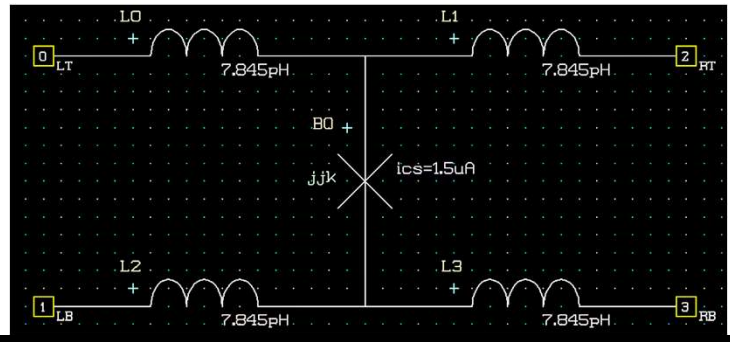
Example ABR device functions

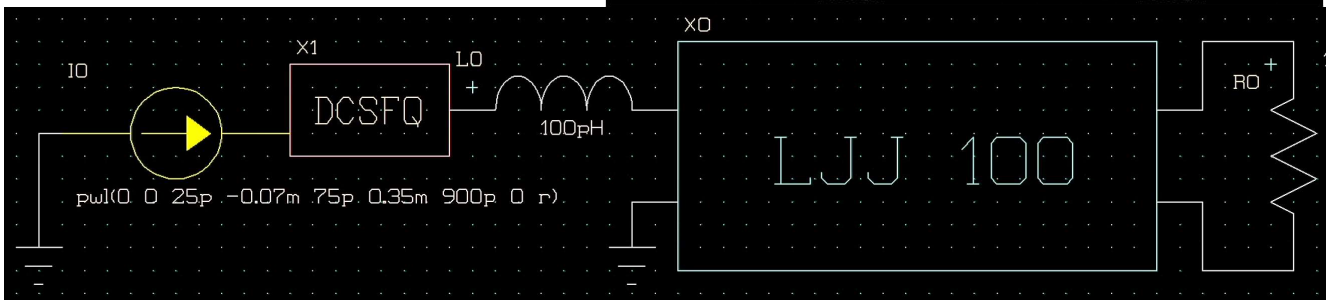


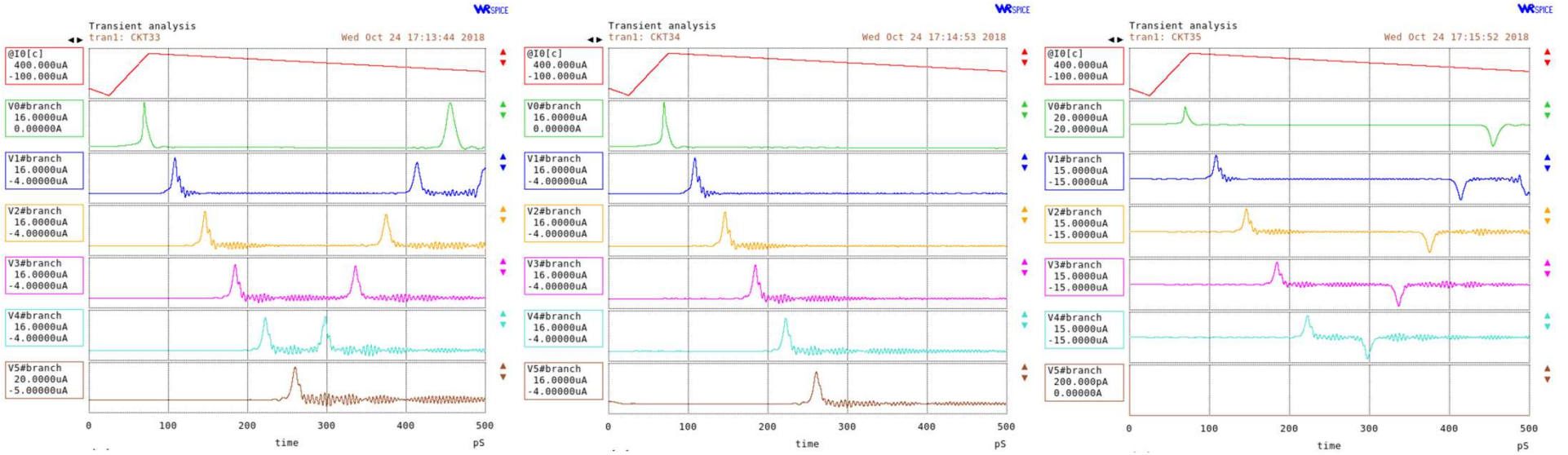
Example logic construction

WRSPICE simulations of discrete LJJ

- Preliminary effort completed in FY18
  - ASC (Sep. '18) 10.1109/TASC.2019.2904962
- Modeled buildable test structures in XIC
- Confirmed ballistic fluxon propagation
  - Verified predicted dLJJ line impedance of 16 Ω

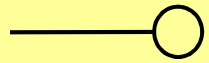


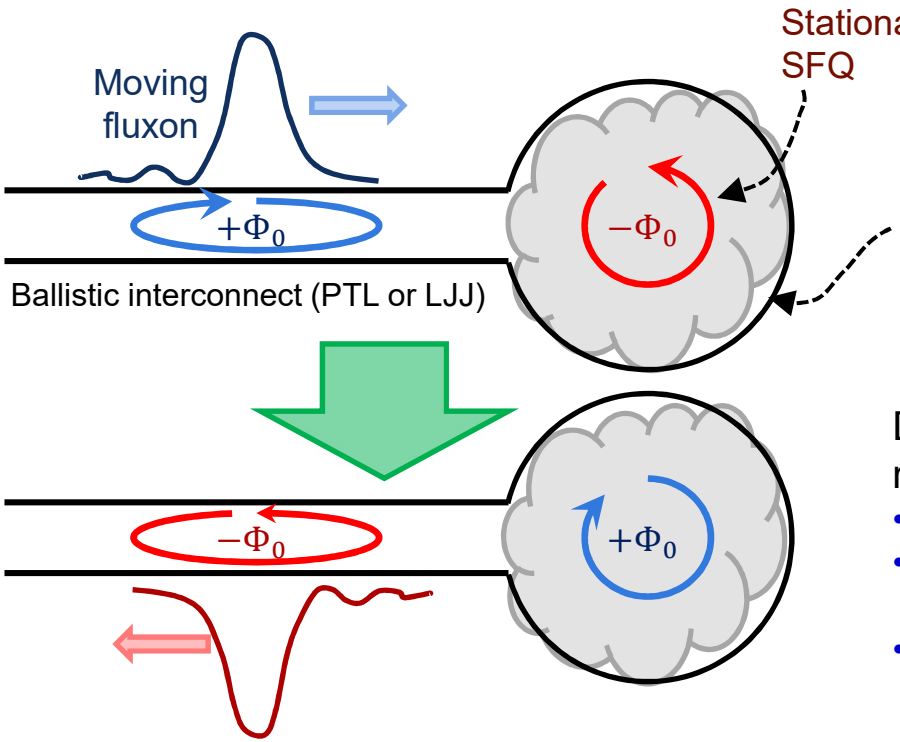




Simplest Fluxon-Based ABRC Function

- **Another FY18 task** was: Characterize the simplest nontrivial ABRC device functionalities, given a few simple design constraints applying to an SCE-based implementation, such as:
  - (1) Bits encoded in fluxon polarity; (2) Bounded planar circuit conserving flux; (3) Physical symmetry.
- Determined through theoretical analysis that the simplest such function is the following ***1-Bit, 1-Port Reversible Memory Cell (RM):***
  - Due to its simplicity, this is the preferred target for our detailed circuit design efforts looking forwards…

RM icon: 



RM Transition Table

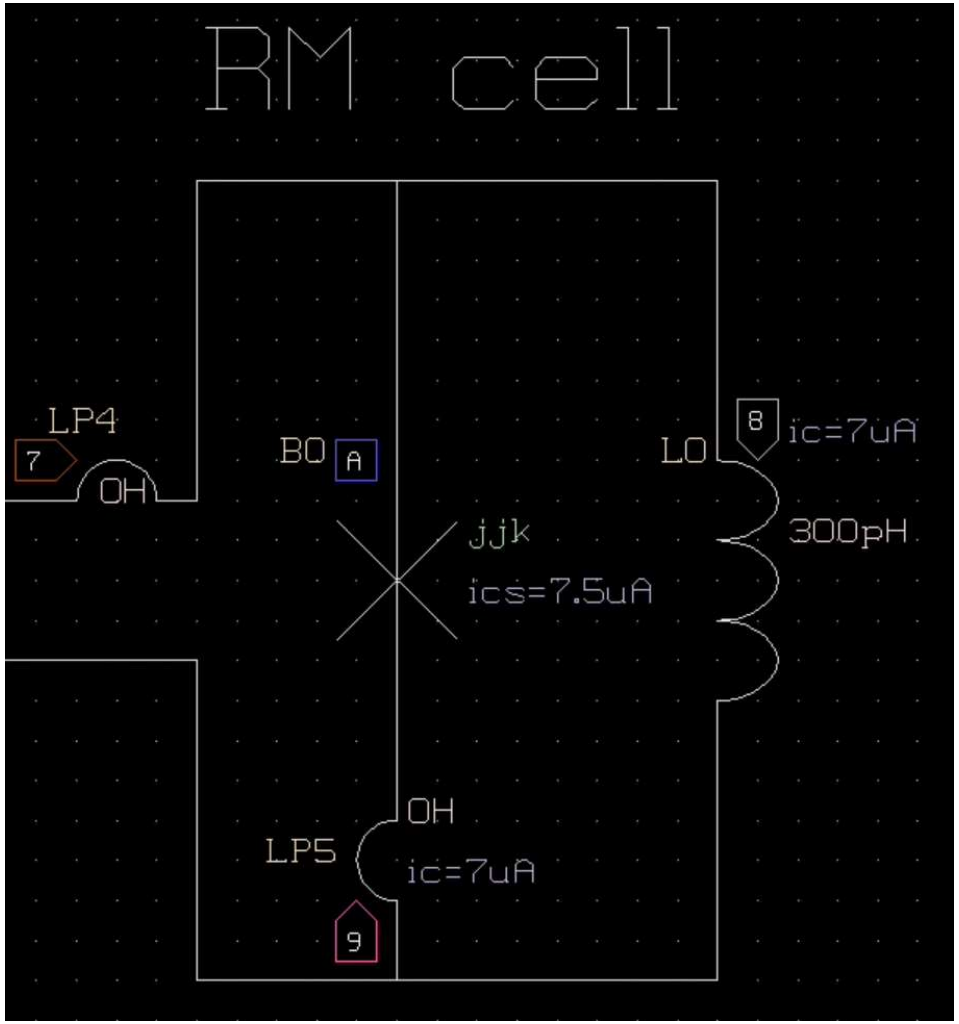
Input Syndrome		Output Syndrome
+1(+1)	→	(+1)+1
+1(−1)	→	(+1)−1
−1(+1)	→	(−1)+1
−1(−1)	→	(−1)−1

Some planar, unbiased, reactive SCE circuit (to be designed) w. a continuous superconducting boundary
- *Only* contains L's, M's, C's, and *unshunted* JJs
- Keep junctions *subcritical* when possible (avoids R_N)
- Conserves total flux, approximately nondissipative

Desired circuit behavior (NOTE: conserves flux, respects T symmetry & logical reversibility):
- If polarities are opposite, they are swapped (shown)
- If polarities are identical, input fluxon reflects back out with no change in polarity (not shown)
- *Elastic scattering* type interaction: Input fluxon kinetic energy is (nearly) preserved in output fluxon

RM—First working implementation!

- DeBenedictis: “Try just putting a JJ across the loop.”
  - This actually works!
- JJ sized to = about 5 LJJ unit cells (~1/2 pulse width)
  - I first tried it twice as large, & fluxons annihilated instead…
    - 🤔 “If a 15uA JJ rotates by 2π, maybe ½ that will rotate by 4π”
- Loop inductor sized so 1 SFQ will fit in the loop (but not 2)
  - JJ a bit below critical with 1
- WRSPICE simulations with +/−1 fluxon initially in the loop
  - Uses `ic` parameter, & `uic` option to `.tran` command
  - Produces initial ringing due to overly-constricted initial flux
    - Can eliminate via small shunt *G*



WRspice simulation results

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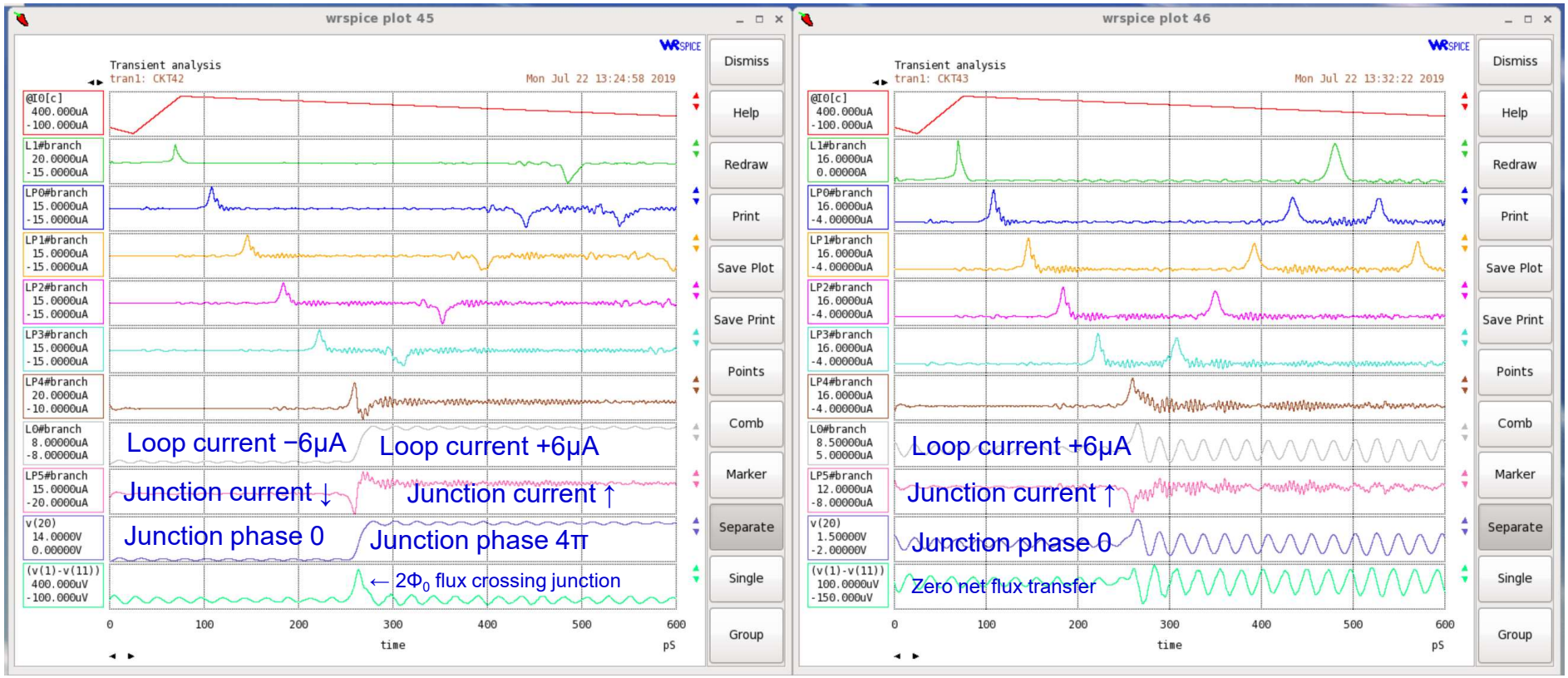
Polarity mismatch → Exchange

Polarity match → Reflect (=Exchange)



Next Steps re: RM Design

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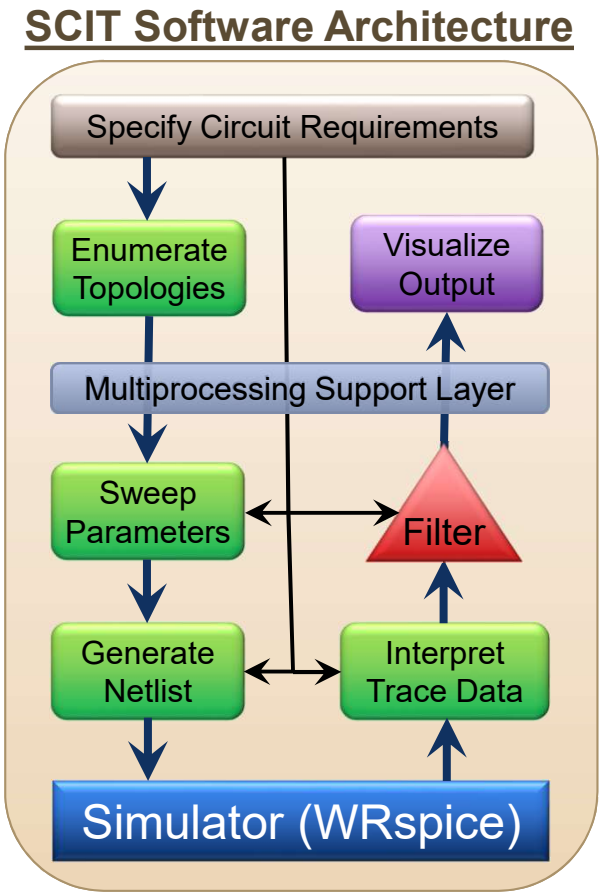
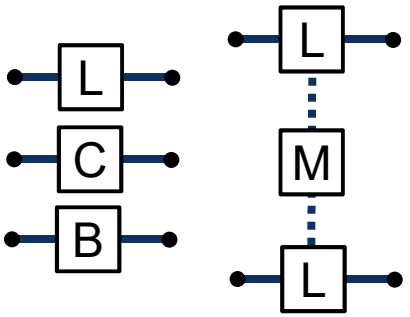
- Understand better, at a theoretical level, the engineering requirements for this circuit to work properly.
  - And, can we generalize this understanding to more complex cases?
    - Goal: Design circuits for a wide variety of other ABRC functions.
- Detailed design & empirical testing of a physical prototype.
  - Lay out artwork, extract parasitics, fabricate a test chip, and experimentally test the circuit behavior in the lab.
- Carry out further elaborations of design to fine-tune dynamic response for high-fidelity preservation of pulse shape.
  - Should be able to use 3D physics modeling, solve inverse problem to craft a very high-quality custom layout (similar to metamaterials).
- Investigate applications, *e.g.*:
  - Can this device be extended to become the basis for a relatively dense SFQ memory fabric (compared to *e.g.* arrays of NDRO cells)?
    - Develop suitable row/column interface logic
    - Optimize the cell design for more compact area

Automation of Circuit Discovery

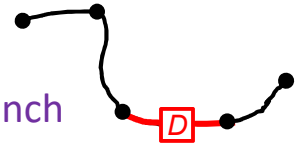
- Due to the novelty of our new logic style, the principles to design much improved/more complex ABRC circuits aren't obvious…
  - **Solution:** Automate our circuit-discovery methodology!
- Started developing a new tool, named **SCIT**
  - ***Superconducting Circuit Innovation Tool***
- Outline of the SCIT processing flow:
  1. Define circuit design requirements
  2. Enumerate possible circuit topologies
     - In order of increasing complexity
  3. Delegate topologies to MPC nodes
  4. Sweep over device parameter space
  5. Generate a netlist for each test design
  6. Simulate netlist locally (in e.g. WRspice)
  7. Interpret & summarize resulting traces
  8. Filter for results with desired properties
  9. Facilitate visualization of candidate designs
- Challenges to be solved include:
  - Identifying state changes in arbitrary circuits



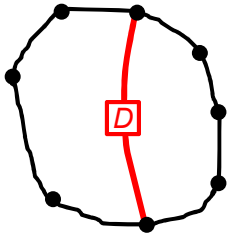
Topology Enumeration Algorithm



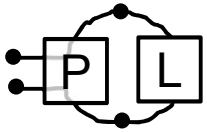
- Two-terminal circuit primitives:
  - L – Wire segment with inductance.
  - C – Capacitive coupling between nodes.
  - B – Josephson junction.
  - M – Mutual inductive coupling between wire segments.
- An algorithm to enumerate all N-primitive planar circuits:
  - Recursively, enumerate all $(N-1)$-primitive circuits; for each:
    - For each primitive branch in the circuit,
      - For each device type L,C,B:
        - » Generate each possible in-line device insertion on that branch



    - For each primitive loop in the circuit,
      - For each device type L,C,M,B:
        - » Generate each possible device placement across that loop
        - » Special case for M: Couple two wire segments.



  - Base case for recursion:
    - One loop with two primitives, I/O port (P) and wire (L).



Conclusion

- **Key result:** We have simulated the first concrete working example of an SCE circuit implementing one of the reversible functions in the new ABRC model.
  - Provides a **reversible memory cell** functionality using just 1 JJ.
- **Next steps** include:
  - **Prototype & test** this circuit in a suitable process.
  - **Identify additional functions** in the ABRC model that may be amenable to similarly straightforward implementations.
  - **Implement circuit search tool** (SCIT) for more rapid discovery of circuits for more complex ABRC functionalities.
- **Impact:** ABRC could become the foundation for an important new class of low-energy SCE logic families.
  - Our present project is starting to lay the groundwork.