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Asynchronous Ballistic Reversible Computing using Superconducting Elements (Project #41)

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ACS BAA Portfolio Review
WebEx
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Contributors to the larger effort:

- Full group at Sandia:
  - Michael Frank (Nonconventional Computing)
  - Rupert Lewis (Quantum Phenomena)
  - Nancy Missert (Nanoscale Sciences)
    - Matt Wolak
  - David Henry (MESA Hetero-Integration)

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- Thanks are also due to the following colleagues & external collaborators:
  - Erik DeBenedictis
  - Kevin Osborn (LPS/JQI)
    - Liuqi Yu
  - Steve Kaplan
  - Rudro Biswas (Purdue)
    - Dewan Woods
  - Karpur Shukla (CMU/Brown U.)
    - w. Prof. Jingming "Jimmy" Xu
  - David Guéry-Odelin (Toulouse U.)
  - FAMU-FSU College of Engineering:
    - Sastry Pamidi (ECE Chair)
    - Jerris Hooker (Instructor)
    - Fadi Matloob
    - Frank Allen
    - Oscar L. Corces
    - James Hardy
  - *Others may be forthcoming…*

Outline of talk

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- **Motivation:** Improving *dissipation-delay efficiency* in SCE
  - Appears limited in existing SCE logic families (as well as in CMOS)
  - Can we find a new SCE logic style that may give a path forward?
- **Approach:** Reversible computing without clocking overhead?
  - Adiabatic SCE logic families have dissipation/op $\propto$ 1/(transition time)
    - Typical in *classical* adiabatic processes: *e.g.* resistance, friction, viscosity
  - However, *quantum* adiabatic processes can do better than this!
    - Exponential adiabaticity of Landau-Zener transitions in scattering procs.
  - Can elastic scattering of fluxons do *ballistic* reversible computing?
    - Use *Asynchronous Ballistic Reversible Computing* model of computation
- **ACI/ACS-funded project at Sandia:**
  - Review of progress to date: LJJ interconnects, RM cell, test chip
  - Project plan looking forwards:
    - Continued technology development (more circuits / experimental tests)
      - Also investigating whether theoretical methods of *superadiabaticity / shortcuts to adiabaticity* (STA) might be applied in fluxon-based systems

Project Plan Outline (from Proposal)

- Three main technical thrusts:
  - Theory, Modeling, Applications
    - PI – M. Frank
  - Devices, Circuits & Simulation
    - Co-PI – R. Lewis
  - Fabrication, Measurement
    - Key Personnel: N. Missert
- University subawards:
  - Design Tools (FAMU/FSU)
    - Matloob, Allen, Corces, Hardy
  - Fundamental Physics (Brown)
    - K. Shukla w. J. Xu
  - Circuit Analysis (Purdue)
    - R. Biswas & D. Woods
- One year base period and two one-year option periods

Project Year	Thrust 1: Theory, Modeling, Applications & Design Automation (PI — M. Frank)	Thrust 2: Device Physics, Circuit Layout, Simulation, & Electrical Testing (Co-PI — R. Lewis)	Thrust 3: Device Structures, Fabrication Process, & Metrology (N. Missert)
BASE PERIOD **Year 1:** Initial discovery / exploration Budget request: $350K	- Categorize 3-port polarized ABRC functional elements. - Finish developing SCIT (Superconducting Circuit Innovation Tool). - Work w. collaborators on circuit modeling & reversible physics.	- Develop capability to design, simulate and test SFQ-based circuits containing multiple elements. - Work w. remote collabs. on device & circuit models	- Develop adaptations to Sandia's in-house fabrication process to minimize dissipation in JJs with Ta-N and AlN barriers for initial designs of ABRC circuit elements
OPTION PERIOD 1 **Year 2:** Create novel logic technology. Budget request: $400K	- Utilize SCIT to create optimized circuit designs for selected functional elements. - Create optimized logic architectures based on simplified primitives. - Work w. collaborators to assess capacity for superadiabaticity to occur in SFQ-based ABRC.	- Layout and test optimized functional element designs. - Begin measuring energy efficiency of designs. - Work w. remote collaborators to improve circuit models based on measurement results.	- Incorporate AlN barriers into JJs, SQUIDs, and LJJs. - Supervise fabrication of first ABRC test circuits. - Work with external fabrication lines to obtain circuits incorporating AlOx JJs if needed.
OPTION PERIOD 2 **Year 3:** Create novel digital architectures. Budget request: $400K	- Design and optimize useful functional unit designs using the new logic elements (e.g., 4-bit adder). - Work w. collaborators to identify ways to amplify superadiabatic scaling in more advanced designs.	- Layout and test optimized functional unit designs (e.g., 4-bit adder). - Characterize energy efficiency. - Continue working w. collaborators to further improve circuit models.	- Further improve capacity, reliability of updated in-house fab process. - Supervise fabrication of complete ABRC demonstration chips. - Consider next steps for in-house fab capability.

Dissipation-delay Efficiency (DdE)

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- A key motivating Figure of Merit (FOM) in the present study.
- For a single *primitive* transition of the digital state of a system between two distinct informational states, consider:
  - The *energy dissipation* D incurred by that transition process.
    - Relates to real-world costs associated with supply of energy and cooling.
  - The *delay* d, defined as the time interval from start to end of process.
    - Relates to costs associated with achieving a given level of parallel performance.
- Then define the *dissipation-delay product* $\mathrm{DdP} = D \cdot d$.
  - Note that since D refers specifically to energy *dissipation*, not to energy *invested* in the signal, in reversible processes, it is *not subject to the "quantum speed limit"* (QSL) lower bound of $\sim h$! (*E.g.* Margolus-Levitin)
    - No *fundamental* lower bound to DdP is yet known!
      - In fact, it would be identically zero for any perfectly-known unitary time-evolution.
  - Of even more general interest than DdP per se is dissipation *as a function of* delay, $D(d)$, considered over a range of practical (tolerable) delay values…
    - We'd like to extend the *pareto frontier* of this function within the useful range.
- *Dissipation-delay efficiency* (DdE) of a given computing technology just refers to the reciprocal of DdP, $\eta_{\mathrm{Dd}} = (Dd)^{-1}$.

Existing Dissipation-Delay Relations

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Energy & delay, CMOS FO3 HP

One CMOS logic gate

2017 ("10 nm")

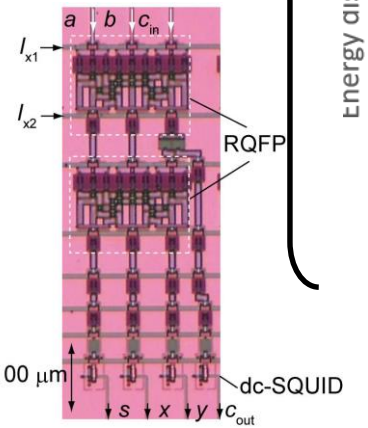
2033 ("1 nm")

Source: IRDS '17
More Moore chapter

Energy ×4, Delay ×3

For full adder function

RQFP = Reversible Quantum Flux Parametron (Yokohama U.)



Energy & delay for full adder cell

2017 ("10 nm")

2033 ("1 nm")

RQFP FA @ 300 K

×1,000 W/W

RQFP FA @ 4K

kT @ *T* = 300 K

kT @ *T* = 4 K

Data from T. Yamae, ASC '18

CV² logic node energy

CV/I delay, s

Energy dissipation for full adder operation, J

Full adder delay / Clock period, s

Exponential Scaling of Efficiency?

- Can we do *better than linear* scaling of dissipation with speed? → **YES!**
  - Some observations from Pidaparthi & Lent, 2018 →
- Landau-Zener '32 (!) formula for quantum transitions in *e.g.* atomic scattering problems with a missed level crossing…

$$P_{\mathrm{D}} = \mathrm{e}^{-2\pi\Gamma}$$

  - Shows that the probability of exciting the (dissipative) high-energy state scales down *exponentially* as a function of speed…
    - This *exponential* adiabaticity is a commonly-seen feature of many quantum systems!
- ∴ Dissipation-delay *product* has ***no lower bound*** for quantum adiabatic transitions!
  - Also… With *superadiabaticity* a.k.a. *shortcuts to adiabaticity*, we can do even better!
    - Approach 0 diabaticity even @ very *fast* speeds!
      - More on this later…

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Open Access Article

Exponentially Adiabatic Switching in Quantum-Dot Cellular Automata

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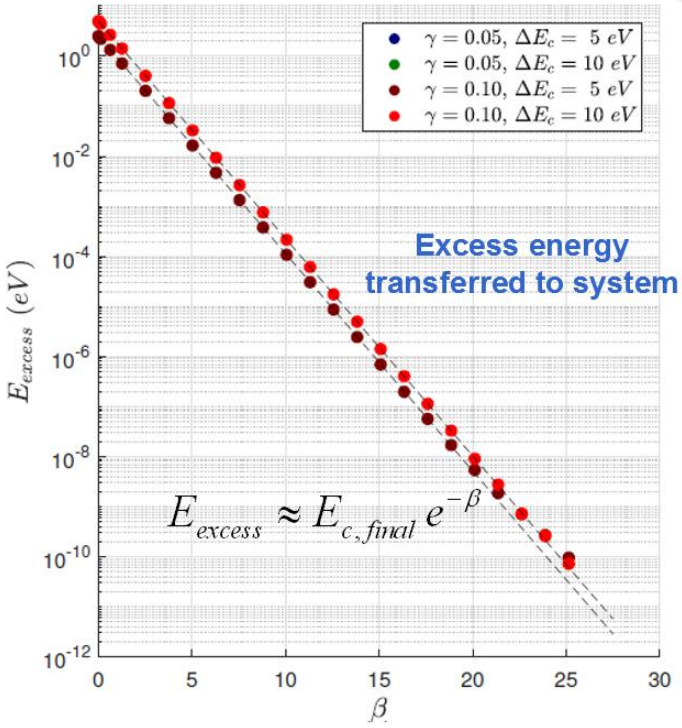
(This article belongs to the Special Issue Quantum-Dot Cellular Automata (QCA) and Low Power Application)



Ballistic Reversible Computing

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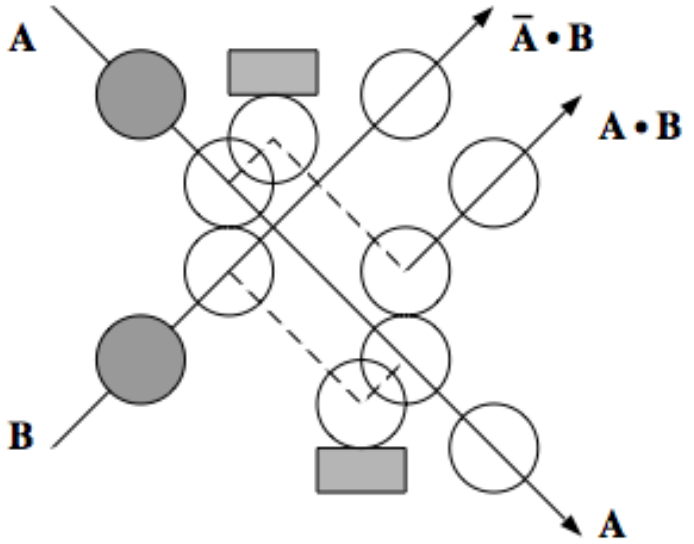
- Can we envision reversible computing as a *deterministic* elastic scattering process?
- Historical origin of this concept:
  - Fredkin & Toffoli's *Billard Ball Model* of computation ("Conservative Logic," IJTP 1982).
    - Based on elastic collisions between moving objects.
    - Spawned a subfield of "collision-based computing."
      - Using localized pulses/solitons in various media.



- No power-clock driving signals needed!
  - Devices operate when data signals arrive.
  - The operation energy is carried by the signal itself.
    - Most of the signal energy is preserved in outgoing signals.
- However, existing design concepts for ballistic computing invoke implicitly *synchronized* arrivals of ballistically-propagating signals…
  - Making this work in reality presents some serious difficulties, however:
    - Unrealistic in practice to assume precise alignment of signal arrival times.
      - Thermal fluctuations & quantum uncertainty, at minimum, are always present.
    - Any relative timing uncertainty leads to chaotic dynamics when signals interact.
      - Exponentially-increasing uncertainties in the dynamical trajectory.
    - Deliberate resynchronization incurs an inevitable energy cost.
- Can we come up with a new ballistic model that avoids these problems?

Asynchronous Ballistic Reversible Computing

in Superconducting Electronics (LDRD at Sandia)

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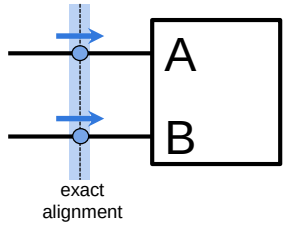
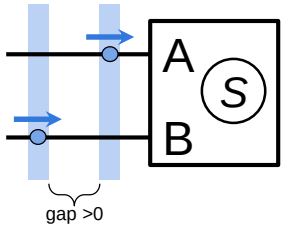
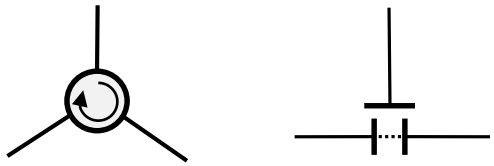
- **Problem:** Conservative (dissipationless) dynamical systems generally tend to exhibit chaotic behavior…
  - This results from direct nonlinear *interactions* between multiple continuous dynamical degrees of freedom (DOFs)
    - *E.g.*, positions/velocities of ballistically-propagating pulses
- **Core insight:** In principle, we can greatly reduce or eliminate this tendency towards dynamical chaos…
  - We can do this by *avoiding* any direct interaction between continuous DOFs of different ballistically-propagating signals
- Require localized pulses to arrive *asynchronously*—and furthermore, at clearly distinct, non-overlapping times
  - Device's dynamical trajectory then becomes *independent* of the precise (absolute *and* relative) pulse arrival times
    - As a result, timing uncertainty per logic stage can now accumulate only *linearly*, not exponentially
      - Only occasional re-synchronization will be needed
  - For devices to still be capable of doing logic, they must now maintain an internal discrete (digitally-precise) state variable
- No power-clock signals, unlike in adiabatic designs
  - Devices simply operate whenever data pulses arrive
  - The operation energy is carried by the pulse itself
    - Most of the energy is preserved in outgoing pulses
      - Signal restoration can be carried out incrementally
- **Goal of current project:** Demonstrate ABRC principles in an implementation based on fluxon dynamics in SCE



Synchronous Ballistic



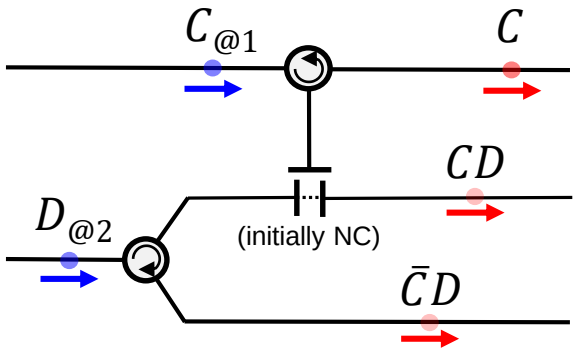
Asynchronous Ballistic



Rotary (Circulator)

Toggled Barrier

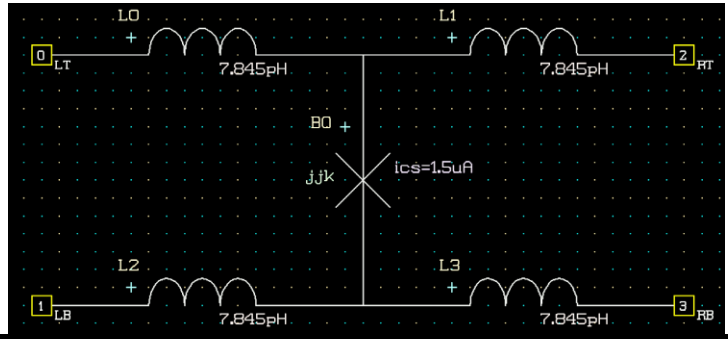
Example ABR device functions

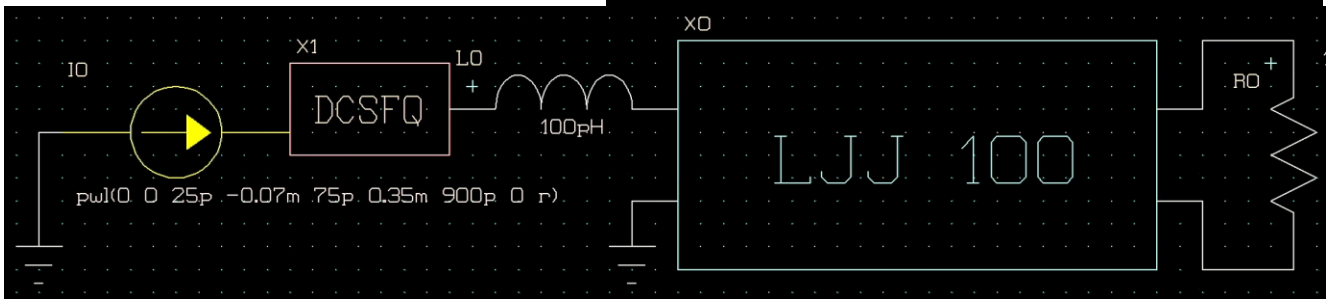


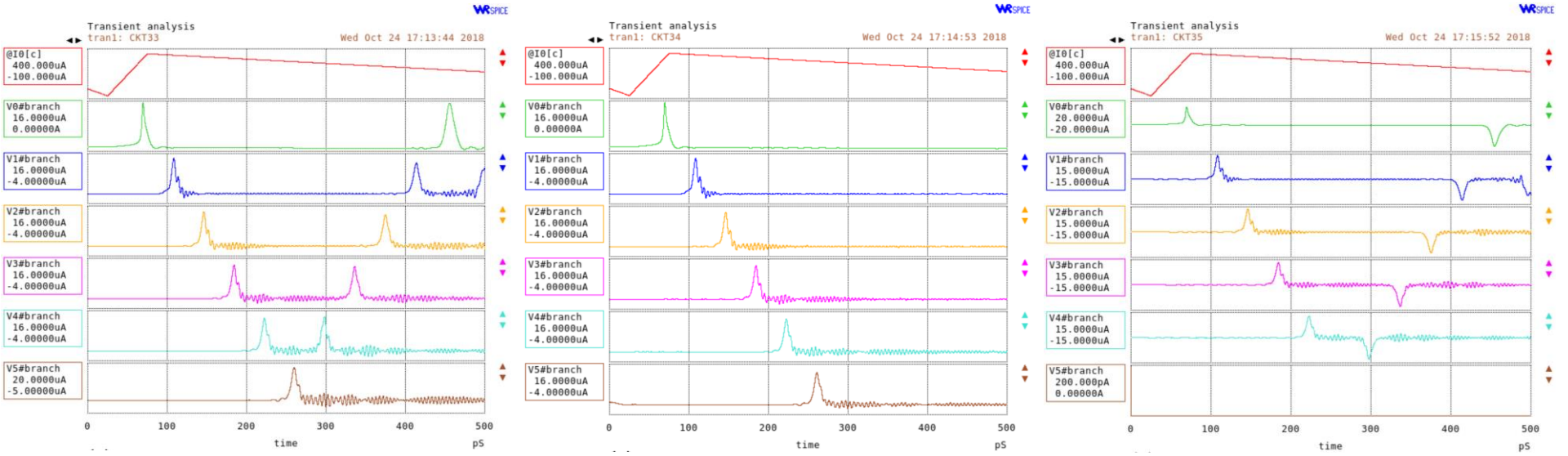
Example logic construction

WRSPICE simulations of discrete LJJ

- Preliminary effort completed in FY18
  - ASC (Sep. '18) 10.1109/TASC.2019.2904962
- Modeled buildable test structures in XIC
- Confirmed ballistic fluxon propagation
  - Confirmed predicted dLJJ line impedance of 16 Ω







Simplest Fluxon-Based ABRC Function

- Another FY18 task was: Characterize the simplest nontrivial ABRC device functionalities, given a few simple design constraints applying to an SCE-based implementation, such as:
  - (1) Bits encoded in fluxon polarity; (2) Bounded planar circuit conserving flux; (3) Physical symmetry.
- Determined through theoretical analysis that the simplest such function is the following

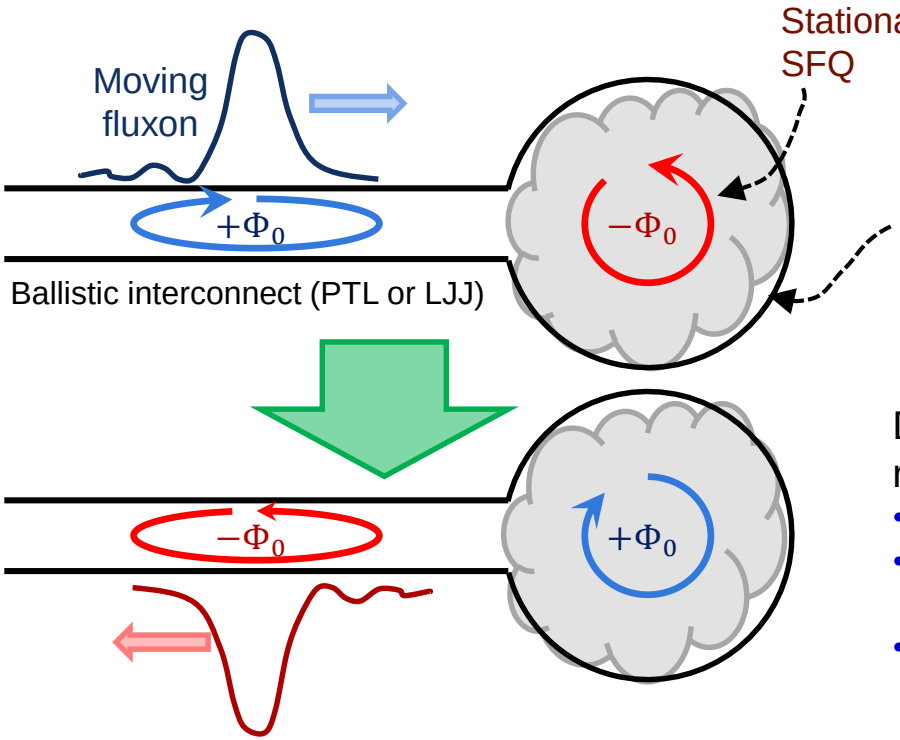
1-Bit, 1-Port Reversible Memory Cell (RM):

- Due to its simplicity, this is the preferred target for our detailed circuit design efforts looking forwards…

RM Transition Table

Input Syndrome		Output Syndrome
+1(+1)	→	(+1)+1
+1(−1)	→	(+1)−1
−1(+1)	→	(−1)+1
−1(−1)	→	(−1)−1

RM icon:

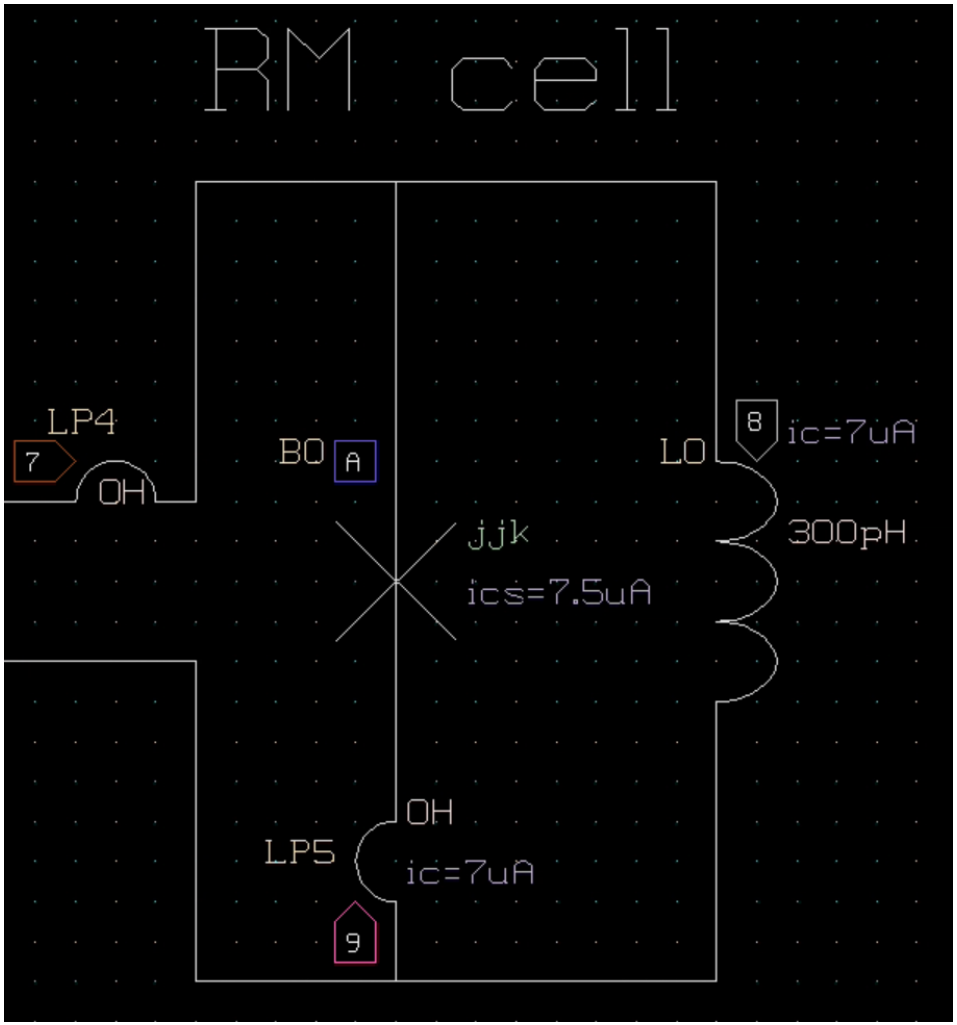


Some planar, unbiased, reactive SCE circuit (to be designed) w. a continuous superconducting boundary
- *Only* contains L's, M's, C's, and *unshunted* JJs
- Junctions should mostly be *subcritical* (avoids R_N)
- Conserves total flux, approximately nondissipative

Desired circuit behavior (NOTE: conserves flux, respects T symmetry & logical reversibility):
- If polarities are opposite, they are swapped (shown)
- If polarities are identical, input fluxon reflects back out with no change in polarity (not shown)
- *Elastic scattering* type interaction: Input fluxon kinetic energy is (nearly) preserved in output fluxon

RM—First working implementation!

- Erik DeBenedictis: “Try just strapping a JJ across that loop.”
  - This actually works!
- JJ sized to = about 5 LJJ unit cells (~1/2 pulse width)
  - I first tried it twice as large, & fluxons annihilated instead…
    - 🤔 “If a 15uA JJ rotates by 2π, maybe ½ that will rotate by 4π”
- Loop inductor sized so 1 SFQ will fit in the loop (but not 2)
  - JJ a bit below critical with 1
- WRspice simulations with +/−1 fluxon initially in the loop
  - Uses `ic` parameter, & `uic` option to `.tran` command
    - Produces initial ringing due to overly-constricted initial flux
      - Can damp w. small shunt *G*



WRspice simulation results

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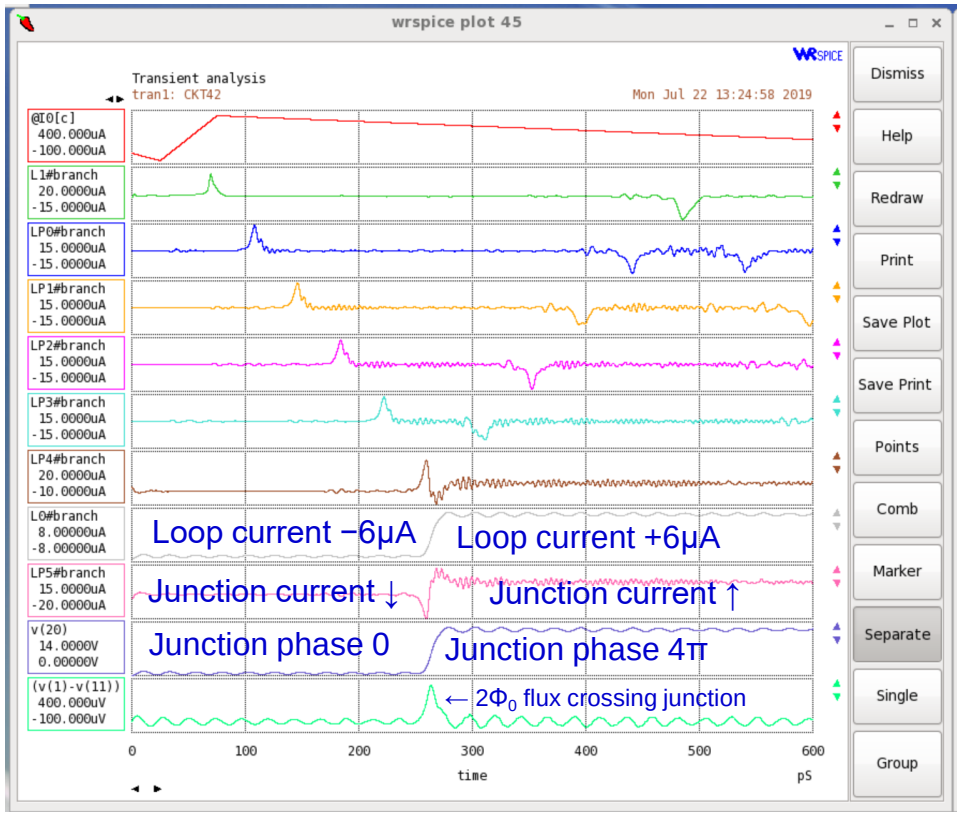
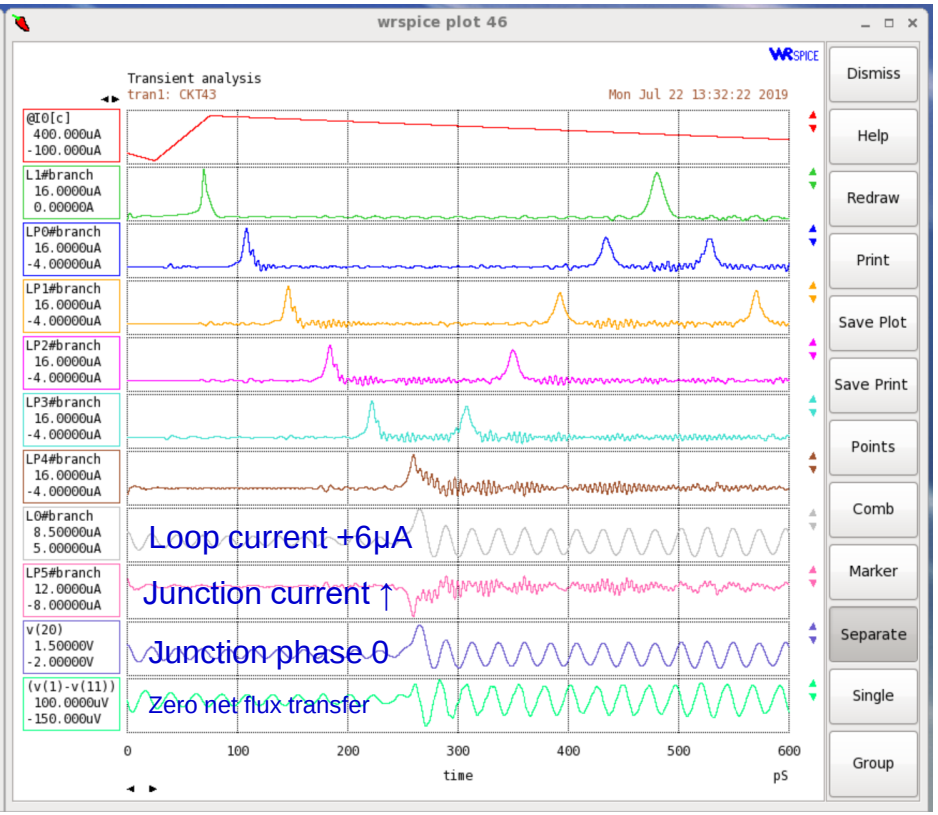
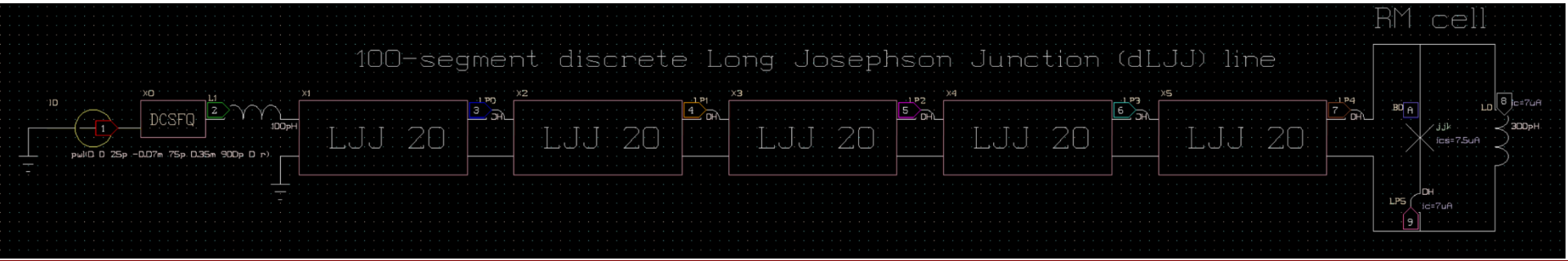
Polarity mismatch → Exchange

Polarity match → Reflect (=Exchange)

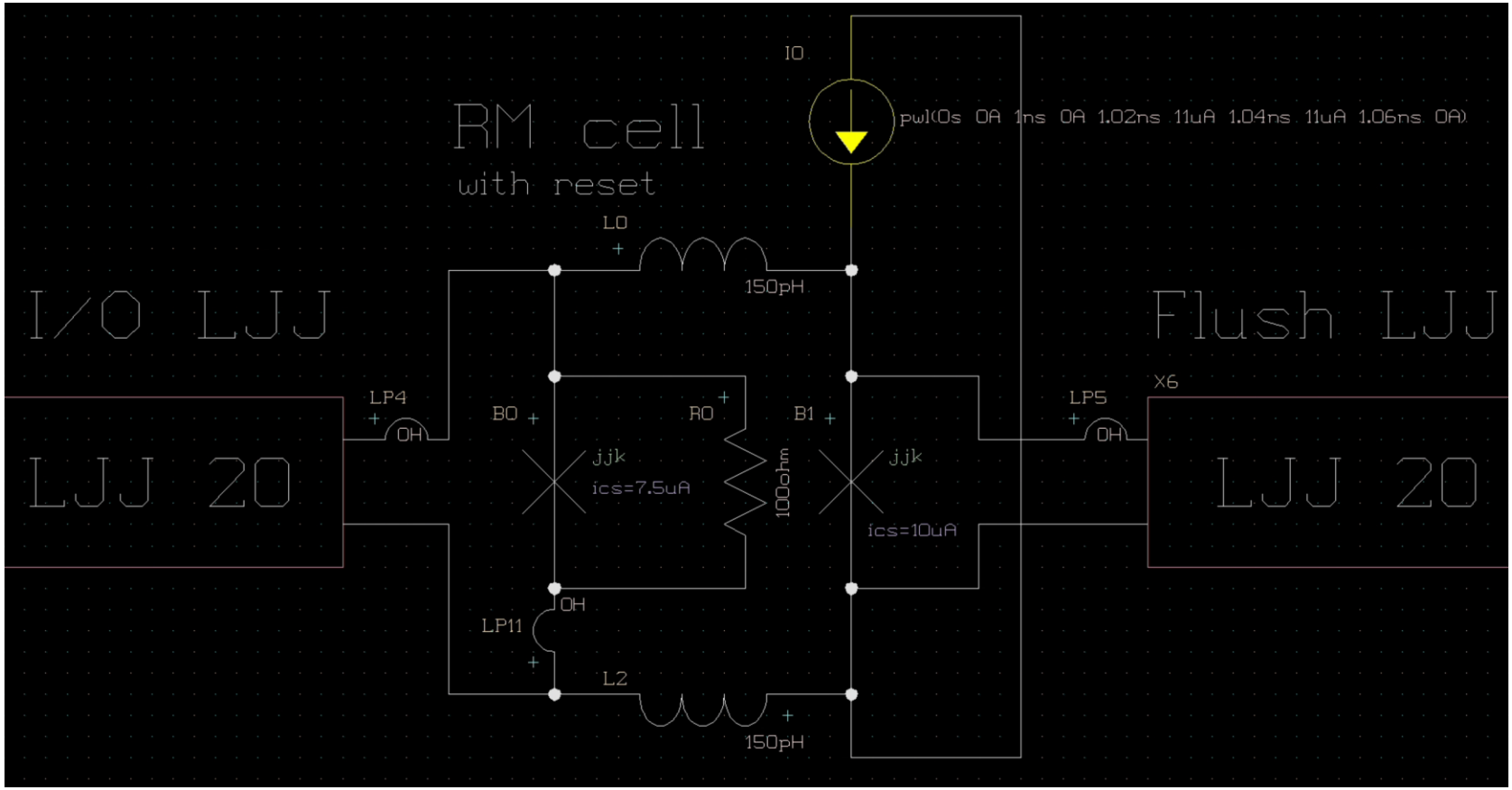






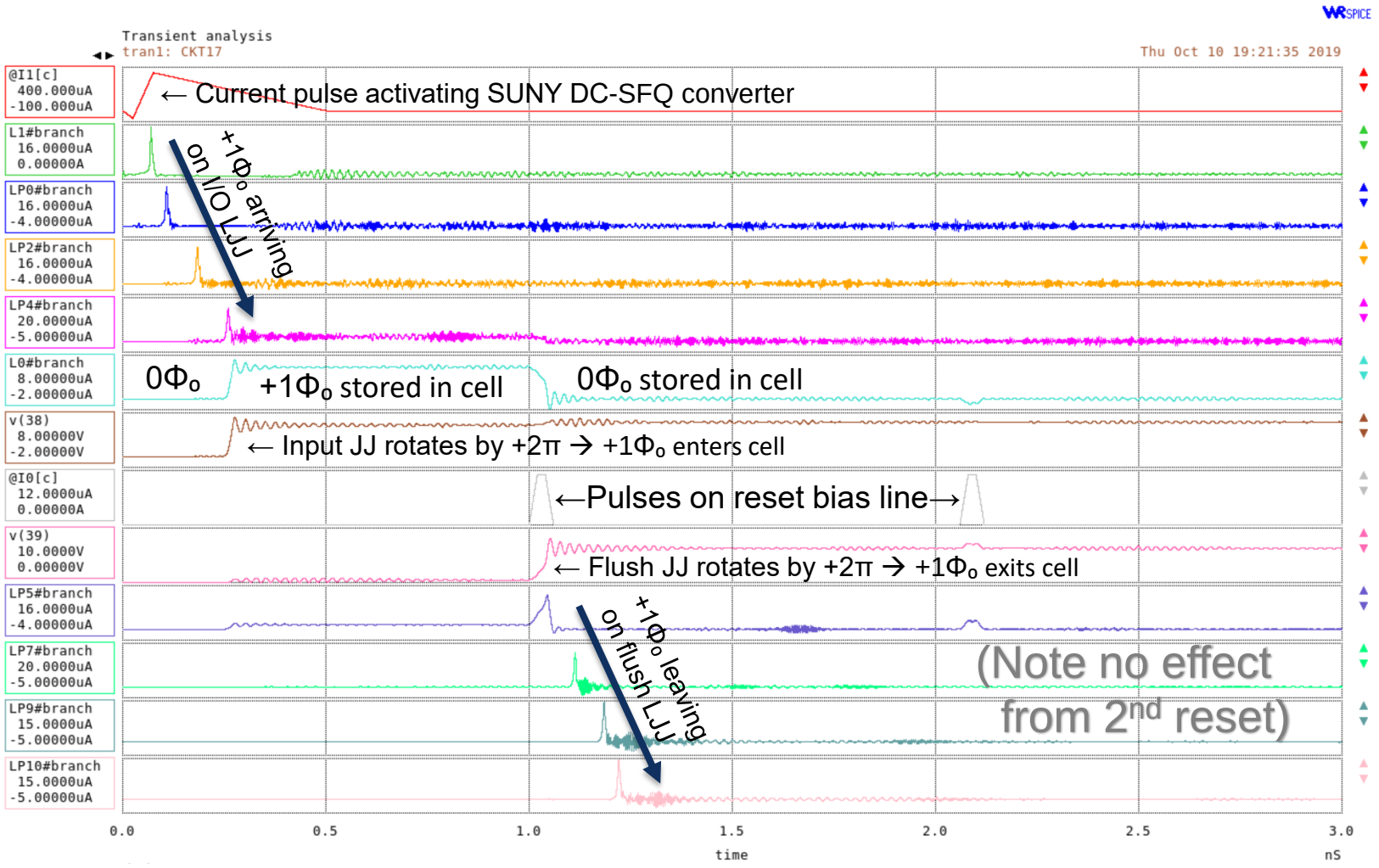
Resettable version of RM cell

- For testing—apply current pulse of appropriate sign to flush the stored flux (the pulse here flushes out positive flux)
  - To flush either polarity → Just do both (±) resets in succession

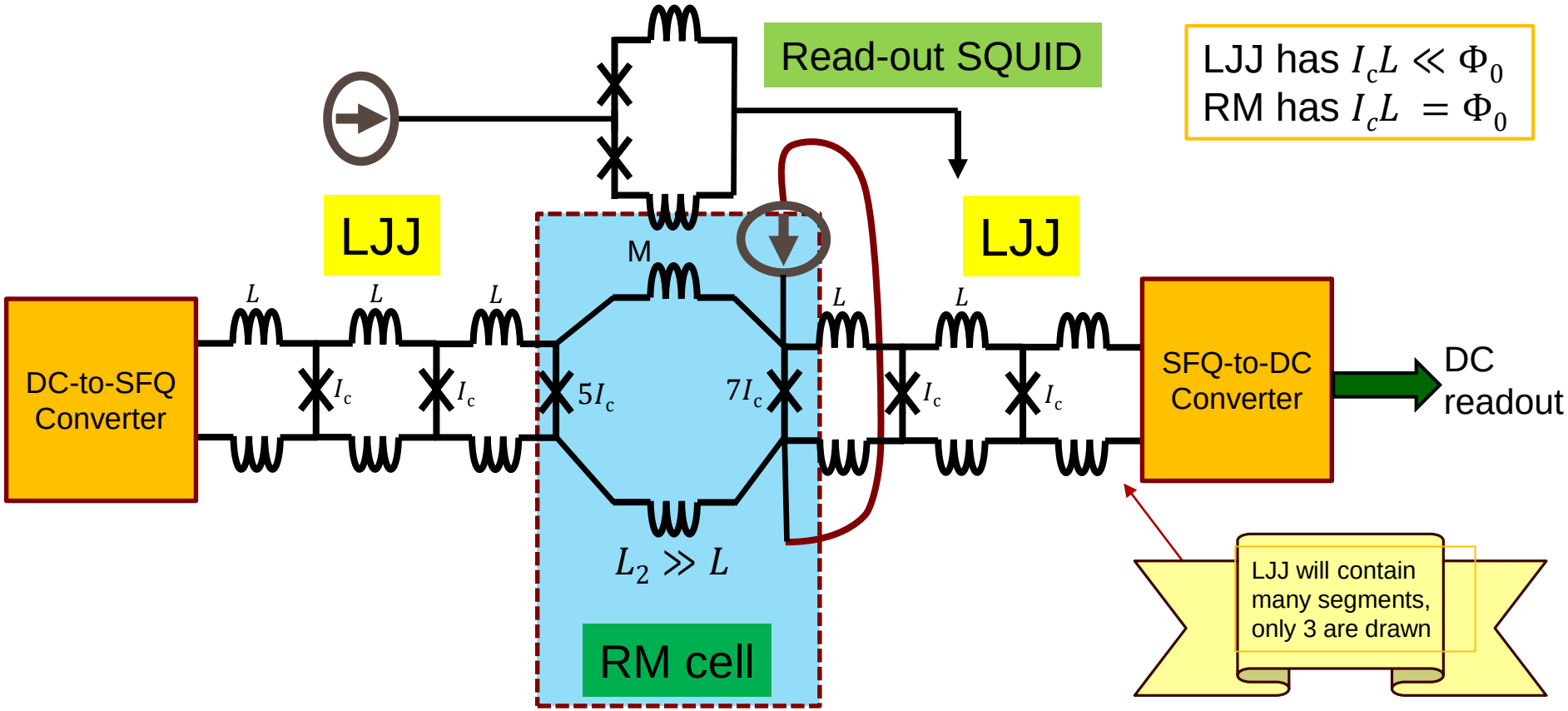


SPICE simulation of RM cell reset

- Simulates as expected (one-polarity reset shown)
  - Reset of an already-flushed cell is a no-op

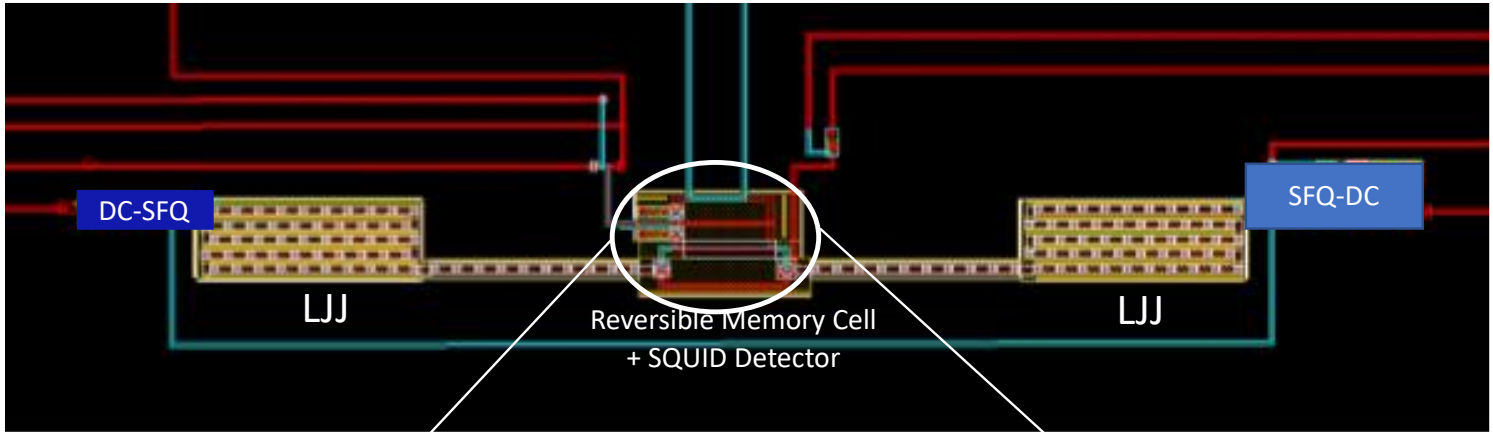


Sketch of SQUID-based test setup

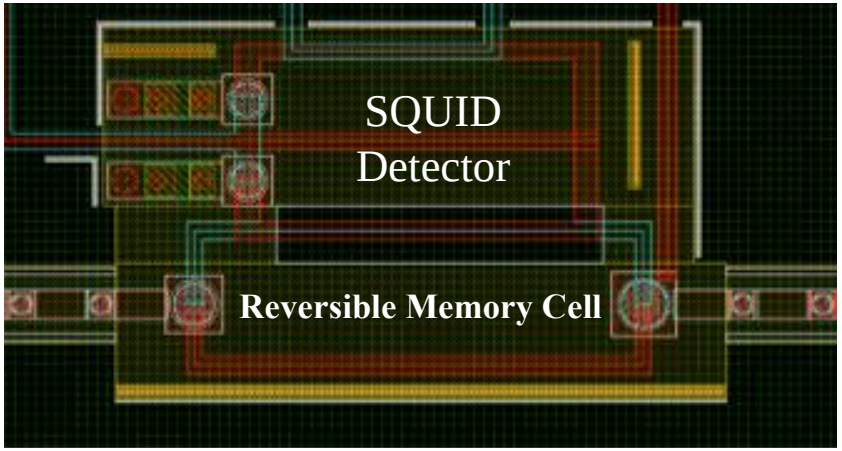


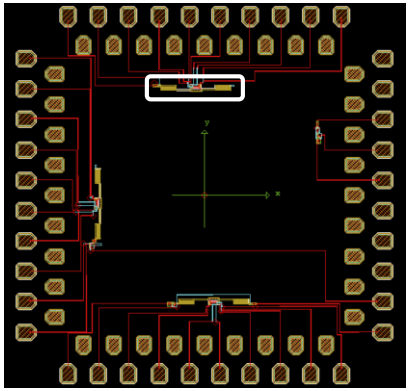
Test Circuit Layout

- Circuit elements were rescaled for operation @ 4K ($10\times$ larger I_c values)
- Complete test circuit layouts were generated for SeeQC's 4-layer Nb process
  - Low $J_c = 1\ \mu A/\mu m^2$ increases layout dimensions, reduces manufacturing variation
- A 5×5 mm die with 4 test circuits was taped out on Feb. 17th



DC-SFQ & SFQ-DC designs are from SeeQC (obscured due to NDA)





Some Next Steps re: RM Cell

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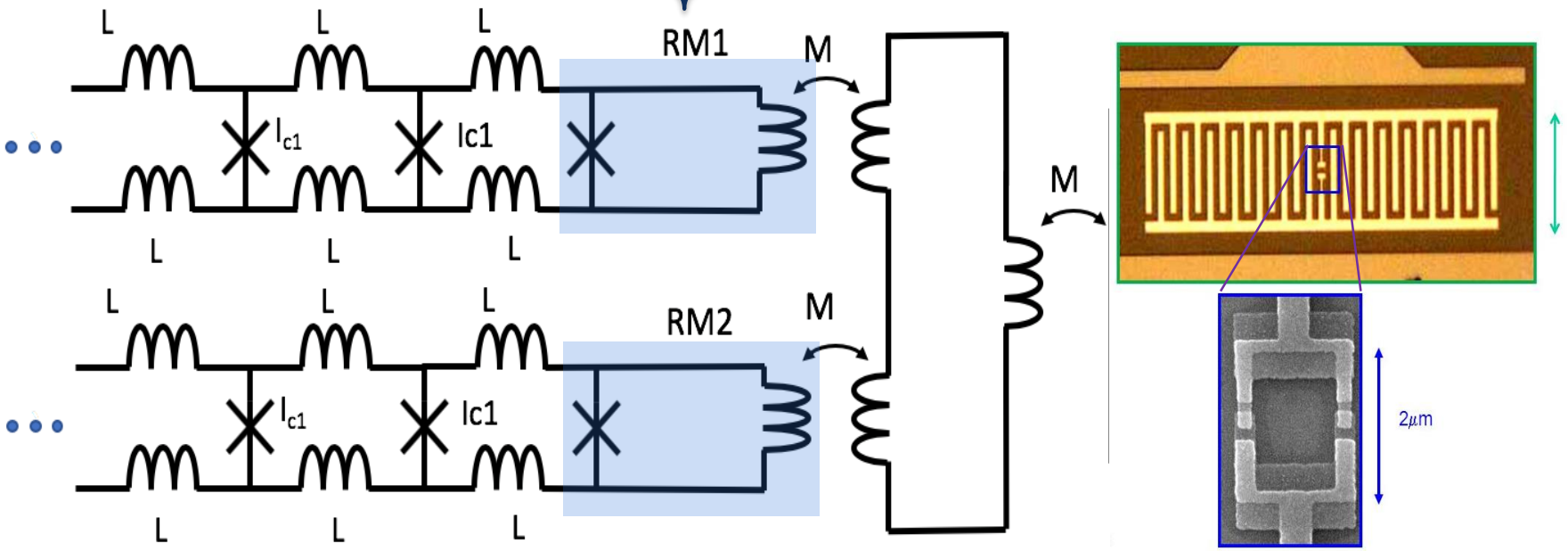
- Detailed design & empirical testing of a physical prototype.
  - Experimentally measure the fabricated circuits in our lab.
- Need to understand better, at a theoretical level, the engineering requirements for such circuits to work properly.
  - And, can we generalize this understanding to more complex cases?
    - Goal: Design circuits for a wide variety of other ABRC functions.
- Carry out further elaborations of design to fine-tune dynamic response for high-fidelity preservation of pulse shape.
  - Should be able to use 3D physics modeling, solve inverse problem to craft a very high-quality custom layout (similar to metamaterials).
- Investigate applications, *e.g.*:
  - Can this be extended to become the basis for a dense memory fabric?
    - Develop row/column interface logic
    - Optimize the cell design for more compact area
      - Try smaller loop inductance, larger I_c in I/O junction
  - Can this cell have utility in quantum computer control circuits?
    - See next slide

RM Cells for Qubit Control?

Idea by Rupert Lewis

RM cells can be reconfigured with nearly zero energy dissipation near the qubit!

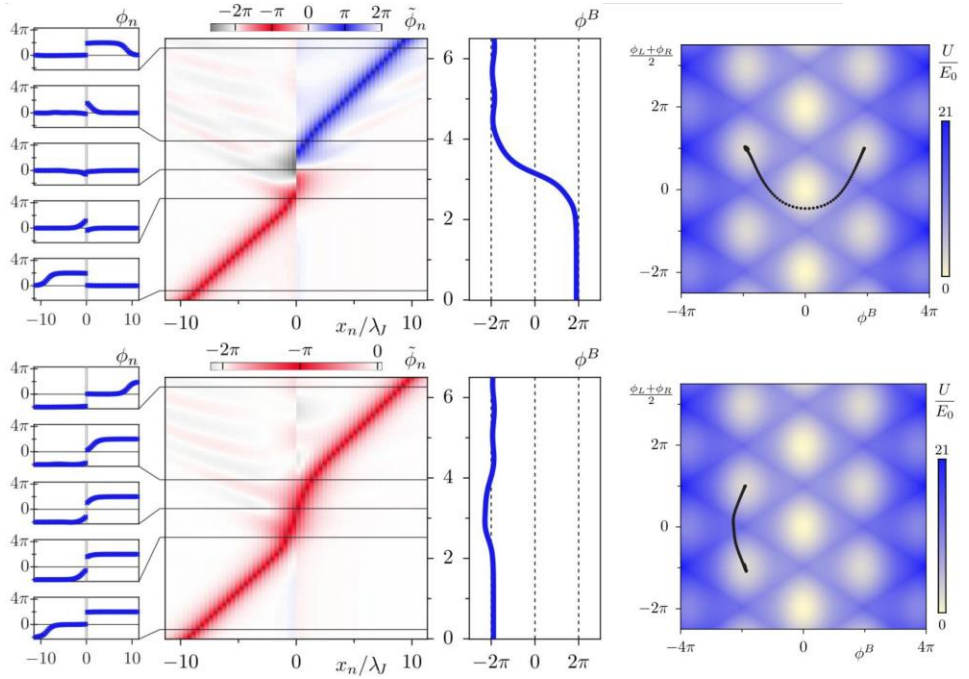


flux biasing of a transmon qubit tunes its frequency

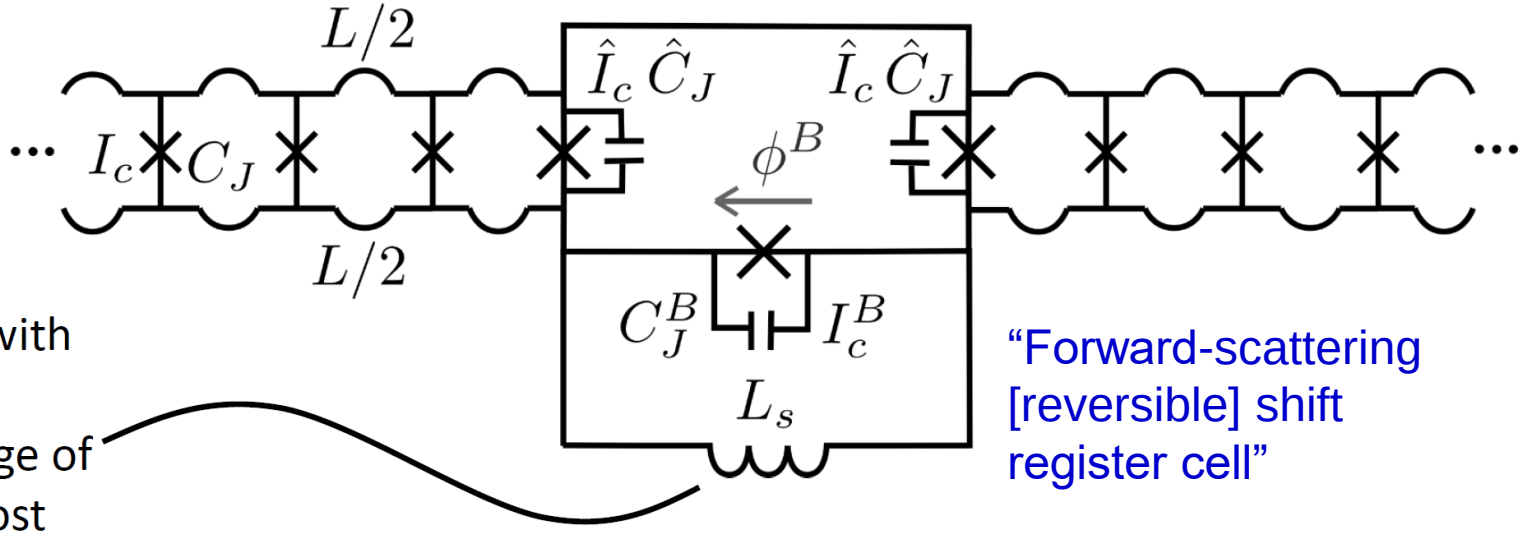
Note: Entire structure scales well to a low-J_c process for decreased fluxon energy and even *lower* energy dissipation, while maintaining good noise immunity at QC temperatures (~10s of mK)

Related Work at LPS

- Kevin Osborn (w. W. Wustmann & L. Yu) at LPS have recently also begun exploring stateful gates in the ABRC family…
  - This one is functionally similar to the RM cell, except the output comes out a different port
- Function was verified in detailed simulations →
  - Error margins are ≥30%
  - Peak efficiency ≥90%



(Related to our 1-bit gates)



Inductor loop "precharged" with 1 SFQ.
Ls allows storage of one SFQ, at most

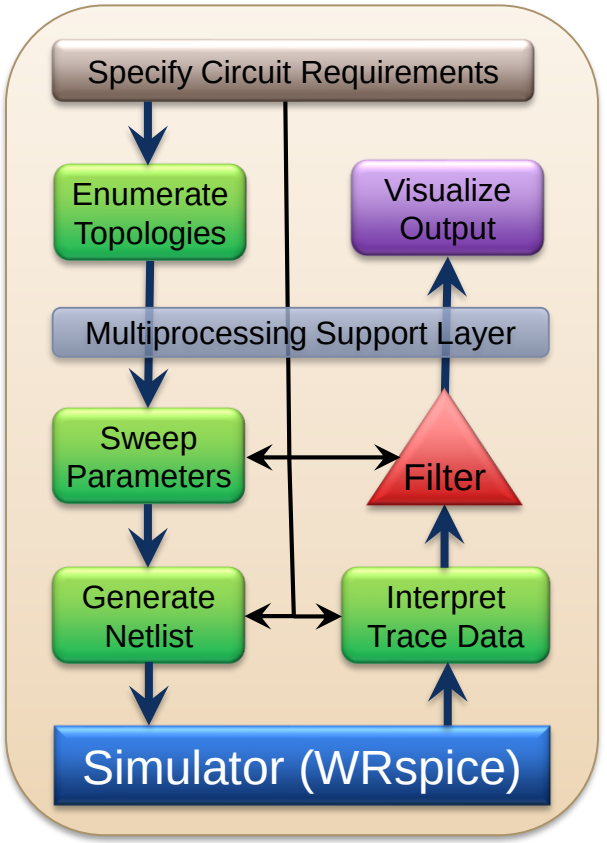
"Forward-scattering [reversible] shift register cell"

Automation of Circuit Discovery

Undergraduate outreach – Work currently delegated to a senior design team at the ECE department, FAMU-FSU College of engineering

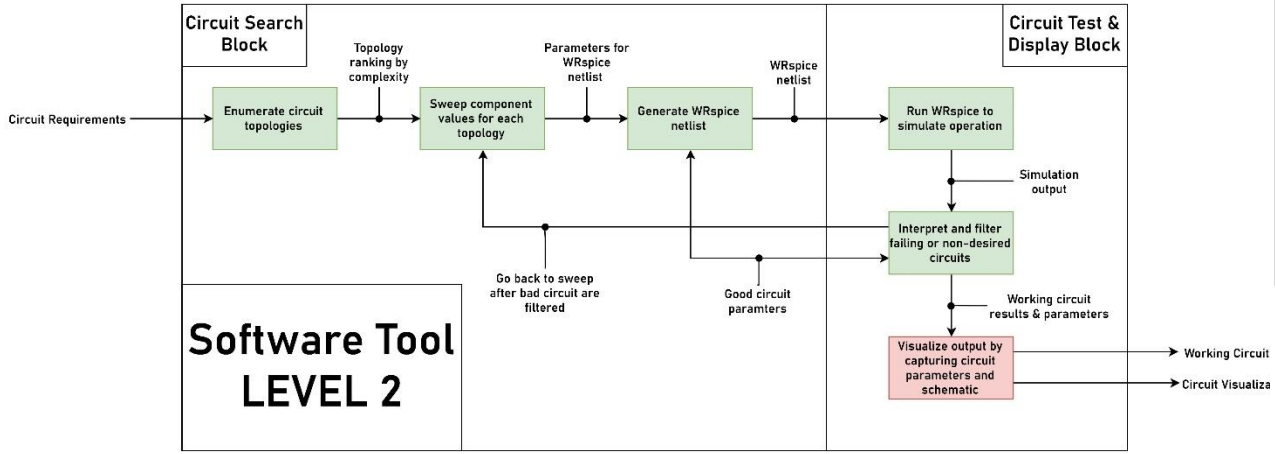
- Due to the novelty of our new logic style, the principles to design much improved/more complex ABRC circuits aren't obvious…
  - **Solution:** Automate our circuit-discovery methodology!
- Started developing a new tool, named **SCIT**
  - ***Superconducting Circuit Innovation Tool***
- Outline of the SCIT processing flow:
  1. Define circuit design requirements
  2. Enumerate possible circuit topologies
     - In order of increasing complexity
  3. Delegate topologies to MPC nodes
  4. Sweep over device parameter space
  5. Generate a netlist for each test design
  6. Simulate netlist locally (in e.g. WRspice)
  7. Interpret & summarize resulting traces
  8. Filter for results with desired properties
  9. Facilitate visualization of candidate designs

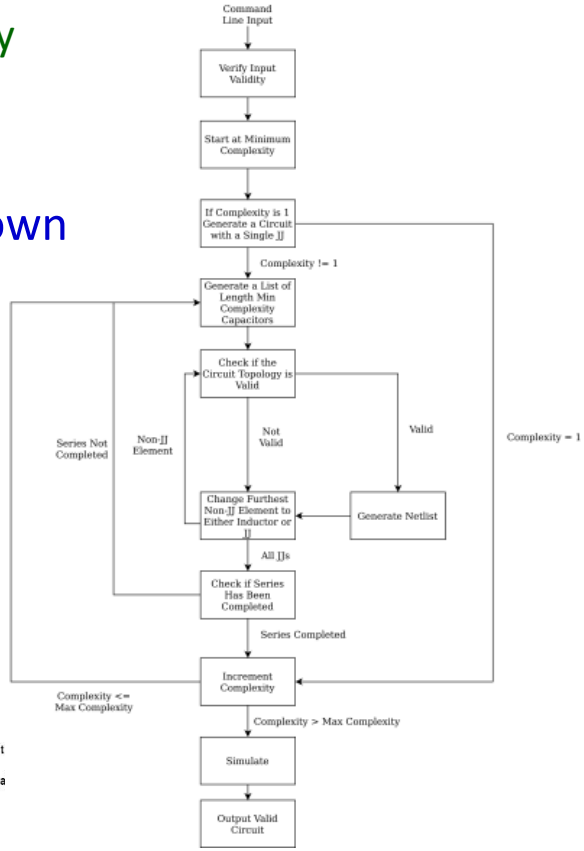
SCIT Software Architecture



SCIT Effort – Present Status

- Multi-year Senior Design projects in ECE Department, FAMU-FSU College of Engineering
  - Department chair **Sastry Pamidi** and course instructor **Jerris Hooker** have some superconductivity expertise
    - College has historical ties with adjacent Mag Lab (NHMFL)
  - This year's students:
    - Fadi Matloob, Frank Allen, Oscar Corces, James Hardy
- Present status:
  - Some software components already functional
  - Project temporarily stalled due to university shutdown
    - Project file server not accessible ☹



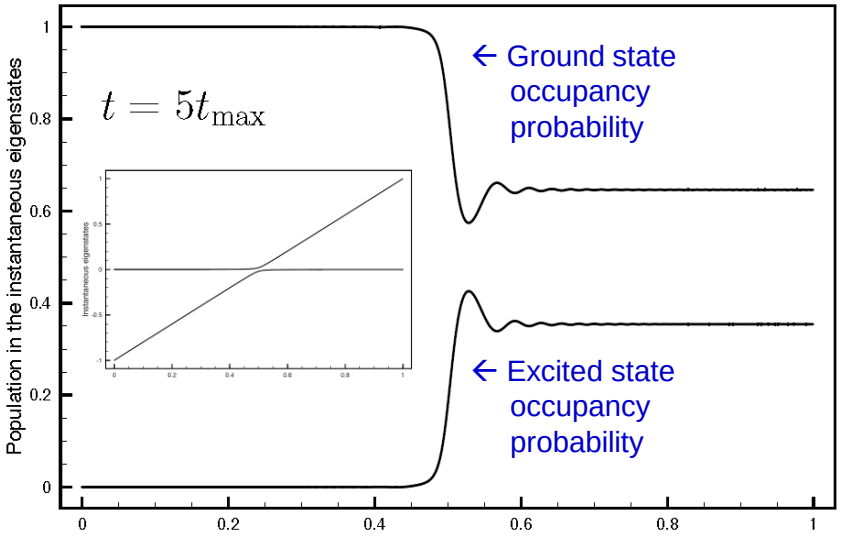


Superadiabaticity / Shortcuts to Adiabaticity (STA)

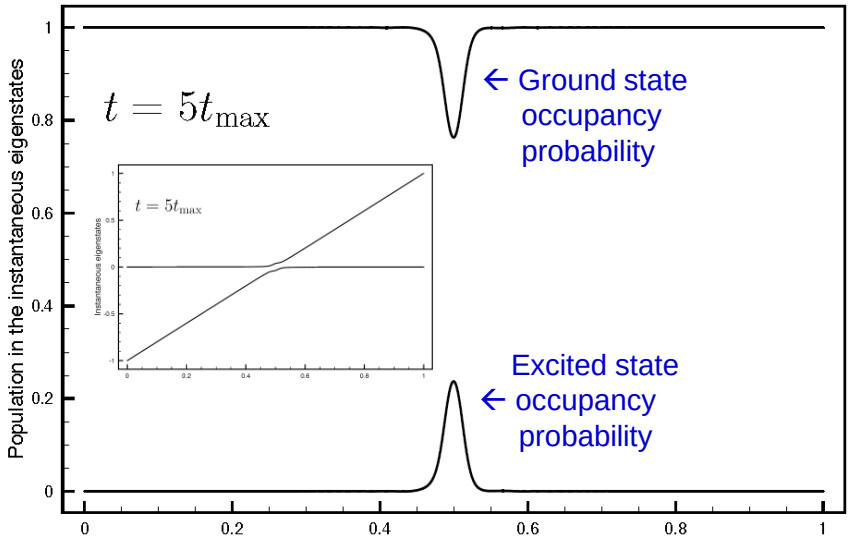
- A line of fundamental physics research showing that we can theoretically attain or approach 0 diabaticity (dissipation) even in evolutions occurring at fast, *constant* speeds.
  - This relates to my more general point from earlier about the fundamental dissipationlessness of known unitary evolutions.
- Some (at least theoretical) applications of this so far:
  - *Fast* Carnot-efficient heat engines!
  - Fast general thermodynamic engines for manipulating the state of quantum systems (*e.g.* Maxwell's Demon type setups).
  - Faster superconducting circuits for controlling quantum computers!
- Why not also investigate whether these methods can be used to achieve fast *classical* dissipationless reversible computing?
  - And whether this theory can translate to engineering practice…

Example Use of STA: Fast Dissipationless Transitions of a Quantum Dot System

- Credit: David Guéry-Odelin (U. Toulouse)
- Example system:
  - A quantum-dot system previously described by Lent for use in reversible logic, undergoing an (externally-driven) transition between two different Hamiltonians.
- Figures show occupancy of ground (top) & 1st excited eigenstate (bottom).
  - t is the total time over which the transition takes place (adjustable)
  - t_{max} is a somewhat arbitrary duration when the system is transitioned at certain designated "maximum speed" (at which dissipation is near maximum)
- If system later relaxes from an excited state → state energy will be dissipated.
  - But, we assume here that the relaxation time is large compared to the transition time itself.
- Both figures below show an example calculation at which transition speed = 1/5 maximum
  - But, the same method works in principle to achieve zero dissipation at *any* speed!



Normal quantum adiabatic process: Substantial excitation/dissipation



Using counterdiabatic protocol: Zero net excitation/dissipation

Open Problems in STA for RC

- Can any of the various STA protocols that theorists have described actually be implemented *practically*?
  - Need more exploration of engineering mechanisms for doing so.
  - What are the limits on these methods' efficiency *in practice*, if any?
- Can the STA protocols be applied (in a complete way) to various specific examples of physical implementations of reversible computing?
  - In particular (for our project): Is there any way to apply them to fluxon dynamics, specifically in ABRC-type circuits?
    - Certain classical-quantum equivalences suggest yes!
      - See next slide
    - Could an appropriate counterdiabatic Hamiltonian be introduced spatially, through appropriate tailoring of the structure at which the fluxon dynamics occurs?
- However, best way to proceed is still very unclear!
  - This is a wide-open research area…

Shortcuts to Fluxon Adiabaticity?

Work in progress with Karpur Shukla (CMU / Flame U. / Brown U.)

- Jarzynski ‘13 [1] discusses *dissipationless classical driving*, which can be viewed as an example of a classical analogue to quantum shortcuts to adiabaticity (STA)
  - Prescribes theoretical modifications to driving Hamiltonian
- Okuyama & Takahashi ‘17 (10.7566/JPSJ.86.043002) builds a more complete theory of classical STA on this foundation…
  - *Korteweg-de Vries* (KdV) *hierarchy* characterizes conserved quantities
    - Gesztesy & Holden ‘97 [2] show how to modify the KdV hierarchy as needed to model the sine-Gordon equation—describes fluxons in LJJs!
- Takahashi ‘19 (10.7566/JPSJ.88.061002) goes on to discuss methods for *Hamiltonian engineering* in the context of adiabatic QC…
  - Can apply to engineering classical reversible transformations also?
    - Needs more study…

[1] C. Jarzynski, Phys. Rev. A **88**, 040101(R) (2013)
[2] F. Gesztesy and H. Holden, arXiv:solv-int/970710

Conclusion

- Some path to further **increase dissipation-delay efficiency** of superconducting circuits over the long term is needed.
  - **No *fundamental* limit** on this quantity is yet known!
- Inspired by **collision-based computing**, we have simulated the first concrete working example of an SCE circuit implementing one of the reversible functions in the new ABRC model of computation.
  - This is a **reversible memory (RM)** cell functionality requiring just 1 JJ.
  - Some of the key **next steps** for the RM cell development include:
    - **Empirically test** our first test chips once we get them back.
    - **Design additional test chips** for purposes of measuring energy dissipation.
    - **Identify additional functions** in the ABRC model that may be amenable to producing similarly straightforward implementations.
    - **Finish implementing circuit search tool** (SCIT) for more rapid discovery of circuits for more complex ABRC functionalities.
- In the bigger picture, there is a significant need to begin investigating new quantum (or quantum-inspired) techniques for reducing dissipation in reversible computational processes.
  - **Shortcuts-to-adiabaticity** (STA) is just one example of such an approach
  - **Other ideas:** Harness topological invariants, quantum Zeno effects, *etc.*
- Many possible paths still remain to be explored for **continuing to improve dissipation-delay efficiency** far into the future.