All-SiC Power Modules for Energy Storage Power Electronics

Ranbir Singh, Siddarth Sundaresan and Stan Atcitty

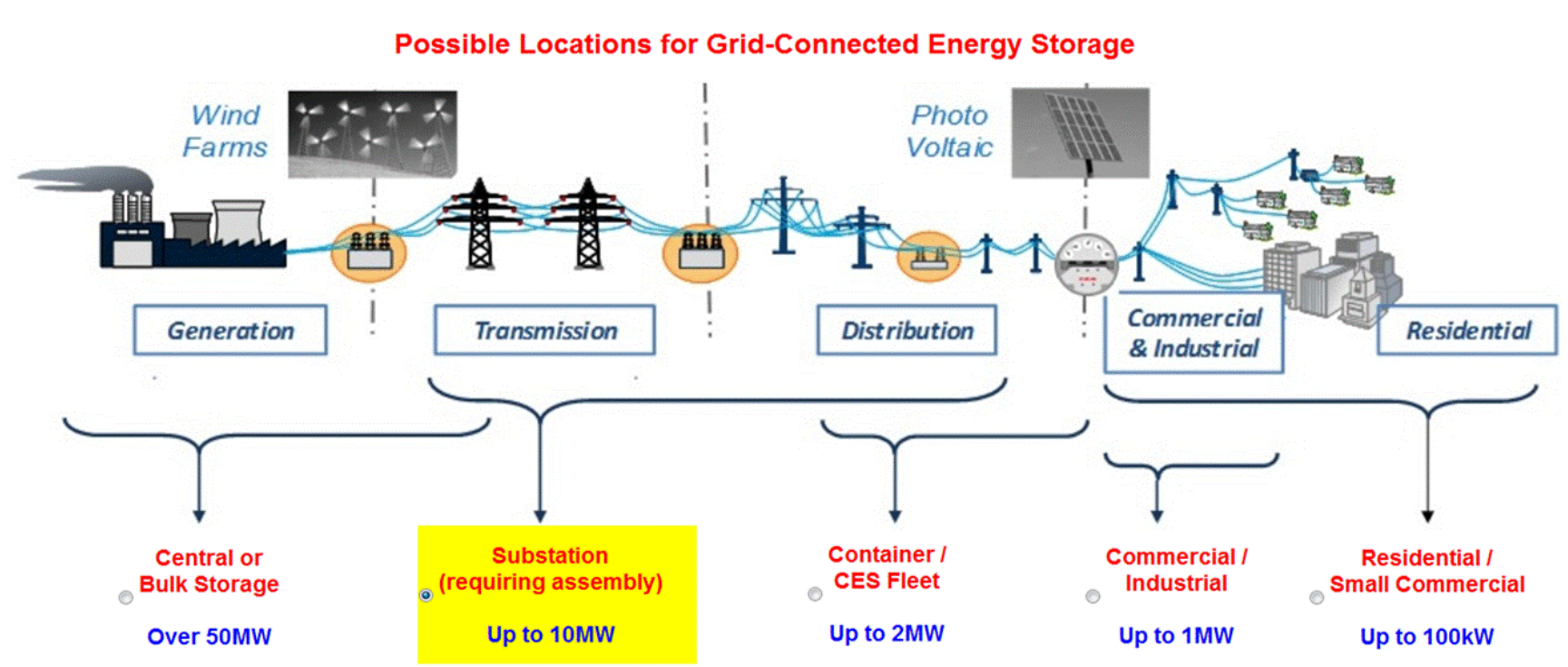
GeneSiC Semiconductor Inc.

Sandia National Labs

Acknowledgement: The authors thank Dr. Imre Gyuk for funding this work and Dr. Stan Atcitty for technical contributions. Sandia National Laboratories is a multi-mission laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SBIR Phase II Grant DE-SC0013816

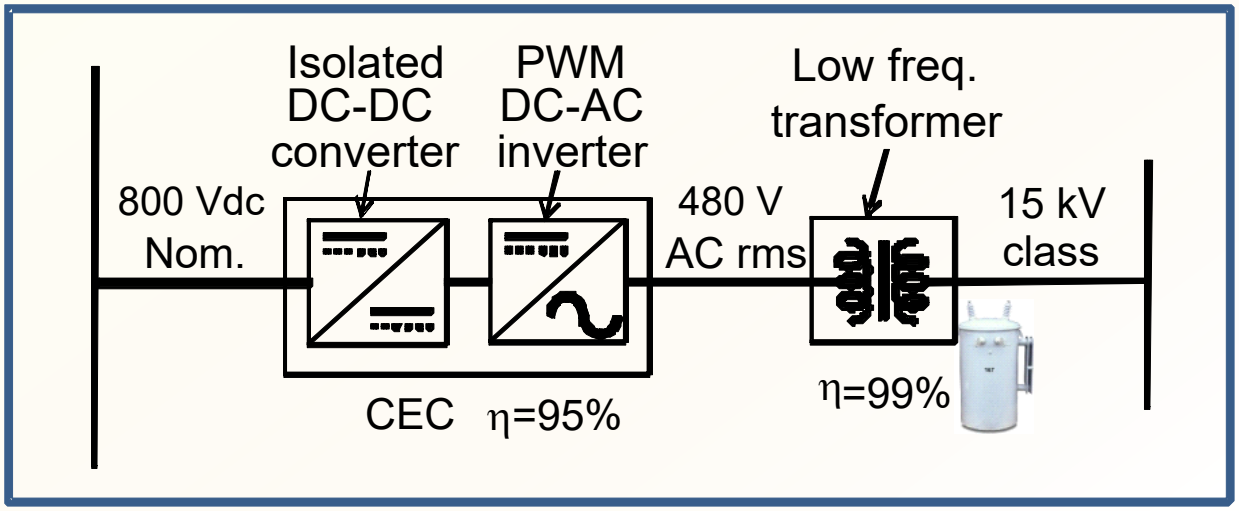
GeneSiC SEMICONDUCTOR

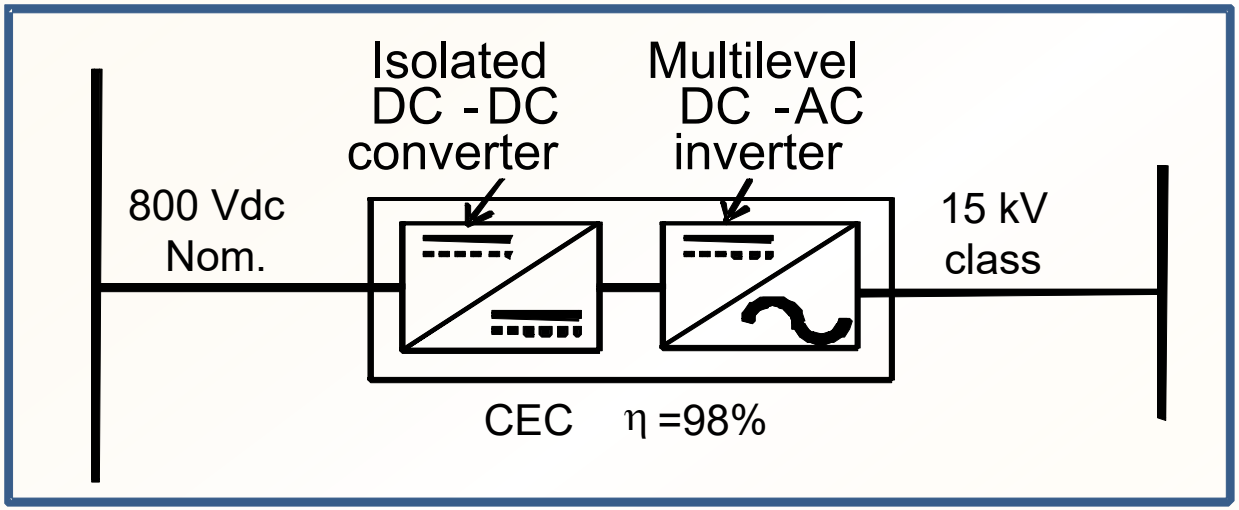
Energy Storage Opportunities at Medium Voltages (3-20 kV)



- Many Energy storage opportunities require power electronics that can enable conversion efficiencies needed for making energy storage viable
- Silicon Carbide high voltage devices will play a pivotal role

Battery Energy Storage Power Electronics Architectures





- Bidirectional, isolated DC-AC Power Conversion systems needed
- High Efficiencies are needed due to two-way power flow
- Compact systems help in wider deployments
- Low Frequency Transformer occupies space

Calculated Loss Comparisons at 1 MVA

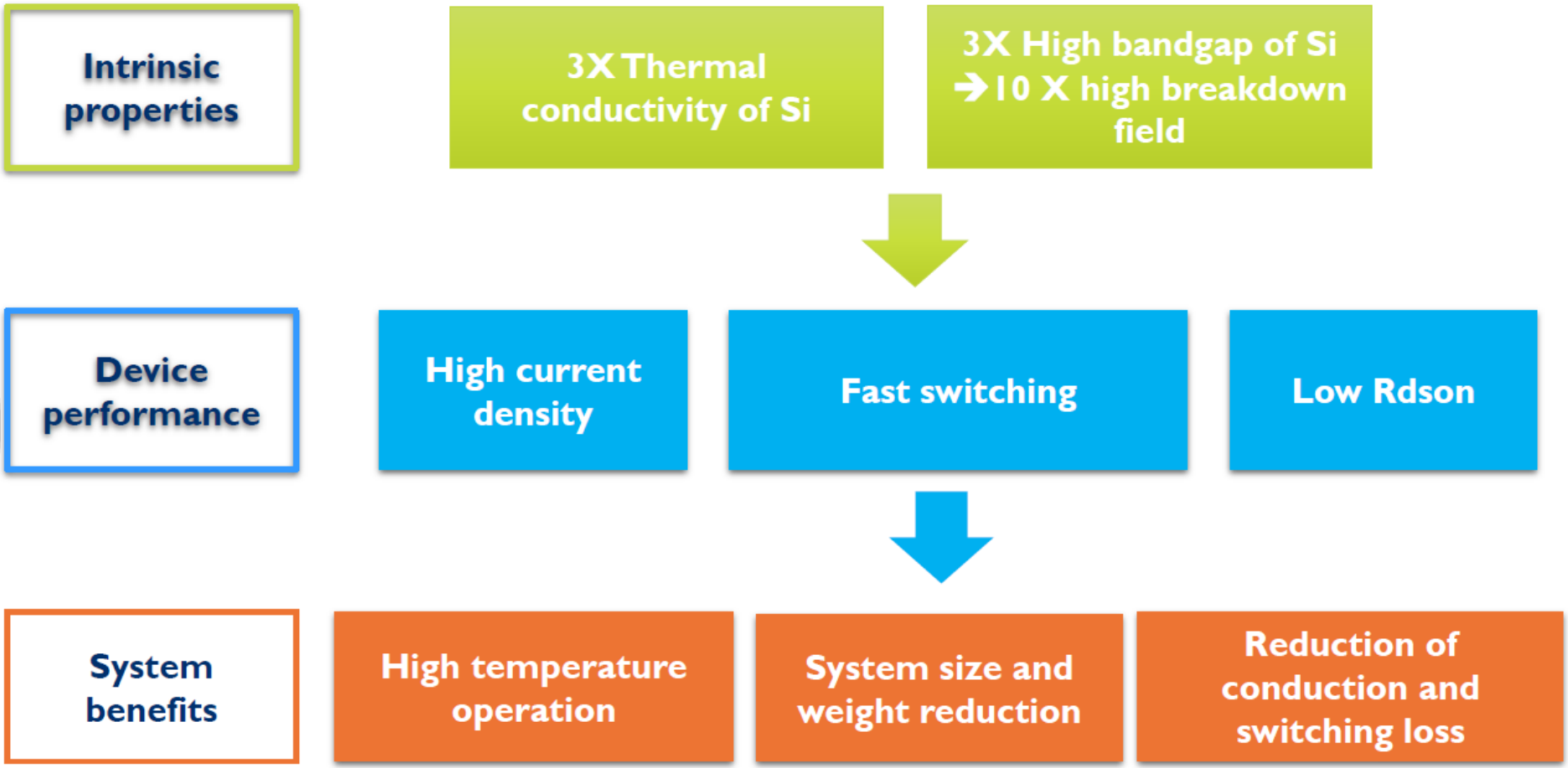
Table 1: Medium Voltage/Low Current Side loss even at 1 MVA operation.

Active Power (MW)	Reactive Power (MVAR)	Loss (W)
1	0	3064
0.8	0.6	4175
0.6	0.8	5330

Table 2: Low Voltage/ High Current Side Loss

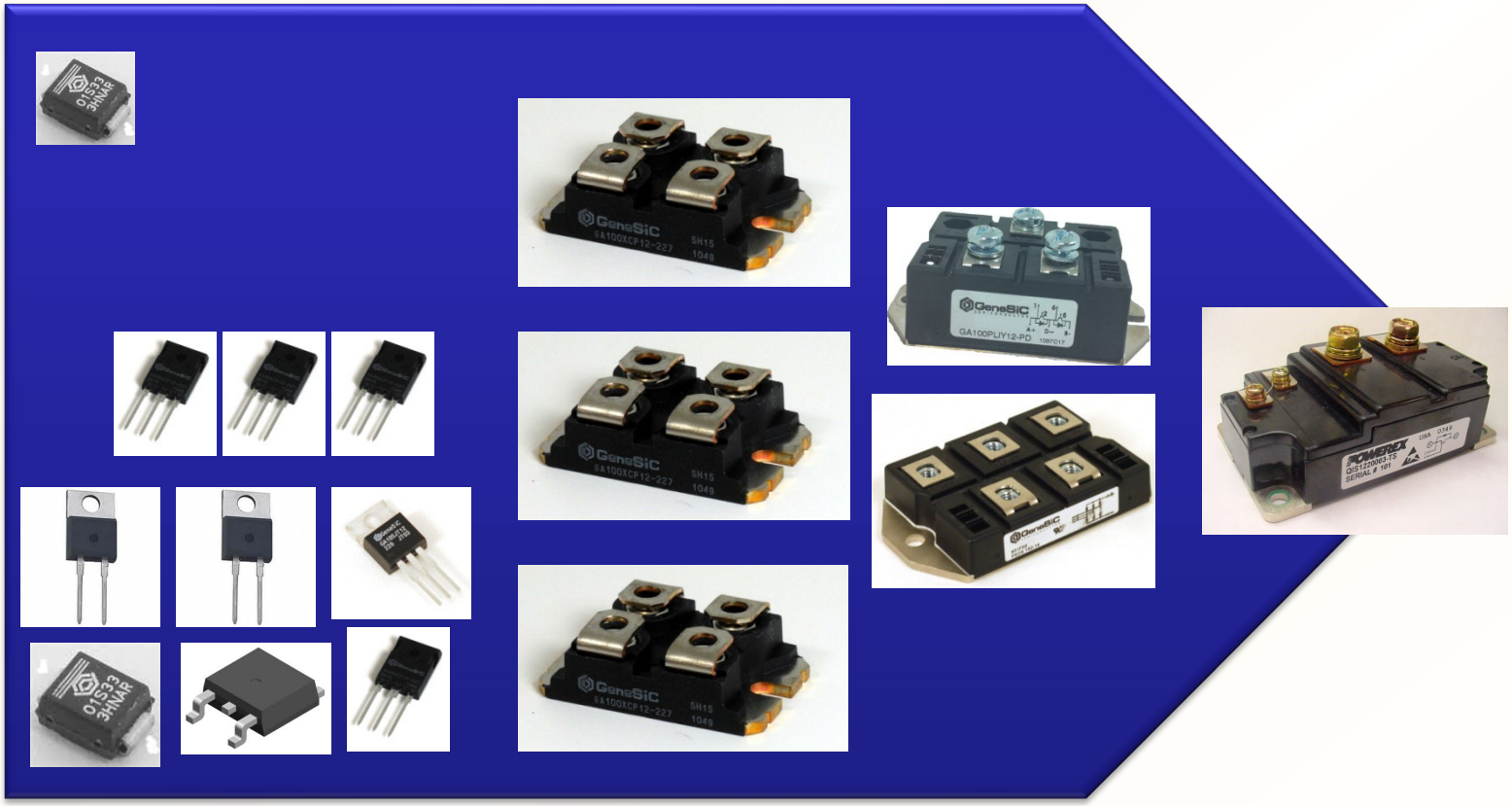
Active Power (MW)	Reactive Power (MVAR)	Loss (kW)
1	0	32
0.8	0.6	27
0.6	0.8	23

Why SiC Power Devices?



GeneSiC's Power Discrete and Module Roadmap

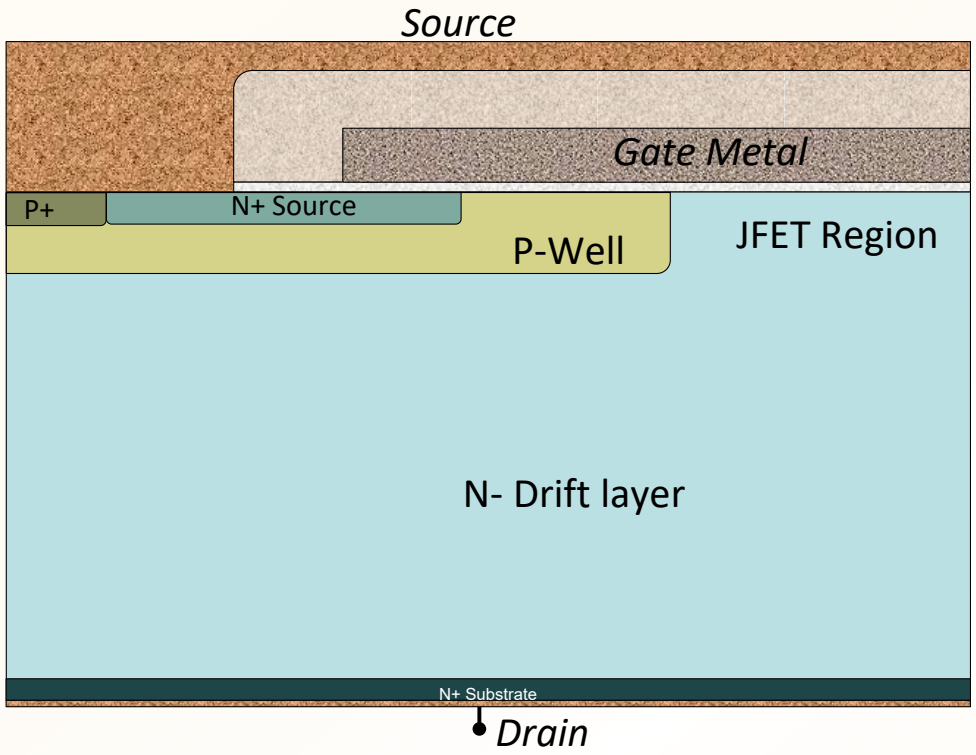
SiC MOSFETs and Rectifiers



Ultra High Voltage devices

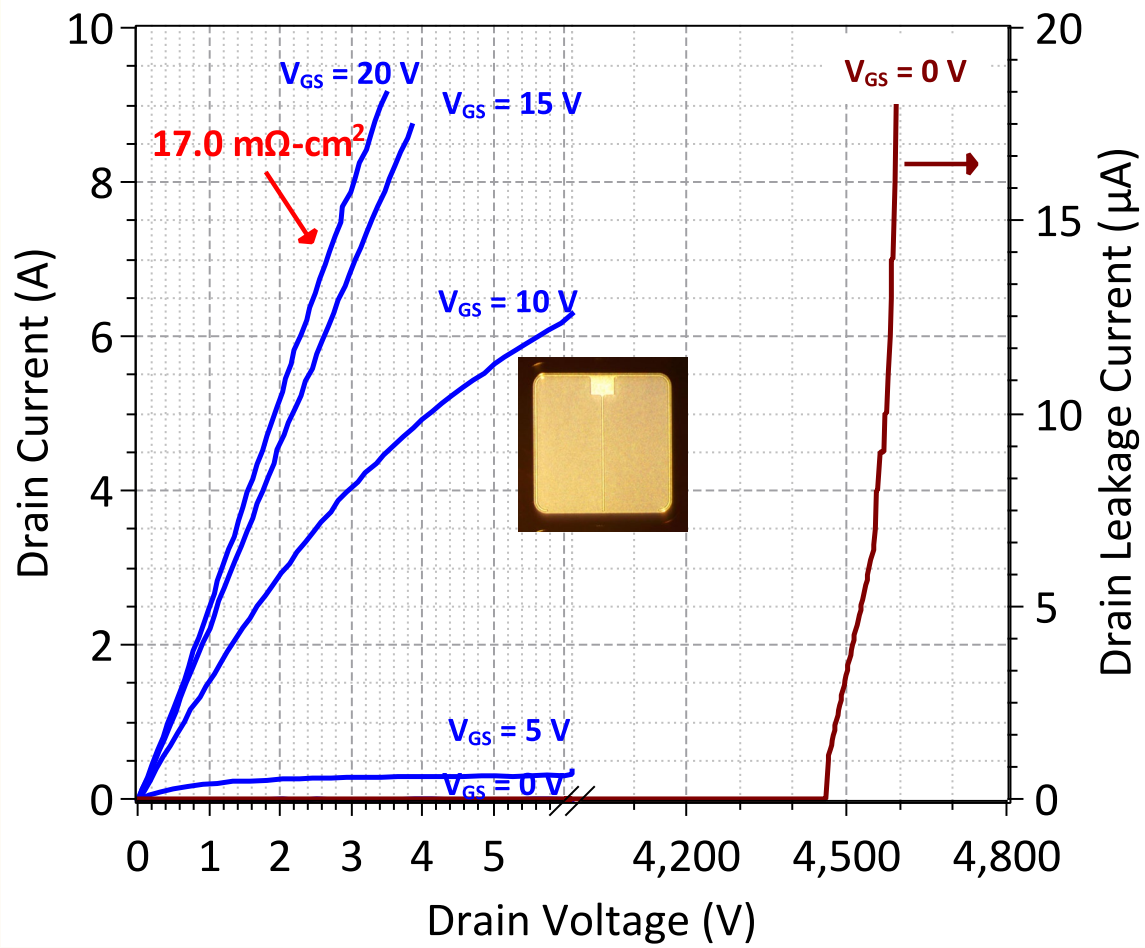
SiC MOSFETs, Thyristors and Rectifiers

Device Design and Fabrication



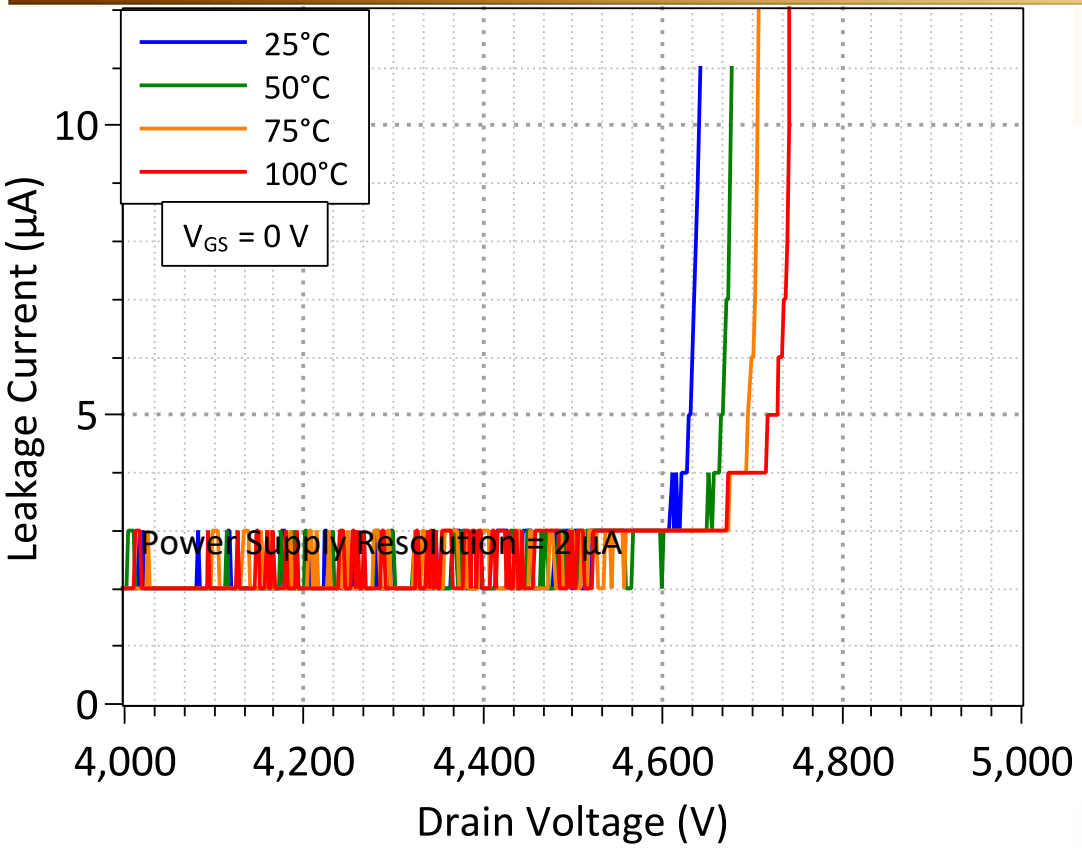
- SiC Planar DMOSFETs fabricated on 35 µm thick, ≈2.8x10^{15} cm^{-3} doped N- drift epilayers
- The device design space constituted different JFET Doping Profiles, Channel Lengths and JFET spacings

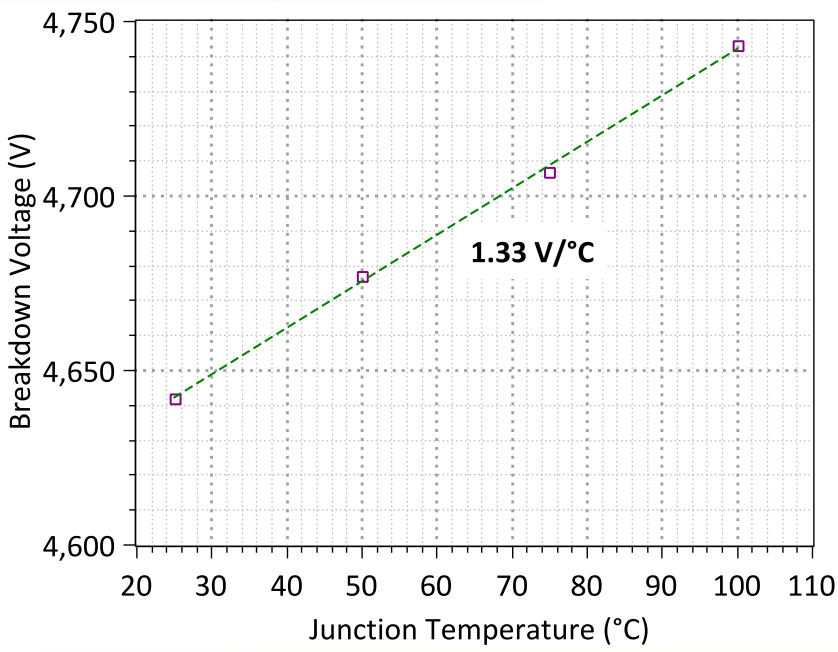
Output and Blocking Characteristics



- 2.74 mm x 2.74 mm die
  - Active Area = 0.046 cm^2
- $R_{on,sp}$ of 17.0 mΩ-cm^2, and breakdown voltage of 4600 V measured at 25°C
- BV close to theoretical limit for 35 µm/3x10^{15} cm^{-3} thick N- drift layer
- V_{TH} extracted as 2.4 V (at I_D = 5 mA)

Breakdown Voltage Variation with Temperature



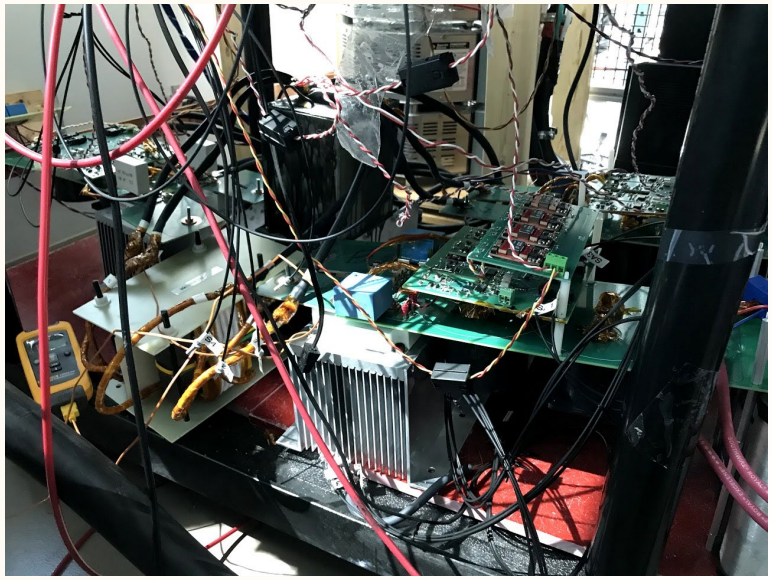


- Breakdown voltage increases linearly with measurement temperature
- Extracted temperature co-efficient of avalanche breakdown as 1.33 V/°C

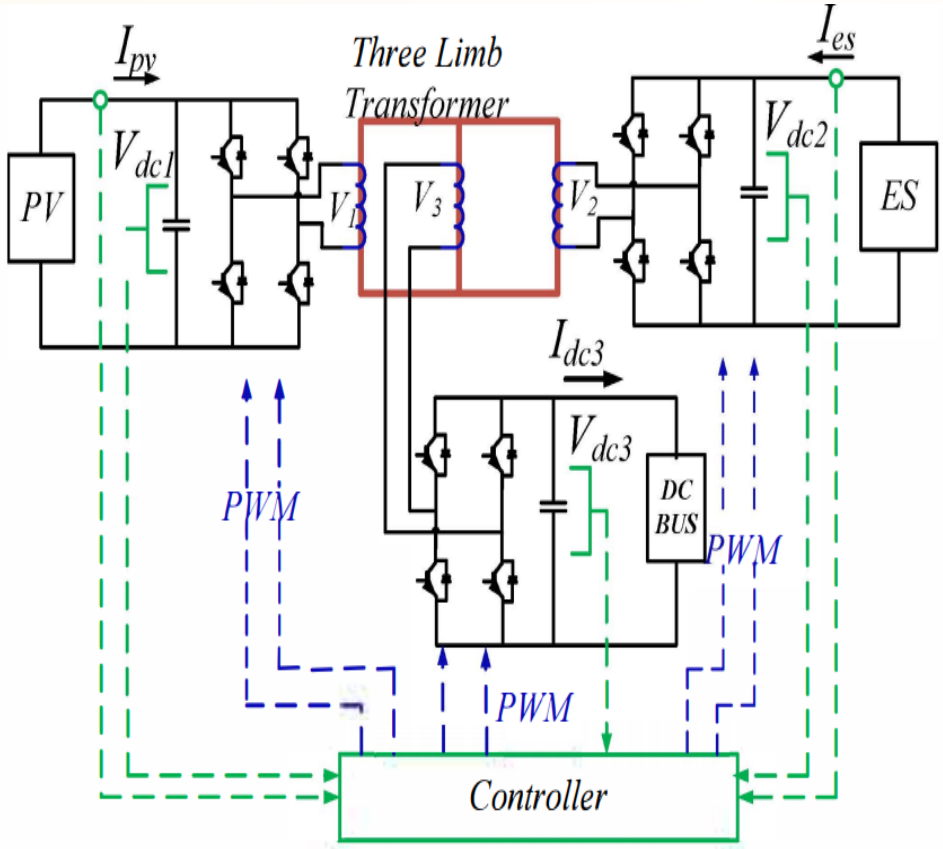
50kW Test Bench

Triple Active Bridge:

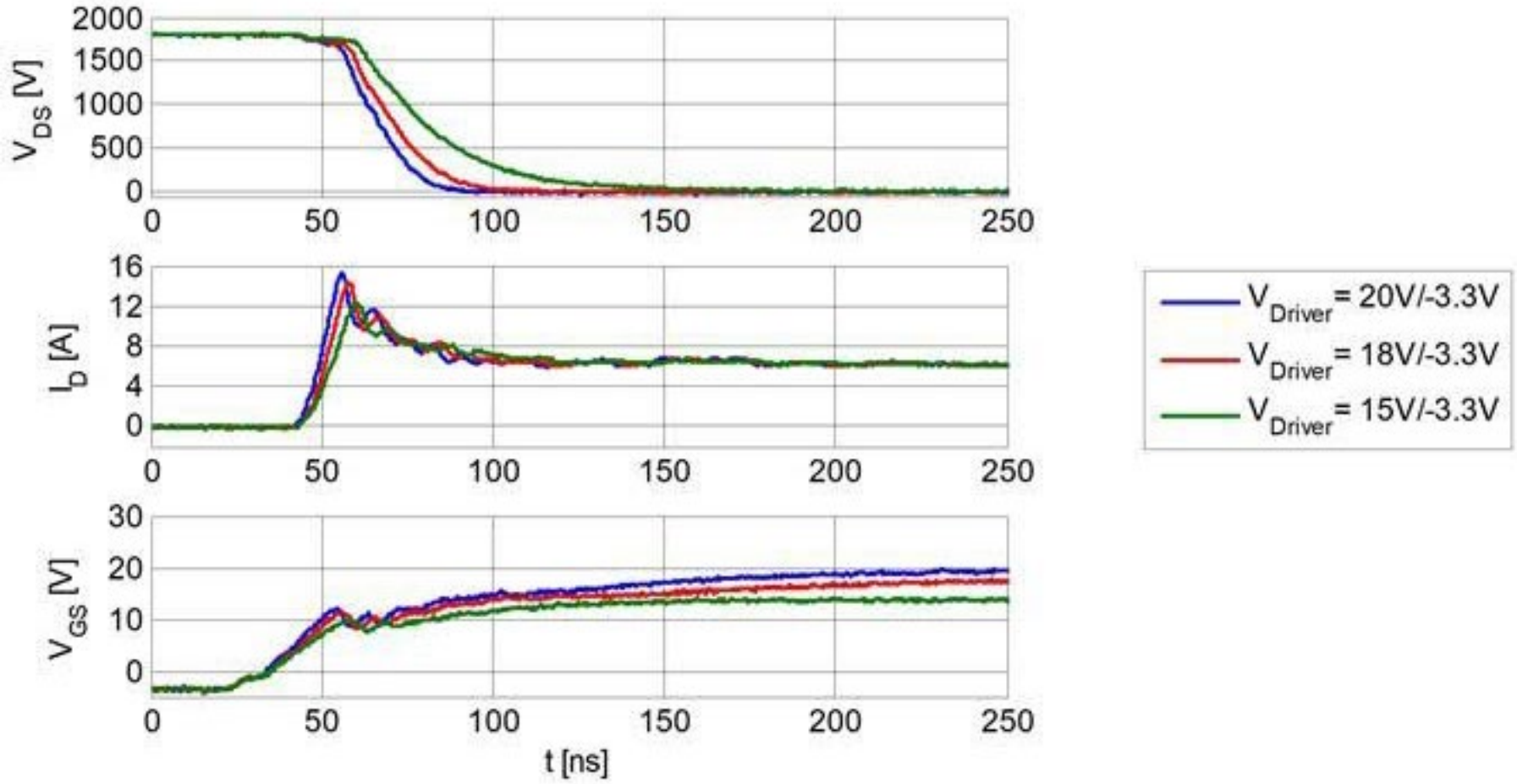
► **Integration of photovoltaic and energy storage**



Triple Active Bridge Setup at FREEDM System Center (50 kW)

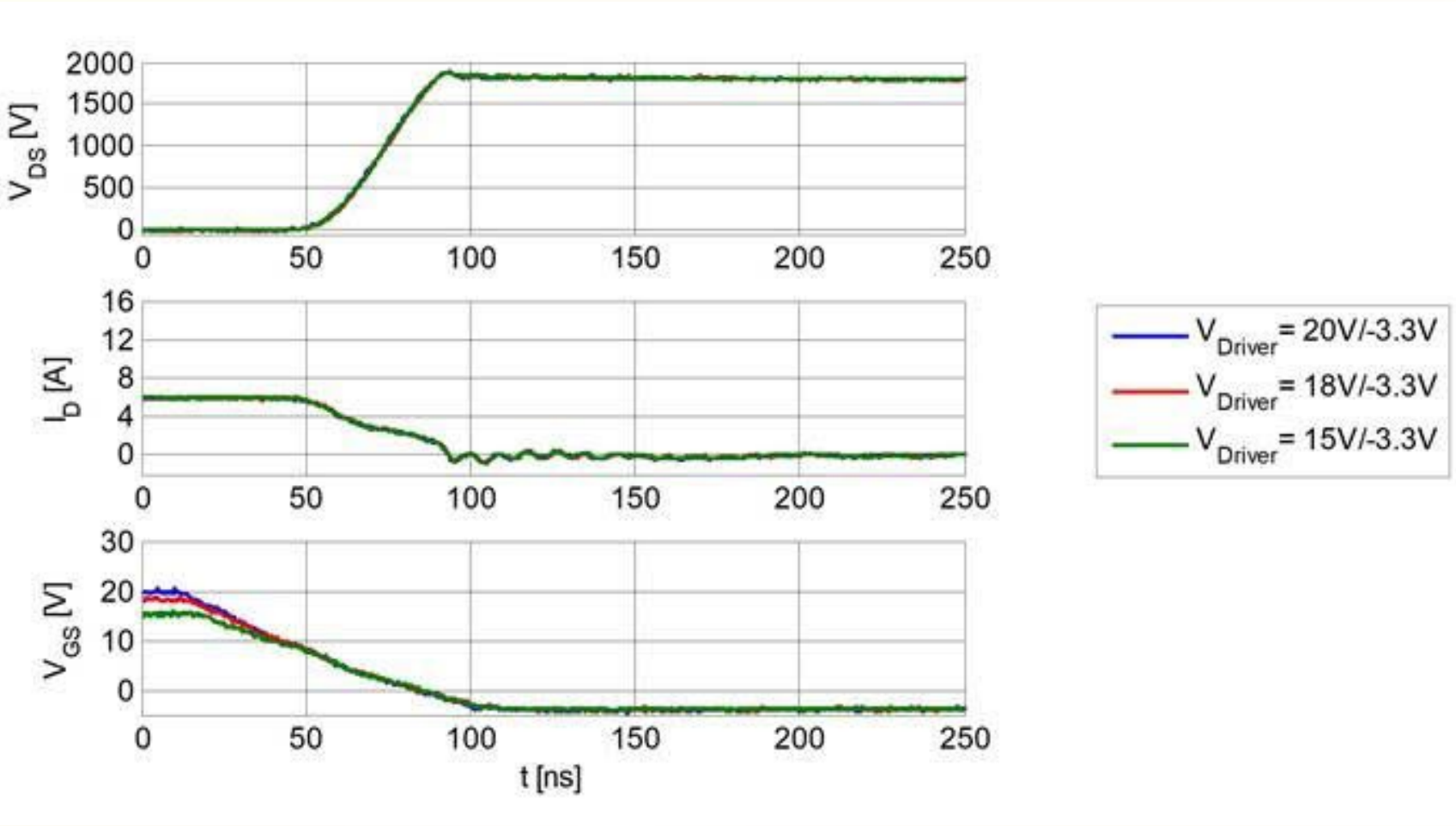


Double Pulse Switching Characterization



- V_{DS} fall time = 30 ns achieved for switching at 1800 V and 6 A, with +20 V drive voltage and $R_{G,ext}$ = 10 Ω

Double Pulse Switching Characterization



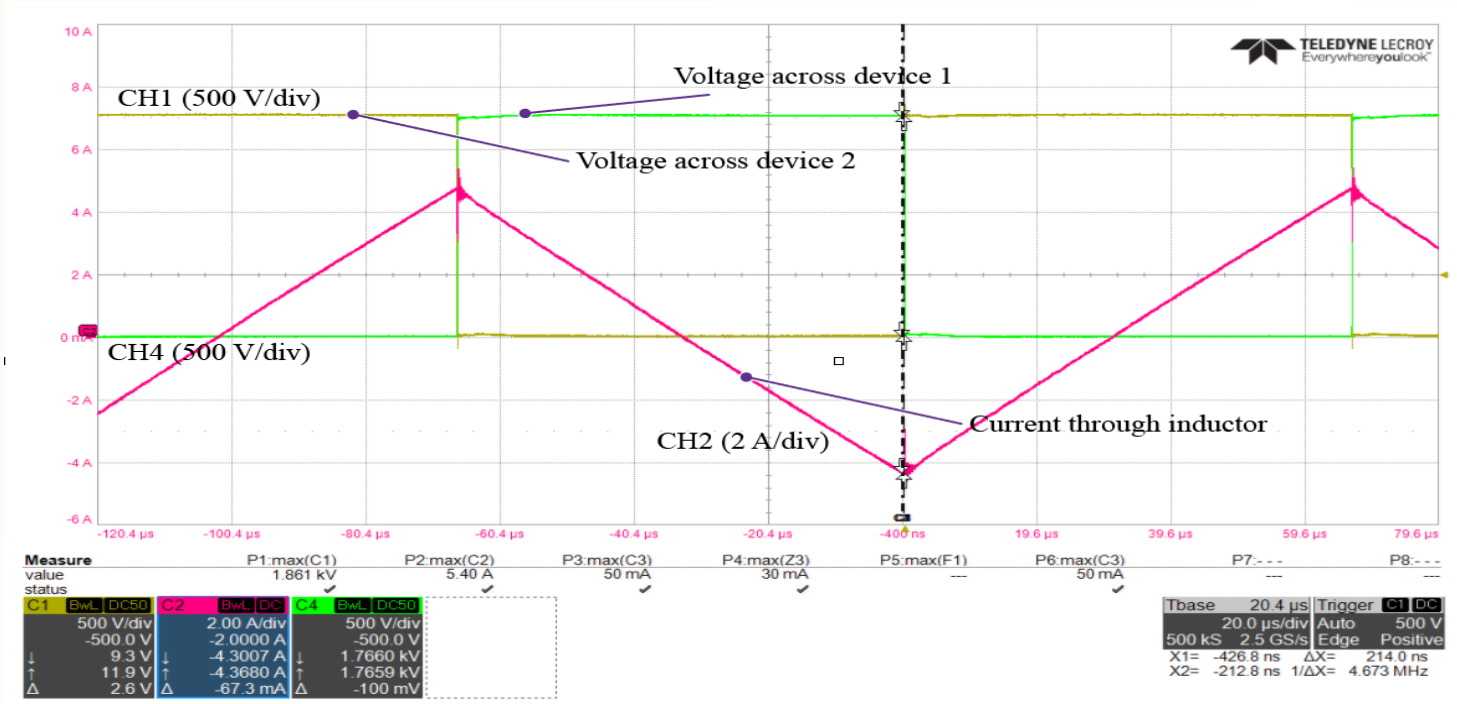
- V_{DS} rise time = 30 ns achieved for switching at 1800 V and 6 A, with -3.3 V Gate Drive Voltage

Half Bridge Operation of 3300 V Devices

Half bridge Operation:

► Inductor is connected and the device are switched at different values of current to test the operation of the devices

► Switching Frequency from 5 kHz to 10 kHz is applied



Status and Future Efforts

- Current Status
  - Technology developed for commercially viable 3300 V SiC MOSFETs
  - Up to 4600 V SiC MOSFETs demonstrated
  - Phase I Project July 2015 – March 2016
  - Phase II Project started Aug 1, 2016
- Future Efforts in Phase I
  - Scale up the voltage ratings to 6500 V
  - Scale up Current ratings to 50 A
  - Quantify the impact of All-SiC based power electronics on grid-tied energy storage systems
  - Work with commercialization partners by making a 400 kW demonstration

Grant Details

- Principal Investigator: Dr. Ranbir Singh
- Program Manager: Dr. Ranbir Singh
- Grantee:

GeneSiC Semiconductor Inc. and North Carolina State University

43670 Trade Center Place

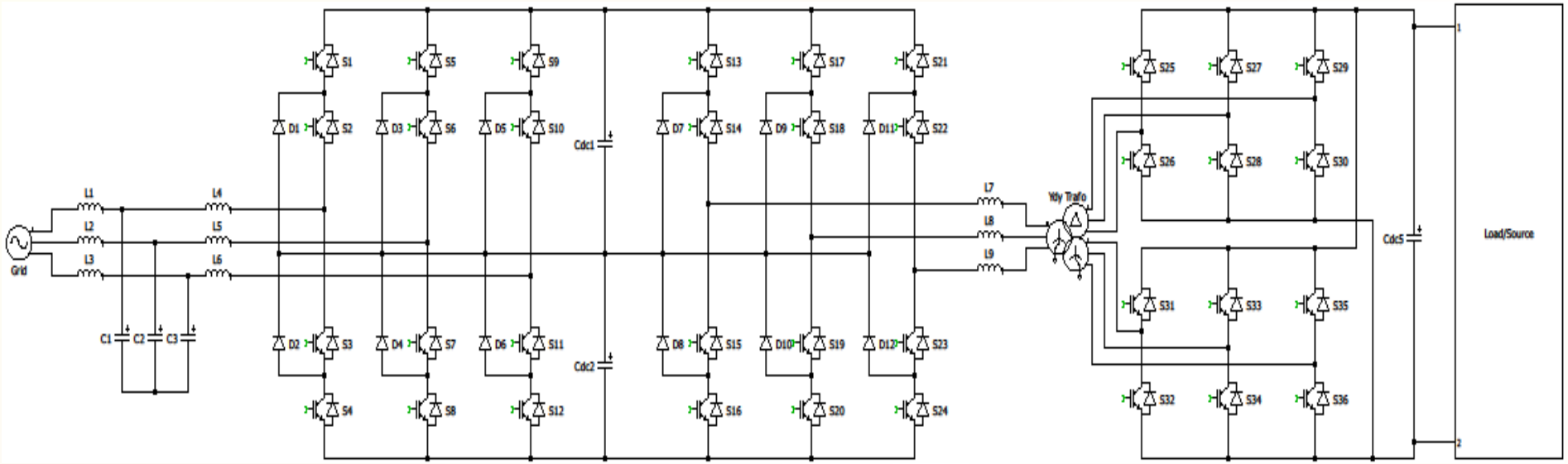
Suite 155

Dulles VA 20166

+1 703 996 8200 (ph)

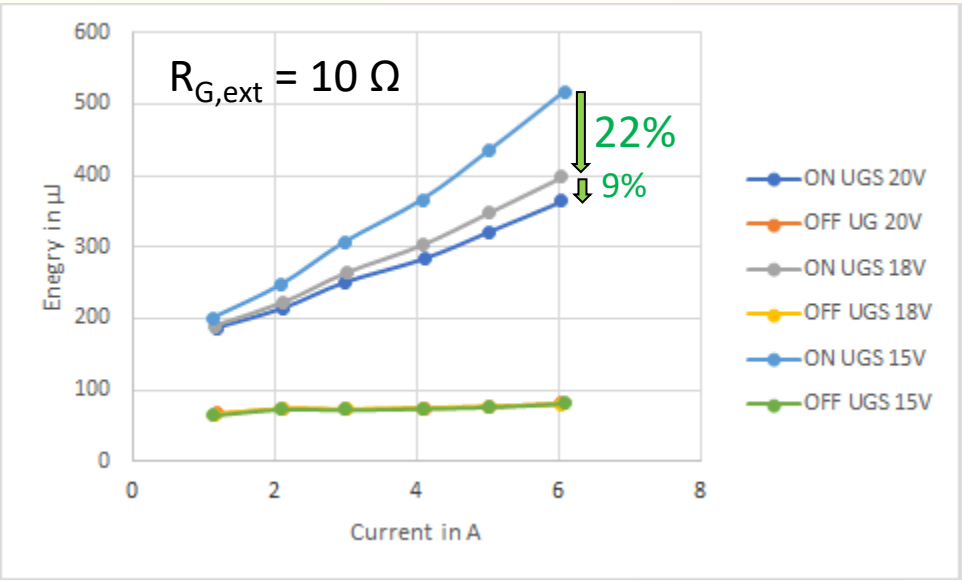
ranbir.singh@genesicsemi.com

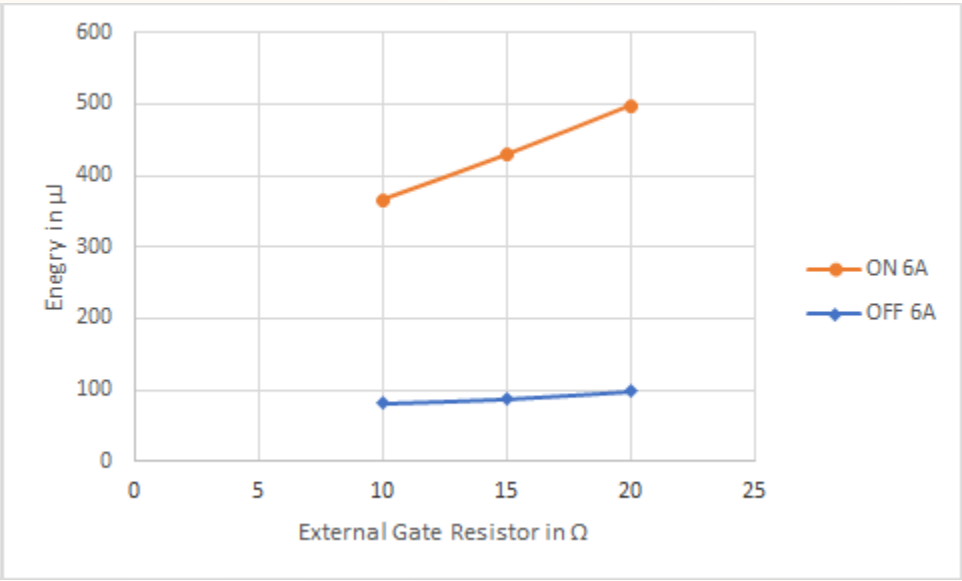
Multi-level Converters using HF/SiC Transistors at >3300 V



- Bidirectional 800 V grid-scale battery connections on secondary side
- 3300 V and 6500 V SiC devices required for high frequency secondary side connection

Double Pulse Switching Characterization





- Energy Losses are extracted from switching waveforms measured at various drain current levels and different gate drive voltages
- 22% decrease in E_{ON} observed, when gate drive voltage is increased from +15 V to +18 V
- Further increase of drive voltage from +18 V to +20 V only yielded 9% improvement in E_{ON}