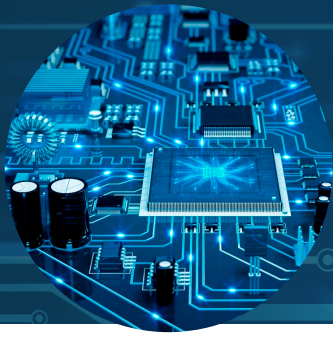




Sandia National Laboratories

# Complementary Metal-Oxide Semiconductor (CMOS) 7

## Radiation-Hardened Technology

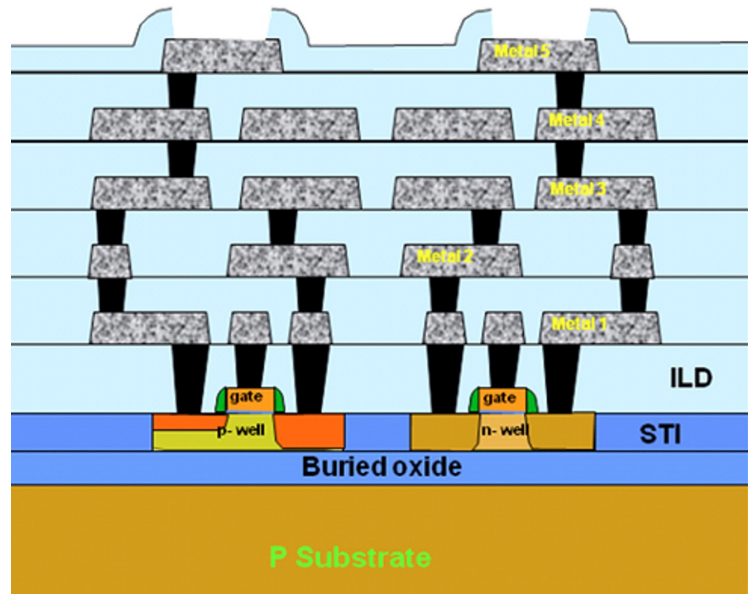


*In support of its primary mission as steward of the U.S. nuclear stockpile, Sandia has developed and delivered microelectronic products for over three decades. This expertise has also been applied to other national security needs. These include ensuring the nonproliferation of nuclear weapons and materials, reducing the threat from chemical and biological weapons, and providing advanced custom designs for other agencies involved in national defense. Sandia's Application-Specific Integrated Circuit (ASIC) development team provides custom microelectronic products and engineering services that fulfill the needs of a diverse set of customers.*

Sandia's CMOS7 technology is a strategically radiation-hardened, 3.3 volt, 350 nanometer, Silicon-on-Insulator (SOI) CMOS process for custom, high reliability digital, analog and mixed-signal ASICs. CMOS7 is a 24 mask level process with 5 metal layers.

Options for analog and mixed-signal applications include Metal-Insulator-Metal (MIM) capacitors and N+ poly resistors.

Sandia uses 350 nanometer geometry to optimize performance for analog circuits resulting in better device matching, higher supply voltages, lower leakage, and broader signal dynamic range than smaller geometry devices. Properly designed and fabricated, larger devices can be more robust in extended operating environments of temperature fluctuations, shock and radiation.



### CMOS7 Radiation Performance

- Sandia National Laboratories has developed and tested its CMOS7 technology to meet or exceed all applicable radiation limits.
- CMOS7 was specifically designed to withstand strategic radiation environments.

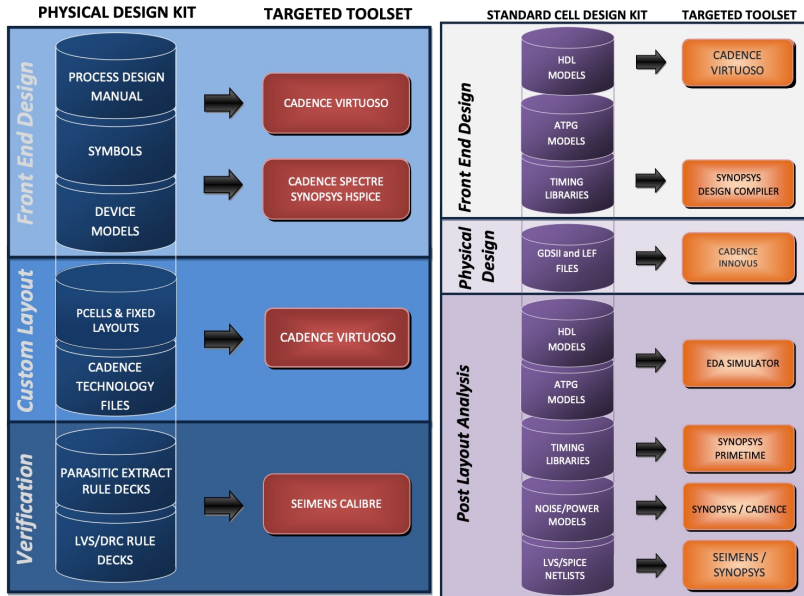
**Performance specifications available upon request for qualified inquiries.**

Sandia National Laboratories has historically focused on high-reliability custom solutions for high-consequence applications. Today Sandia is a Defense Microelectronics Activity (DMEA) Category 1A Accredited Supplier of both "trusted design and foundry services" with an efficient and disciplined process, governed by the Sandia Quality Management system that is certified to the ISO 9001:2015 standard, optimized for high-mix low-volume custom radiation-hardened, digital, analog and mixed-signal ASICs. With in-house capabilities in packaging, test, failure analysis and reliability, Sandia offers a total supply-chain solution for high-reliability custom microelectronics for expanding national security applications.



# Application Specific Integrated Circuit (ASIC) Design Services

Sandia's ASIC development team develops and maintains digital, analog, and mixed-signal design expertise along with a deep understanding of technology offerings and design methodologies to provide custom microelectronic products and engineering services that fulfill the diverse needs of our customers. Sandia's design team implements a disciplined process using the latest electronic design automation (EDA) tools to realize designs in foundry technologies ranging from 350nm to 7nm.



## CMOS7 Foundry Support

### Process Design Kit (PDK)

- Technology model files and support for custom design, layout, and validation.

### Standard Cell and I/O Libraries

- Full suite of standard cell and I/O cells with support for simulation, synthesis, and physical design.

### Analog Intellectual Property (IP) Modules

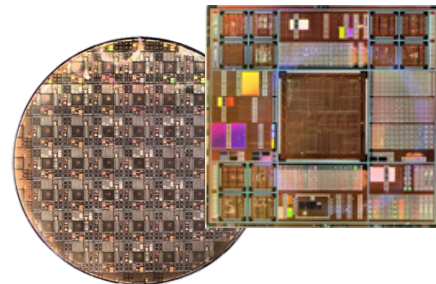
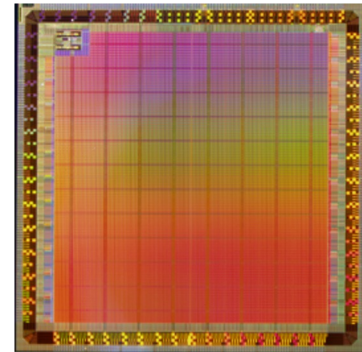
- Including A-to-D Converters, PLLs, and D-to-A Converters (contact for full listing)

### SRAM and ROM Memory Macros

- Pre-configured memory array macros (contact for full listing).

## ViArray Structured ASICs

Sandia has developed its ViArray structured ASICs to enable rapid turn-around, lower non-recurring engineering (NRE) and development costs, and reduced development risk by using pre-qualified base arrays. Structured ViArray ASICs are metal-via configurable design fabrics. Sandia's ViArray structured ASICs are partitioned for power sequencing designed to allow unused transistors to be turned off to minimize power consumption, static current, and photocurrent. The option to include in-package decoupling capacitors is also available. Currently, two product platforms have been developed: Eiger ViArray Digital Radiation-Hardened Structured ASIC and Whistler ViArray Mixed-Signal Radiation-Hardened Structured ASIC.



## Multi-Project Wafer (MPW) Program

### Sandia's MPW Program provides MPW services for CMOS7 radiation-hardened ASICs.

MPW services integrate several different integrated circuit designs on a single reticle set. Sharing mask and wafer resources reduces the overall cost per design, making it more cost effective to produce integrated circuits in low quantities.

For additional information, visit our website at:  
[www.sandia.gov/mesa](http://www.sandia.gov/mesa)