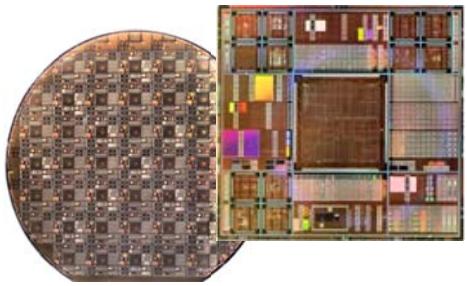
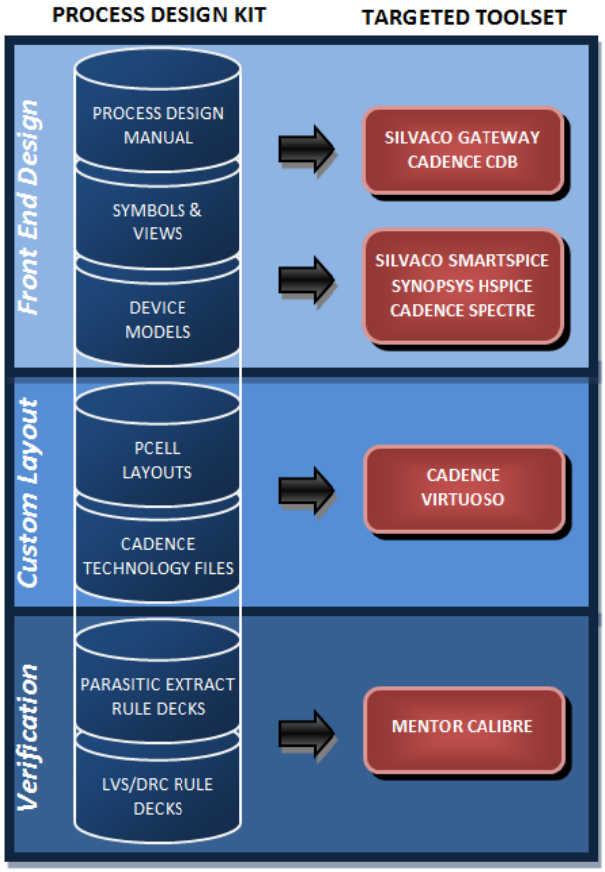
CMOS7 Process Design Kit

The CMOS7 Process Design Kit (PDK) is an organized collection of device models, physical layouts, and EDA technology files/libraries that are needed to design analog or mixed signal integrated circuits in Sandia National Laboratories 0.35um SOI CMOS7 technology.



The PDK consists of the following sub-kits:

- Physical Design Kit
  - Contains the resources needed to do custom design and verification.
- Standard Cell and I/O Design Kits
  - Holds information on the pre-assembled circuits that make up basic logic functions and I/O cells.



Physical Design Kit Highlights

- **Schematic Symbols Targeted for Silvaco Gateway**
- **CADENCE 5.1 Schematic & Symbol Views**
- **SPICE Models (HSPICE, SmartSPICE, and SPECTRE) For Transistors & Passive Devices**
- **PCELL Layouts of Transistor Devices**
- **Physical Verification Rule Files, Targeted Towards Mentor Calibre, for LVS/DRC Analysis**

DEVICE	NAME	DESCRIPTION	MODEL CORNERS SUPPORTED			
			125°C	25°C	-55°C	Process Variation
Transistors	NMOS	3.3 V device	X	X	X	X
	PMOS	3.3 V device	X	X	X	X
Resistors	RP1	Unsilicided poly resistor	X	X	X	
	RNB	Unsilicided NLDD/Nbody resistor	X	X	X	
	RPB	Unsilicided PLDD/Pbody resistor	X	X	X	
	RSEU	SEU resistor	X	X	X	
Diodes	DNB	P+ to Nbody diode	X	X	X	
	DPB	N+ to Pbody diode	X	X	X	
	DIODE_ESD	P+ to Nbody diode, poly isolated	X	X	X	
Capacitor	MIMCAP	Metal-2 to Metal-3	X	X	X	
		Metal-3 to Metal-4	X	X	X	

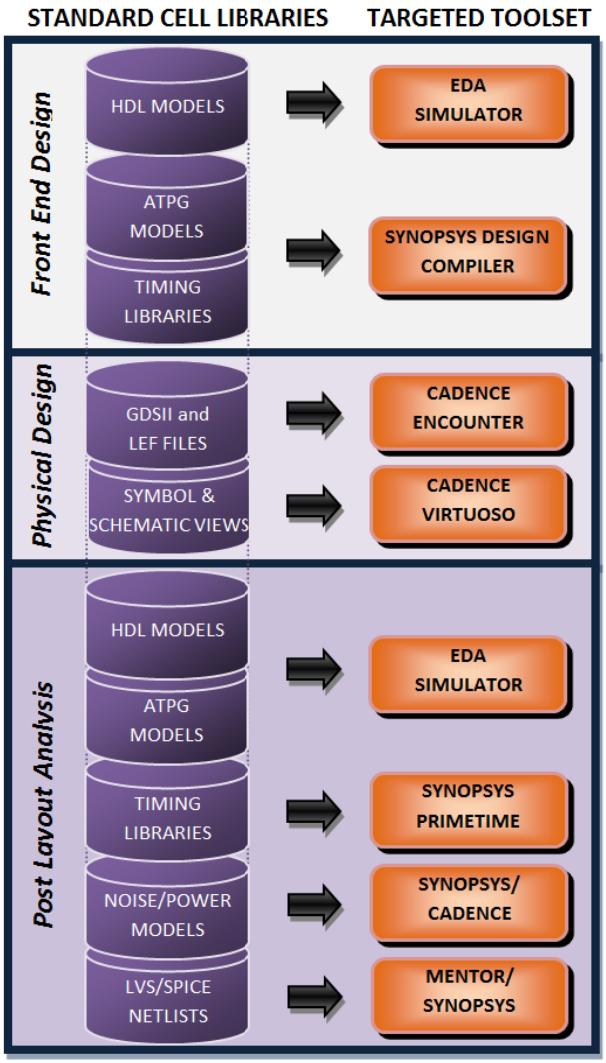
Table Devices Offered

MICROSYSTEMS SCIENCE, TECHNOLOGY & COMPONENTS

MICROSYSTEMS SCIENCE, TECHNOLOGY & COMPONENTS

Standard Cell and I/O Design Kit Highlights

- General Purpose Logic & I/O Cells With Supporting Documentation
- Flip-Flops Offered In Either 30MeV or 80MeV Radiation Tolerances
- VHDL & Verilog Simulation Models For All Standard Cells & I/O
- TETRAMAX ATPG Models
- Timing Libraries Characterized For Worst Case, Typical, & Best Case Operating Conditions Across Process Corners
  - Worst Case: 125°C, 3.0V
  - Typical: 25°C, 3.3V
  - Best Case: -55°C, 3.6V
- Physical Auto Place & Route (APR) Files (LEF, GDSII)
- Cadence 5.1 Schematic & Symbol Views
- SPICE & LVS Netlists
- Celtic Noise Models
- Cadence VoltageStorm Power Models

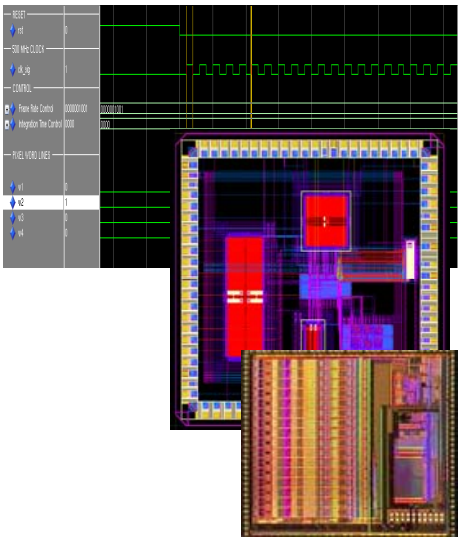


CELL TYPES	VARIATIONS OFFERED	DRIVES OFFERED
Adder	1	1
And	4	3
And/Or	15	3
Buffers	1	9
3-State Buffer	5	6
Register	10	3
Scan Register	5	1
Latch	1	2
Inverter	1	7
Multiplexer	4	4
Nand	4	6
Nor	4	6
Or/And	11	2
Or	4	4
Transmission Gate	1	4
Xnor	1	4
Xor	1	4

Standard Cells Offered

I/O TYPES	VARIATIONS OFFERED	DRIVES OFFERED	SLEW RATES OFFERED
Analog	4	--	--
Bi-Directional	128	4,8,12,16 mA	fast, slow
Input	18	--	--
Output	84	4,8,12,16 mA	fast, slow

I/O Cells Offered



www.sandia.gov/mstc

For more information email snlasic@sandia.gov

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