Proc. 1995 IEDM, pp. 609-612

Embedded Micromechanical Devices for the Monolithic Integration of MEMS with CMOS

J. H. Smith, S. Montague, J. J. Sniegowski, J. R. Murray, and P. J. McWhorter

Sandia National Laboratories
Integrated Micromechanics, Microsensors, and CMOS Technology Department
MS-1080, P.O. Box 5800
Albuquerque, NM 87185-1080 USA

Abstract

A flexible, modular manufacturing process for integrating micromechanical and microelectronic devices has been developed. This process embeds the micromechanical devices in an anisotropically etched trench below the surface of the wafer. Prior to microelectronic device fabrication, this trench is refilled with oxide, chemical-mechanically polished, and sealed with a nitride cap in order to embed the micromechanical devices below the surface of the planarized wafer. The feasibility of this technique in a manufacturing environment has been demonstrated by combining a variety of embedded micromechanical structures with a 2 μm CMOS process on 6 inch wafers. A yield of 78% has been achieved on the first devices manufactured using this technique.

Introduction

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MicroElectroMechanical Structures (MEMS) with driving, controlling, and signal processing electronics. This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process. For example, Analog Devices has developed and marketed an accelerometer [1] which illustrates the viability and commercial potential of this integration. They accomplished this task by interleaving, combining, and customizing their manufacturing processes which produce the micromechanical devices with the processes that produce the electronics. In another approach, researchers at Berkeley [2] have developed a modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent micromechanical processing.

In order to maintain the modularity of the Berkeley approach but overcome some of the manufacturing challenges of their CMOS-first approach, we have developed a MEMS-first process. This process places the micromechanical devices in a shallow trench, planarizes the wafer, and seals the micromechanical devices in the trench. These wafers with the completed, planarized micromechanical devices are then used as starting material for a conventional CMOS process. This technique is equally applicable to other microelectronic device technologies such as bipolar or BiCMOS. At Sandia's Microelectronics Development Laboratory, both 2 μm and 0.5 μm CMOS technologies on 6 inch wafers are available; the 2 μm process is being used as the development vehicle for the integrated technology. Since this integration approach does not modify the CMOS processing flow, the wafers with the subsurface micromechanical devices can also be sent to a foundry for microelectronic processing. Furthermore, the topology of multiple polysilicon layers does not complicate subsequent photolithography. A high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal budget of the microelectronic processing does not affect the mechanical properties of the polysilicon structures. This anneal can affect the doping profile of commonly used epitaxial starting material; however, this effect can be easily addressed by increasing the epitaxial layer thickness of the starting material.

Process Description

Figure 1 is a schematic cross-section of the integrated technology. First, alignment marks are etched onto the surface of wafer in order to provide reference locations for subsequent processing. A shallow trench (~ 6 μm for the single-level polysilicon structures described here) is etched in (100) silicon wafers using a KOH etchant. The KOH etchant preferentially etches the (100) crystal plane and produces a trench with sidewalls having

a (111) orientation and a slope of 54.7^o relative to the surface. This slope aids in the subsequent photo patterning of the MEMS within the wells.

The alignment marks from the top surface of the wafer are used as references to generate another set of alignment marks on the bottom surface of the trench. This approach is used to optimize level-to-level registration and resolution of features within the trench. Feature sizes with critical dimensions as small as 1 μm were successfully defined within the trench.

A silicon nitride film is deposited to form a dielectric layer on the bottom of the trench. Sacrificial oxide and multiple layers of polysilicon are then deposited and patterned in a standard surface micromachining process. Polysilicon studs provide contact between the micromechanical devices and the CMOS; the depth of the trench is sized so that the top of the polysilicon stud lies just below the top of the planarized trench. The shallow trenches are then filled with a series of oxide depositions optimized to eliminate void formation in high-aspect-ratio structures. The wafer is subsequently planarized with chemical-mechanical polishing (CMP). The entire structure is annealed to relieve stress in the structural polysilicon and sealed with a silicon nitride cap. At this point, conventional CMOS processing is performed. The backend of the process requires additional masks to open the nitride cap over the micromechanical layer prior to release of the micromechanical structures.

Photoresist is used as a protection layer over the exposed bond pads during the release process. The slow etching of the undoped, densified glasses used as sacrificial layers and the ability of this photoresist to withstand long, HF-based etches is presently a factor that imposes limits on the design rules used for spacing of release access holes in the structure. Development of photopatterning processes with greater resistance to release etches as well as sacrificial layers with greater etch rates is ongoing.

Results

Figure 2 shows a cross-sectional view of an anchor point for the MEMS device within a trench after planarization. The silicon nitride dielectric layer, the ground plane polysilicon, the micromechanical polysilicon and the sacrificial/planarizing layers are easily seen in this Scanning Electron Micrograph (SEM). Figure 3 is a close-up view of the polysilicon interconnects on the bottom of the trench leading to the polysilicon stud that connects to the CMOS metal. This SEM was taken from a wafer removed from the development lot prior to CMOS fabrication. The micromechanical devices were then released and tested to verify the functionality of the micromechanical designs.

Figure 4 shows a portion of a die from the first completed lot. The figure contains surface-micromachined polysilicon resonators in a trench alongside CMOS sensing electronics. Additional devices including CMOS diagnostic structures, MEMS diagnostic structures, combustible gas detectors and accelerometers were also fabricated on this wafer. The layout of the completed die is shown in Figure 5. The completed MEMS structures showed no mechanical degradation with respect to MEMS structures which had not seen the CMOS process. This first wafer was tested at the wafer scale for parametric and functional data. The CMOS parametrics agreed within acceptable process control limits with our unmodified 2 μm CMOS process. Due to tester limitations, only the combustible gas sensors were tested at the wafer level in a fully-coupled CMOS/MEMS mode. These devices showed a yield of 78% as shown in the wafer map of Figure 6. The combustible gas sensor control circuitry included an op-amp and a set of power MOSFETs. The functional yield data on the control circuitry for the accelerometers and resonators was similar although the tests only exercised the CMOS.

This integration process is not limited to the single-level polysilicon process described here. This process can be used with more intricate micromechanical processes such as the three-level polysilicon technology previously developed at Sandia [3]. An example of this technology built in a trench is shown in Figure 7.

Conclusions

The manufacturability of a technology that integrates surface-micromachined polysilicon structures with microelectronics in a modular fashion has been demonstrated. This technology does not impose additional limits on the size, thickness, or number of layers of the micromechanical polysilicon structures. The modularity of the process allows changes to be made to either the micromechanical process or the microelectronic process without affecting the other process. A planarized wafer with the embedded MEMS can serve as starting material for a conventional microelectronics foundry service since the technology does not require significant modifications of standard microelectronic fabrication processes.

References

[1] W. Kuehnel and S. Sherman, “A surface micromachined silicon accelerometer with on-chip detection circuitry,” *Sensors and Actuators A*, vol. 45, no. 1, pp. 7-16 (1994).

[2] W. Yun, R. Howe, and P. Gray, “Surface micromachined, digitally force-balanced accelerometer with integrated CMOS detection circuitry,” *Proc. of the IEEE Solid-State Sensor and Actuator Workshop `92*, p. 126 (1992).

[3] J. Sniegowski and E. Garcia, “Microfabricated actuators and their application to optics," *SPIE* vol. 2383, pp. 46-64 (1995).

Acknowledgments

The process development engineers, operators, and technicians of the Microelectronics Development Laboratory should also be acknowledged for their contributions to the process development, fabrication, and testing of these devices. The authors are particularly indebted to Dale Hetherington for CMP development, Chris Apblett for high-aspect-ratio oxide fill development, Tony Farino for photolithography development, and Bob Timon for wet process development. This work, performed at Sandia National Laboratories, was supported by the U.S. Department of Energy under contract DE-AC04-94AL85000.

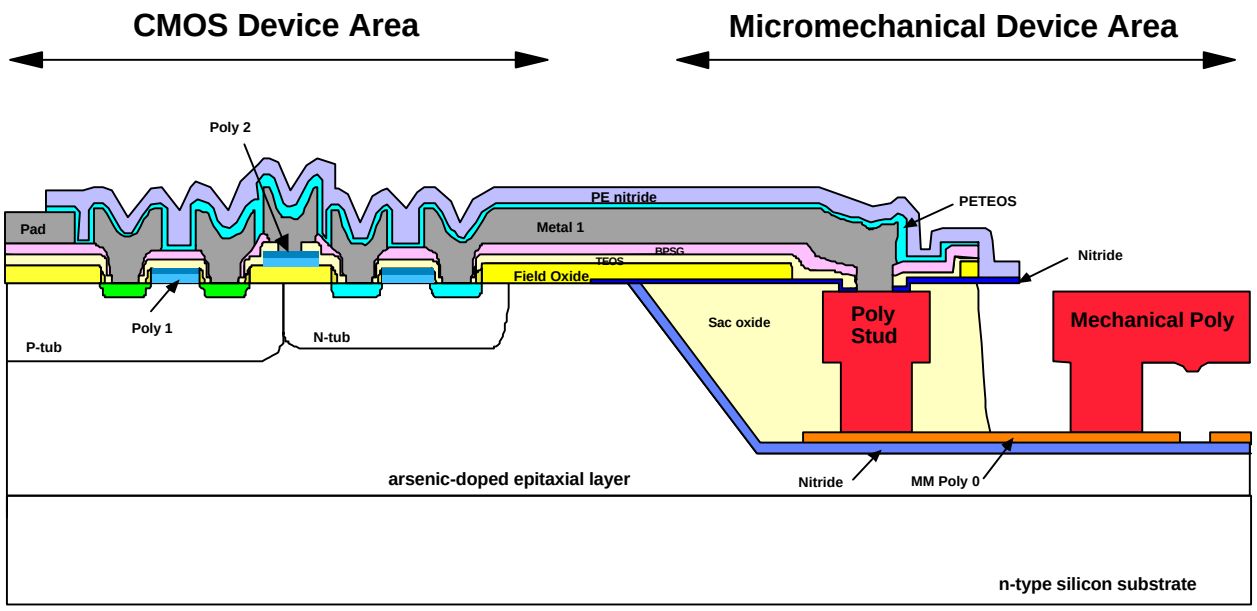

Figure 1. A cross-sectional schematic of the subsurface, embedded MEMS integrated technology.

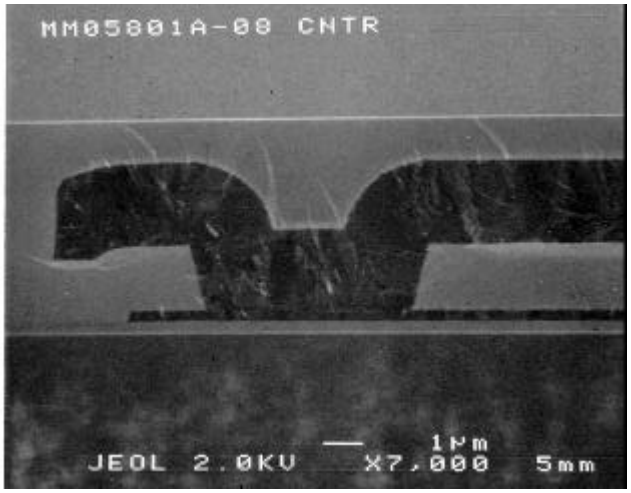

Figure 2. A cross-sectional view of a single-layer polysilicon (with ground plane) structure in a trench. The trench has been refilled with oxide and planarized using chemical-mechanical polishing. This planar structure is ready for standard CMOS processing.

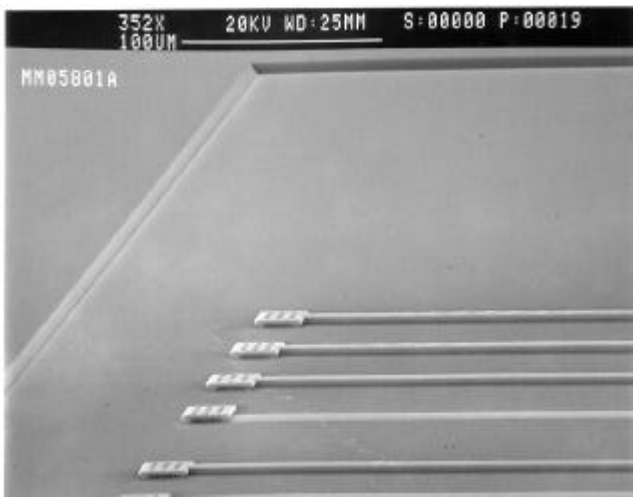

Figure 3. Interconnects leading to polysilicon studs for contact to CMOS metallization prior to fabrication of electronics.

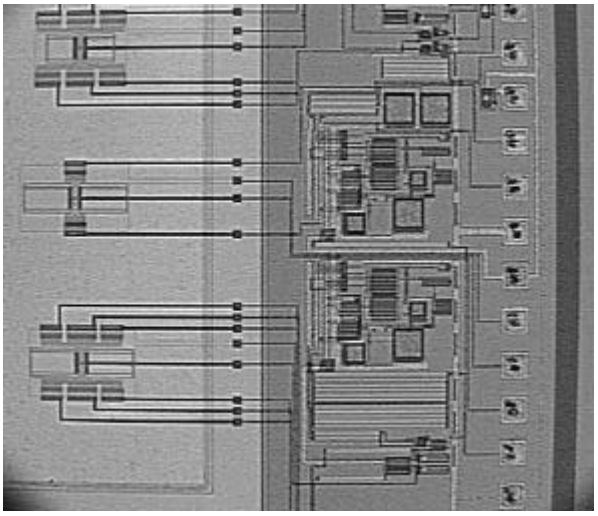

Figure 4. Surface-micromachined polysilicon resonators built in a trench alongside their CMOS sensing electronics. The marks on the bonding pads were caused during wafer-level testing.

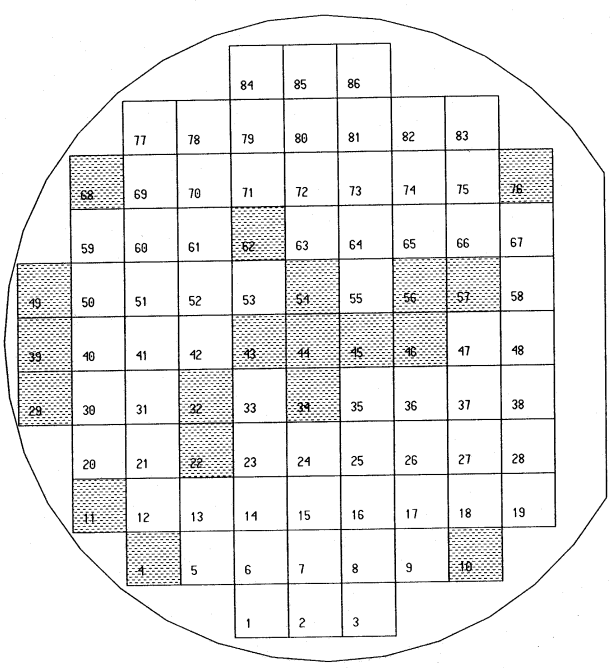

Figure 6. A wafer map showing functionality from a wafer-level test of combustible gas sensor devices. The unshaded devices are functional.

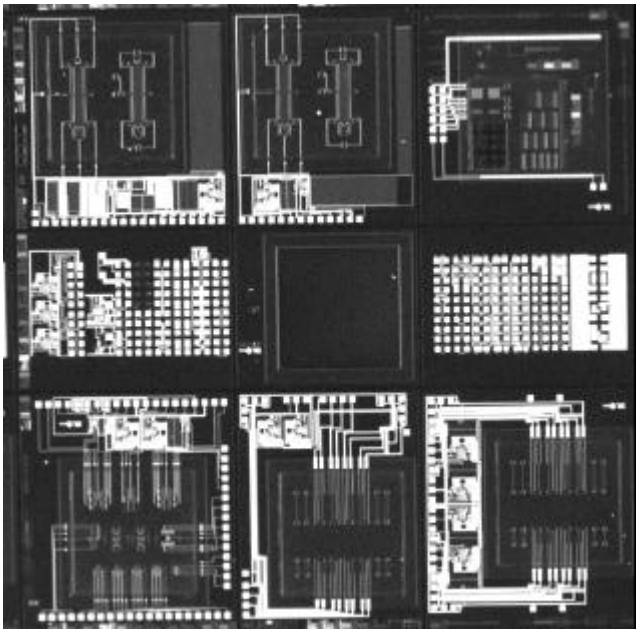

Figure 5. An photograph of the completed integrated MEMS/CMOS die illustrating the layout of the various sensors, resonators, test structures, and electronics.

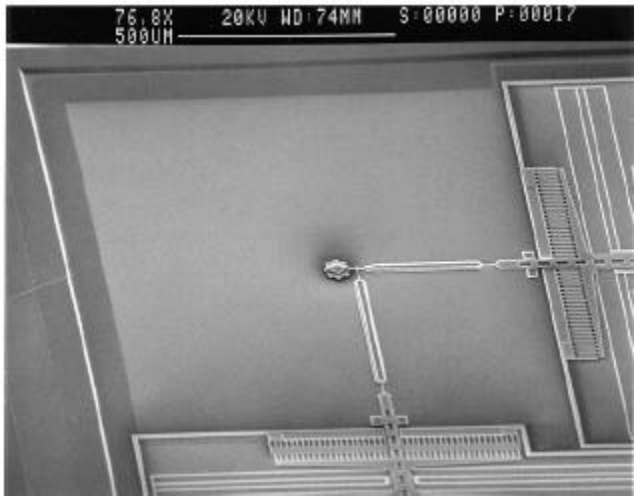

Figure 7. A three-level polysilicon structure (microengine) built in a trench. Here, the trench depth is approximately 12 μm.