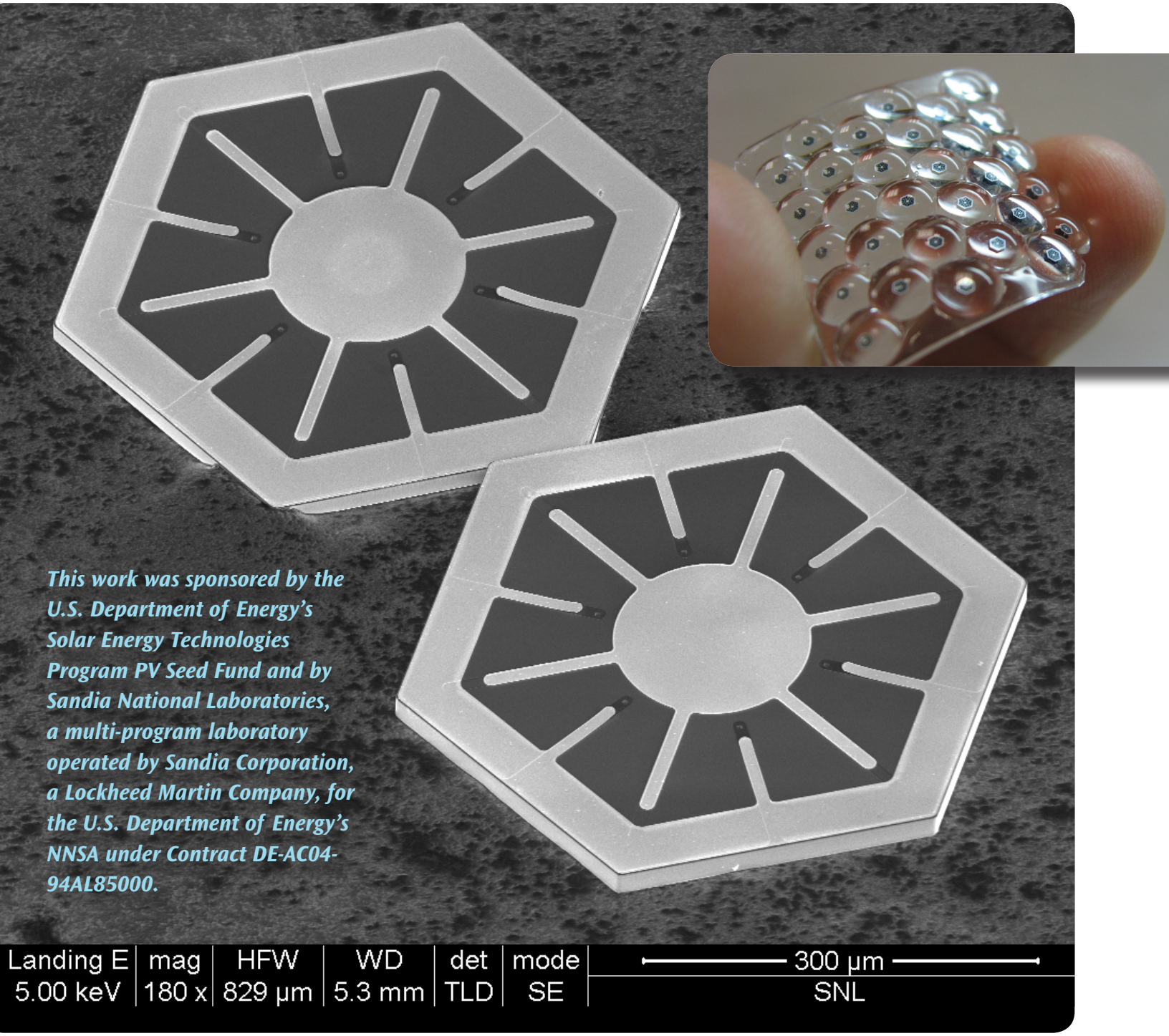
Microsystems Enabled Photovoltaics (MEPV)



This work was sponsored by the U.S. Department of Energy's Solar Energy Technologies Program PV Seed Fund and by Sandia National Laboratories, a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U.S. Department of Energy's NNSA under Contract DE-AC04-94AL85000.

Microsystems Enabled Photovoltaics (MEPV)

1. Developer Information

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B. Joint Submitter(s)

None.

For a video summary of Sandia's microsystems enabled photovoltaics, go to http://mepv.sandia.gov or click the image above to play.

2. Product Information

A. Product Name

Microsystems Enabled Photovoltaics (MEPV).

B. Product Photo

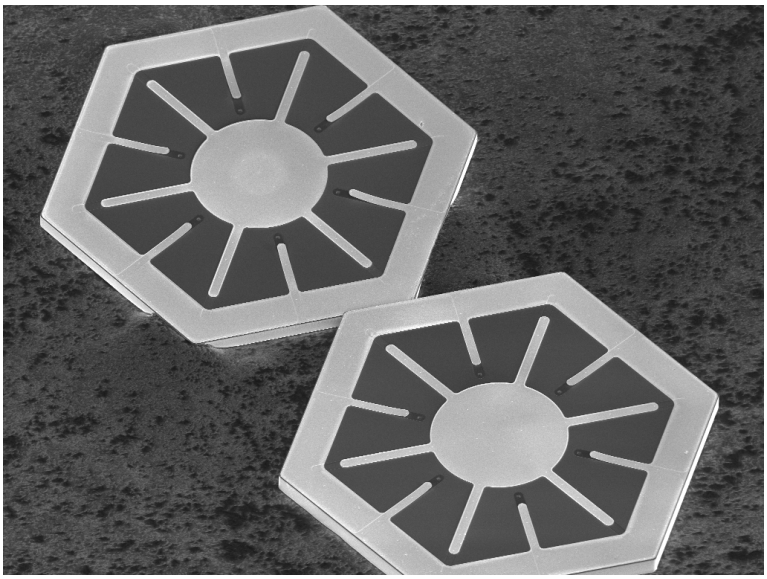

Figure 1. *Scanning electron microscope image of two microscale crystalline silicon photovoltaic cells with radial contacts on the back side. (Source: Sandia)*

3. Brief Description

Microscale photovoltaic cells that harness energy from a variety of light sources and power devices in flexible, moldable, or flat-plate formats.

4. First Marketed

Sandia's MEPV technology was made available for licensing on June 16, 2011 (see Appendix G).

5. Has this product or an earlier version been entered in the R&D100 awards competition previously?

No.

6. Principal Investigator

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7. Product Price

Our team has conducted cost modeling at the cell, module, and system level to estimate the pricing of this photovoltaic cell technology for the most likely application market sectors. Based on this work, the team anticipates product pricing — including profit margin — to be:

- Under \$10/$Watt_{peak}$ for the mobile powering of consumer electronics.
- Less than \$0.60/$Watt_{peak}$ for concentrated photovoltaic (CPV) modules on big box and warehouse rooftops for production of retail electricity.
- Less than \$0.40/$Watt_{peak}$ for CPV modules on power utility farms for production of wholesale electricity.

8. Patents Pending

US Patent Application #11/933,458, November 1, 2007, PHOTOVOLTAIC SOLAR CONCENTRATOR, Gregory N. Nielson, Vipin Gupta, Murat Okandan, Michael Watts

US Patent Application #12/882,976, September 15, 2010, PHOTOVOLTAIC SOLAR CONCENTRATOR, Gregory N. Nielson, Vipin Gupta, Murat Okandan, Michael Watts

US Patent Application #12/894,772, September 30, 2010, SOLAR PHOTOVOLTAIC REFLECTIVE TROUGH COLLECTION STRUCTURE, Gregory N. Nielson, William C. Sweatt, Benjamin Anderson, Murat Okandan

US Patent Application #12/914,441, October 28, 2010, MICROSYSTEM ENABLED PHOTOVOLTAIC MODULES AND SYSTEMS, Gregory N. Nielson, William C. Sweatt, Murat Okandan

US Patent Application #12/957,082, November 30, 2010, PHOTOVOLTAIC SOLAR CONCENTRATOR, Gregory N. Nielson, Murat Okandan, Paul Resnick, Jose Luis Cruz-Campa

US Patent Application #13/164,017, June 20, 2011, SOLAR CELL WITH BACK SIDE CONTACTS, Gregory N. Nielson, Murat Okandan, Paul Resnick, Peggy Clews, Jose Luis Cruz-Campa, Mark Wanlass

US Patent Application #13/164,483, June 20, 2011, PHOTOVOLTAIC SYSTEM, Anthony Lentine, Gregory N. Nielson, William C. Sweatt, Murat Okandan, Sean Hearne, Paul Clem, Paul Davids, Dale Huber, Jeffrey Nelson, Christopher Apblett

US Patent Application #13/239,181, September 21, 2011, STRUCTURED WAFER FOR DEVICE PROCESSING, Murat Okandan, Gregory N. Nielson

US Patent Application #13/240,127, September 22, 2011, MOLDABLE PHOTOVOLTAIC SOLAR CELL MODULE, Gregory N. Nielson, Murat Okandan, Jose Luis Cruz-Campa, Vipin Gupta, Paul Resnick, Carlos A. Sanchez, Peggy Clews

US Patent Application #13/240,520, September 22, 2011, PHOTOVOLTAIC SOLAR CONCENTRATOR, Gregory N. Nielson, Murat Okandan, Jose Luis Cruz-Campa, Vipin Gupta, Paul Resnick, Carlos A. Sanchez, Peggy Clews

"In my role as Director of the Arizona Research Institute for Solar Energy, I have seen many photovoltaic and concentrator photovoltaic technologies and many designs for new technologies. Sandia's microscale photovoltaics is one with a highly innovative approach and a significant chance for a paradigm-shifting success."

— Joe Simmons,
Director of the Arizona Research Institute for Solar Energy, Professor of Materials Science and Engineering, and Professor of Optical Sciences, University of Arizona

US Patent Application #13/240,354, September 22, 2011, MICROSCALE AUTONOMOUS SENSOR AND COMMUNICATIONS MODULE, Murat Okandan, Greg N. Nielson

US Patent Application #61/594776, February 3, 2012, PARALLEL INTERLEAVED INVERTERS, Anthony Lentine, Brian Johnson

9. Primary Function

With dimensions as small as 100-µm wide and 1-µm thick, these miniaturized photovoltaic cells convert photons from the sun or any other light source into electricity.

Sandia's MEPV team has developed microscale photovoltaic (PV) cells using microsystems tools and manufacturing techniques familiar to the semiconductor industry. With dimensions as small as 100-µm wide and 1-µm thick, these miniaturized PV cells convert photons from the sun or any other light source into electricity. As with microelectronic components, the small size of the PV cells enables the packaging and integration of the energy system into a variety of formats that conform to the shapes and contours of the powered device and blend into the device's look, feel, and functionality.

To date, we have developed three microscale PV cell designs:

1. **A silicon back-contacted interdigitated finger pattern.** This cell design is particularly well-suited for sunlight-to-electricity conversion without optical concentration. The back contact design eases the on-wafer placement of solder bump bonds that can be assembled onto flat surfaces with semiconductor pick-and-place tools (e.g., CPV modules or flexible PV sheets).
2. **A silicon back-contacted radial pattern.** Also well-suited for converting sunlight to electricity without optical concentration, the symmetry of the radial back-contacted pattern enables the use of self-assembly approaches without the need for rotational orientation of the cell.
3. **An ultrathin single-junction gallium arsenide (GaAs) cell with back contacts.** This cell design is particularly useful for concentrated photovoltaic designs or for the conversion of diffuse, ambient light to electricity for high value applications (e.g., mobile power, space power). At thicknesses of 1–3 µm, these microscale PV cells can generate more watts per gram and watts per unit area than their crystalline silicon (c-Si) counterparts.

All of the enumerated microscale PV cell designs can be embedded into highly flexible PV modules, incorporated into low-cost microconcentrator modules, or built into consumer electronic products. And because there are no electrical contacts on the front side, these microscale PV cells can be integrated in aesthetically pleasing patterns that may not even reveal the cells' electricity generation capability.

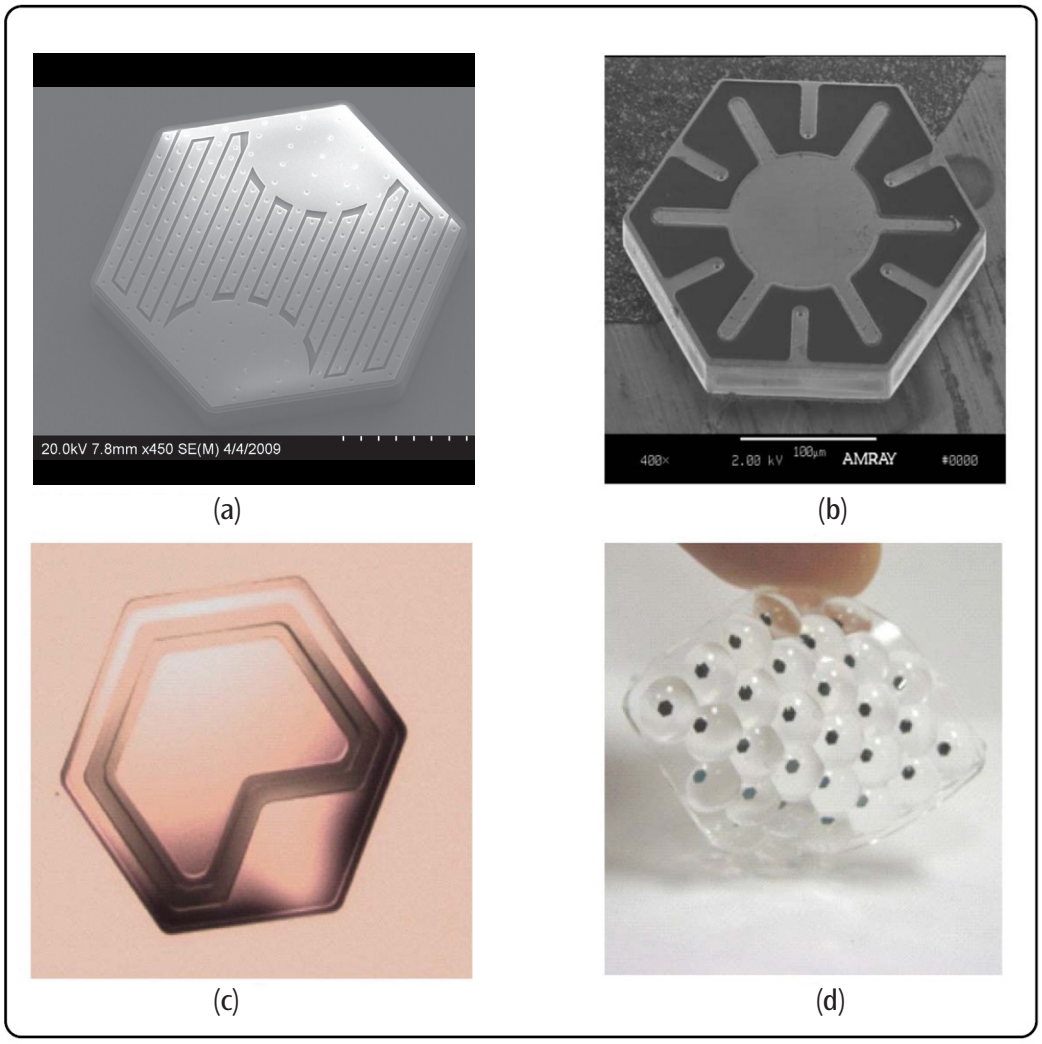


Figure 2. *Pictures of our microscale PV cells: a) Scanning electron microscope (SEM) perspective view of a 250-µm c-Si PV cell released through an anisotropic potassium hydroxide (KOH) under-etch with lateral interdigitated fingers; b) SEM image of a 250-µm wide c-Si PV cell with radial contacts released using a buried silicon dioxide layer; c) Magnified image of a 250-µm GaAs PV cell released using a buried aluminum arsenide layer; d) flexible mechanical model with embedded microscale photovoltaic cells. (Source: Sandia)*

Figure 2 shows optical and scanning electron microscope (SEM) images of these three microscale PV cell designs. This figure also shows c-Si PV cells embedded in silicone.

With these three microscale PV cell designs, the Sandia MEPV team has developed a new class of microsystem-based multijunction PV cells that do not have the operational handicaps of lattice and current matching found in traditional multijunction III-V PV cells. Using three-dimensional (3D) integration processes for stacking with independent electrical connections, our team has developed dual-junction, microscale PV cells with leveled back contacts (see Figure 3) as well as triple-junction, microscale PV cells combining c-Si, GaAs, and indium gallium phosphide (InGaP) junctions.

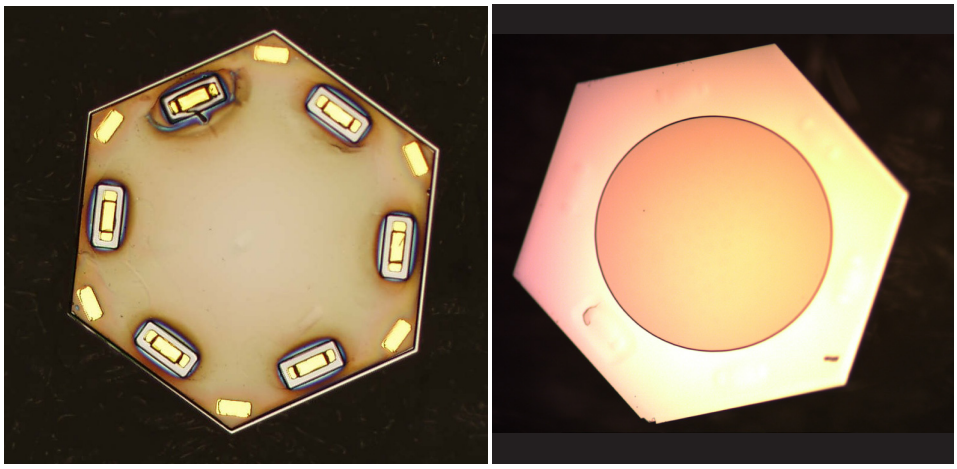


Figure 3. *Left: Magnified image of a 750-µm wide, 6-µm thick GaAs/InGaP PV cell with leveled back contacts. Right: Front side of a microscale GaAs/InGaP PV cell. (Source: Sandia)*

The stacked cell designs are particularly well suited for power applications that require high-watt production per unit area or weight (e.g., manned or unmanned aircraft, satellites, and CPV).

10. How does it operate?

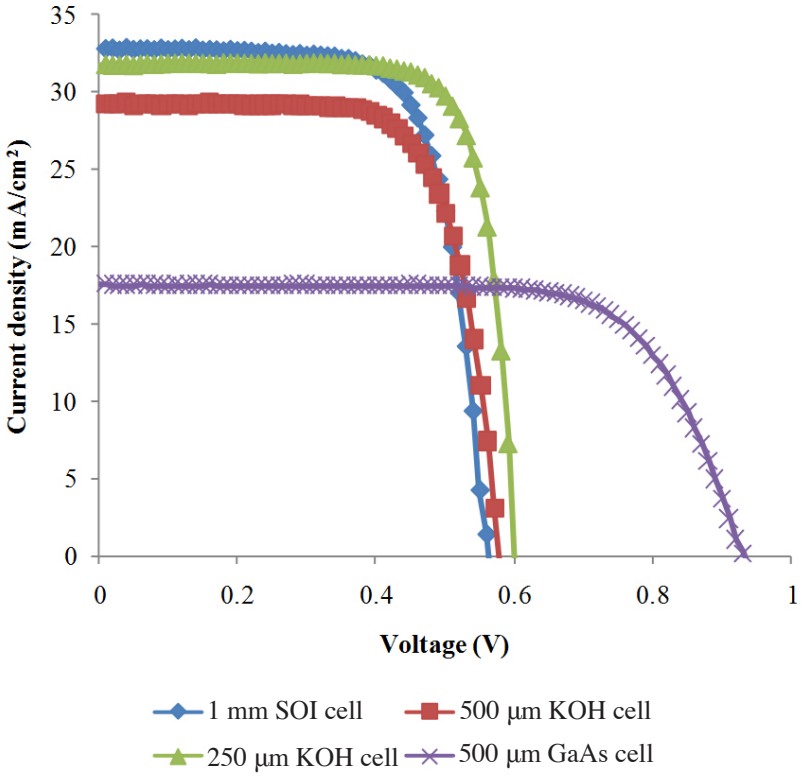
These microscale PV cells generate electricity through the photovoltaic effect. When light shines on the semiconductor, electrons are excited, drift and diffuse in the material, and then are collected at the terminals.

To fabricate these cells, Sandia's MEPV team combine microfabrication techniques from several microsystem technologies. The process flow uses standard equipment and standard wafer thicknesses and allows all high-temperature processing to be performed prior to cell release. In addition, the remaining post-release wafer can be reprocessed and reused resulting in an order-of-magnitude increase in the number of watts generated per gram of expensive semiconductor material (see Comparison Matrix in Section 12B). The c-Si PV cell junctions are created using a backside point-contact PV cell process. The GaAs PV cells have an epitaxially grown horizontal junction. Despite the horizontal junction, these cells also are backside contacted, which enables the fabrication of uniform, aesthetically pleasing front sides without electrical lines.

To characterize the operation of the microscale PV cells, our technologists packaged and connected them for performance testing. Current-Voltage (J-V) curves were obtained under American Society for Test Materials (ASTM) one-sun illuminating conditions. We used a Spectrolab model XT-10 with a 1 kW, short

arc, xenon lamp, class A solar simulator normalized to 1000 W/m^2 using a silicon reference cell. The beam is an 8"x 8" square, and the chuck is temperature controlled using thermoelectrics. The microscale PV cells were connected to a Keithley source meter instrument by the four wire method to obtain the J-V curves. Figure 4 shows the J-V curves of our GaAs and c-Si PV cells to date.

As shown in Figure 4, Sandia's 250-µm wide, 14-µm thick c-Si PV cells have achieved 14.9% conversion efficiency. This level of performance is comparable to the conversion efficiency in the majority of commercially produced c-Si PV cells that are 10–15x thicker. For the single-junction GaAs cell, the conversion efficiency of 11.36% can be boosted to 20–25% with the addition of an anti-reflective coating and the absence of the 1-µm thick InGaP window layer, which our designers incorporated for a future microscale InGaP cell as part of a III-V integrated multijunction PV cell design. For both c-Si and GaAs microscale PV cells, the look, feel, and functional performance of the cells can be systematically improved using the fabrication process developed by the Sandia MEPV team and described in Section 11.



	250 µm KOH	500 µm KOH	1 mm SOI	500 µm GaAs
Efficiency (%)	14.86	12.03	12.87	11.36
V_{oc} (mV)	597	575	562	930
J_{sc} (mA/cm^2)	31.75	29.29	32.07	17.2
FF (%)	78.4	71.2	71.4	71

Figure 4. *PV cell results to date for different materials, sizes, and release approaches. (Source: Sandia)*

11. Building Blocks of MEPV Technology

Our manufacturing processes produce microscale PV cells in two different types of crystalline Si and crystalline GaAs. Each cell type takes advantage of a mechanism for detaching the first 1–20 µm of material from the top of the wafer to create the cells, leaving the rest of the material for future cell production runs and boosting the watts-per-gram usage of the expensive semiconductor material in the wafer by an order of magnitude. The c-Si PV cells are released using either hydrofluoric acid (HF) with silicon-on-insulator (SOI) wafers, or potassium hydroxide (KOH) with (111) oriented wafers. The GaAs cells are released using an aluminum arsenide (AlAs) release layer and HF release chemistry similar to epitaxial lift-off (ELO), but without the supporting release handle that is typically used; this is a manufacturing technique that is familiar to the semiconductor industry.

Production of Microscale Silicon-On-Insulator (SOI) c-Si PV Cells

Figure 5 illustrates the various designs for the SOI-based cells. The n-implantation is in the center and the p-implantation is on the outer rim. Fingers of n-implanted dopants go from the center contact towards the edge without touching the edge, and p-implanted fingers go from the edge towards the center without touching the center. The purpose of these fingers is to reduce the space between the p- and

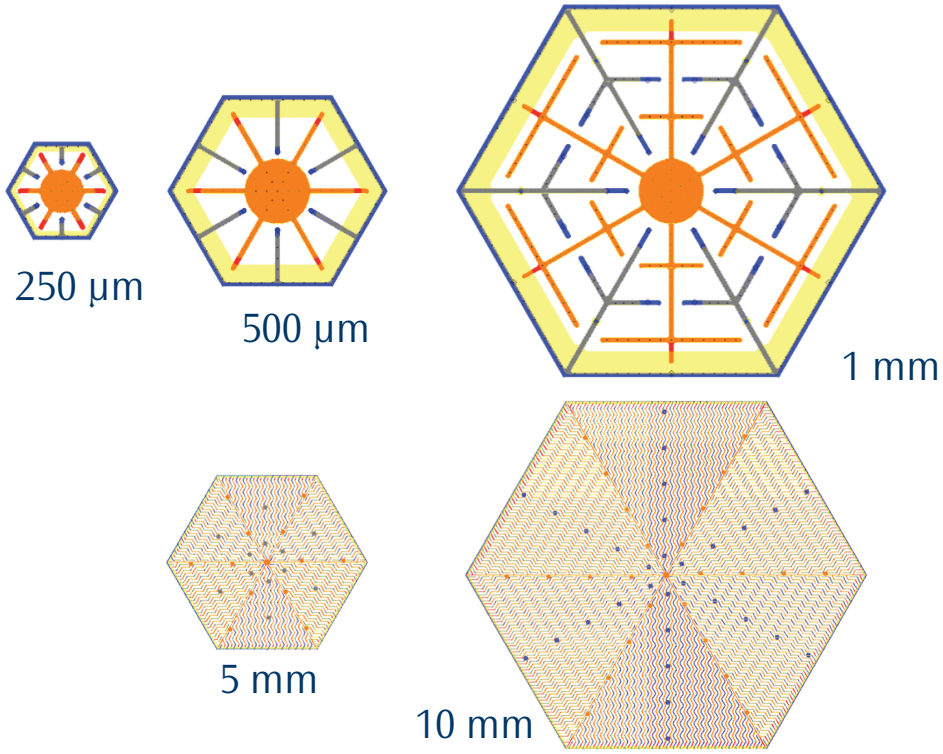


Figure 5. *AutoCAD drawings of mask designs for the radial solar cells of various lateral sizes. (Source: Sandia)*

n-areas and thus enhance carrier collection. The metal contact layer follows the same shape as the implantations below, but only contacts the semiconductor in very small areas (point contacts) through a nitride layer. Figure 6 shows an SEM image and an optical profilometer image of a released 20-µm thick, 1-mm wide c-Si PV cell.

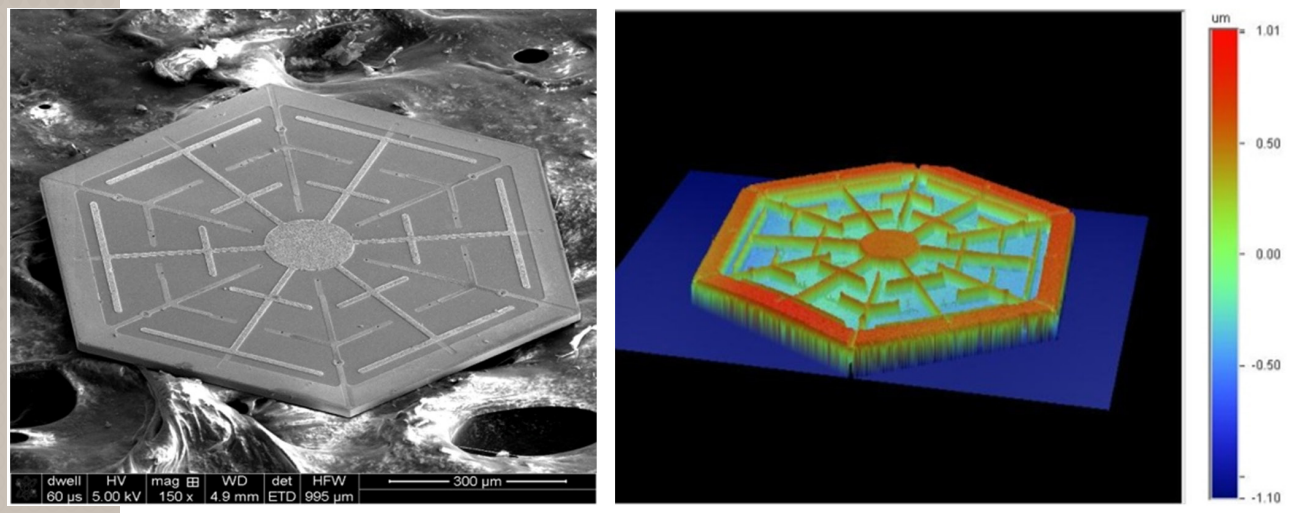


Figure 6. *SEM and optical profilometer image of a 20-µm thick, 1-mm wide c-Si PV cell fabricated from an SOI wafer. (Source: Sandia)*

Production of Microscale (111) c-Si PV Cells

The second approach to fabricate c-Si PV cells uses the crystal plane selective KOH silicon etchant. Compared to the SOI wafer process, this approach has an additional photolithography mask and doesn't require a buried silicon dioxide (SiO_2) layer in the wafer.

Figure 7 illustrates the various designs for these cells. These designs use linear interdigitated metal contact fingers to bring the collected carriers to contacts on either side of the cell. The n- and p-type dopant implantations are performed at alternating positions across the backside of the cell. There are two cell sizes with variations on the size and spacing of the implantation locations for both cell sizes, as shown in Figure 8 and Table 1.

These designs use linear interdigitated metal contact fingers to bring the collected carriers to contacts on either side of the cell.

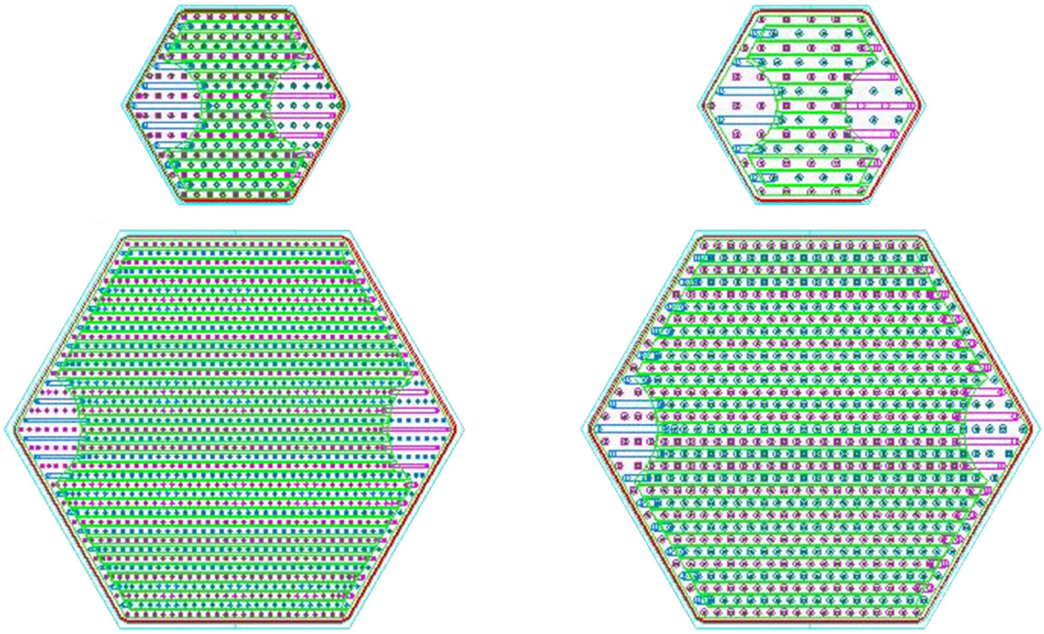


Figure 7. *250-µm and 500-µm linear contact cell designs with interdigitated fingers. (Source: Sandia)*

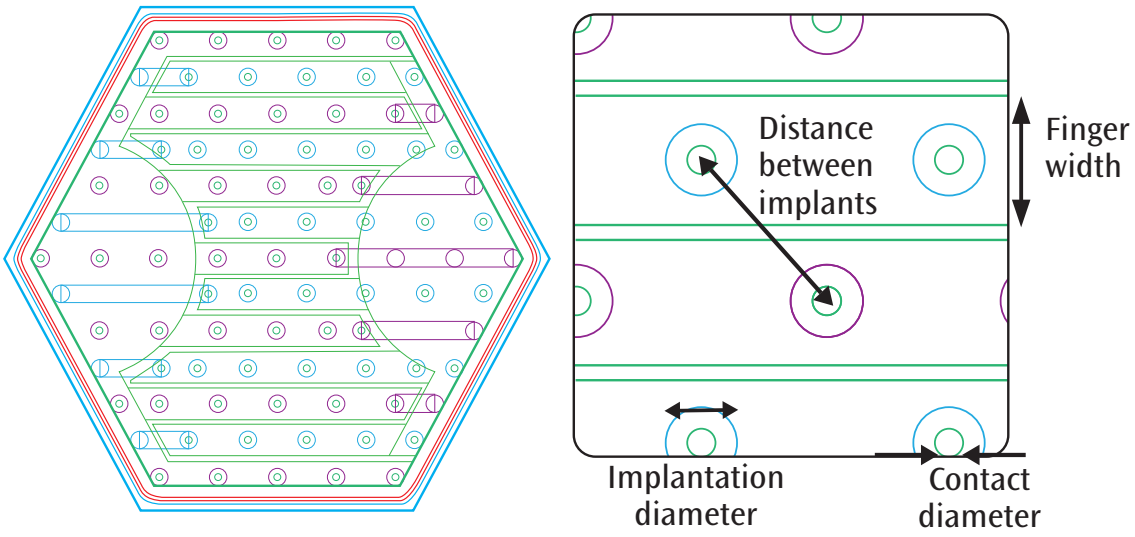


Figure 8. *Left: AutoCAD design of a 250-µm wide c-Si PV cell (backside contacted) with interdigitated fingers. Right: Detail of the implantations and fingers. (Source: Sandia)*

Size of cell and design	Distance between implantations (µm)	Width of finger (µm)	Diameter of implantation (µm)	Diameter of contact (µm)
250-µm tight	13	8.9	6	3
250-µm relaxed	21	13.9	8	3
500-µm tight	12.2	8.6	4	2
500-µm relaxed	15.3	11.5	8	3

Table 1. *Linear Contact Cell Dimensions.*

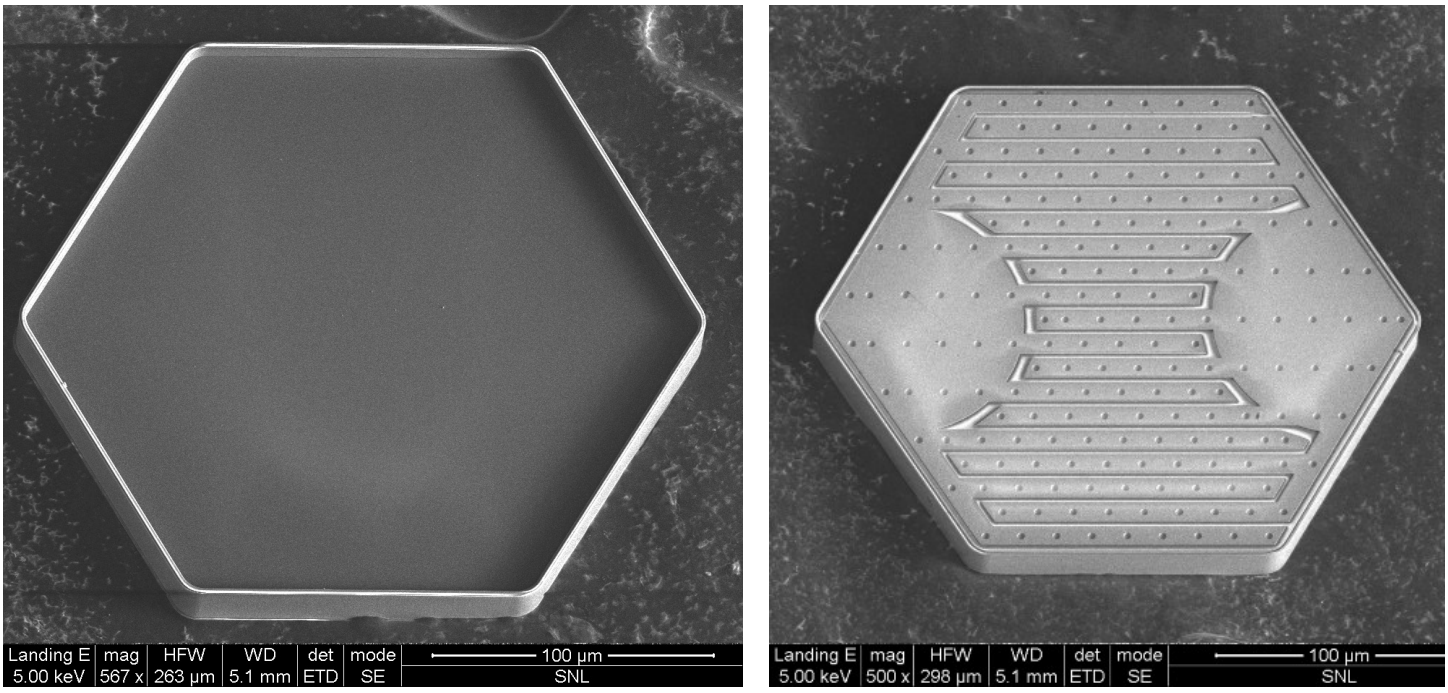


Figure 9. *SEM image of the front side (left) and back side (right) of a 250-µm wide c-Si PV cell fabricated from a (111) oriented wafer. (Source: Sandia)*

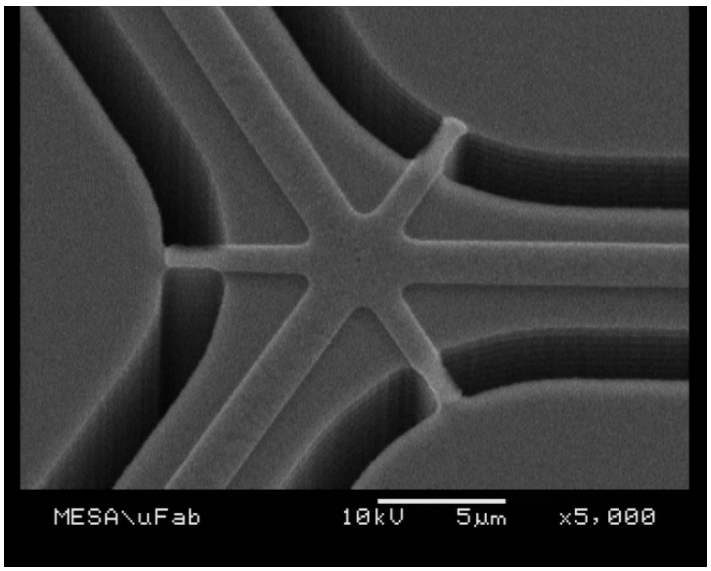


Figure 10. *SEM image of the tether holding the microscale c-Si PV cell to the wafer. (Source: Sandia)*

Figure 9 shows the front and back side of a cell manufactured from a (111) oriented wafer. Only 25 to 30 µm of material from the wafer were used to create the cells, leaving 670 µm of silicon for boosting watts-per-gram wafer output through subsequent cell production runs.

Release of Microscale c-Si PV Cells with Bump Bonds

For both microscale SOI and (111) c-Si PV cell fabrication processes, the finished cells can be released from the wafer into a solution with no particular organization. In order to produce organized arrays of microscale c-Si PV cells, the Sandia MEPV team developed a similar process to the one presented for SOI wafers with the cells tethered to the substrate (see Figure 10).

The tethers allow the cells to be transferred in ordered arrays onto tape for pick-and-place assembly or directly placed onto an interconnected substrate to make a functional module.

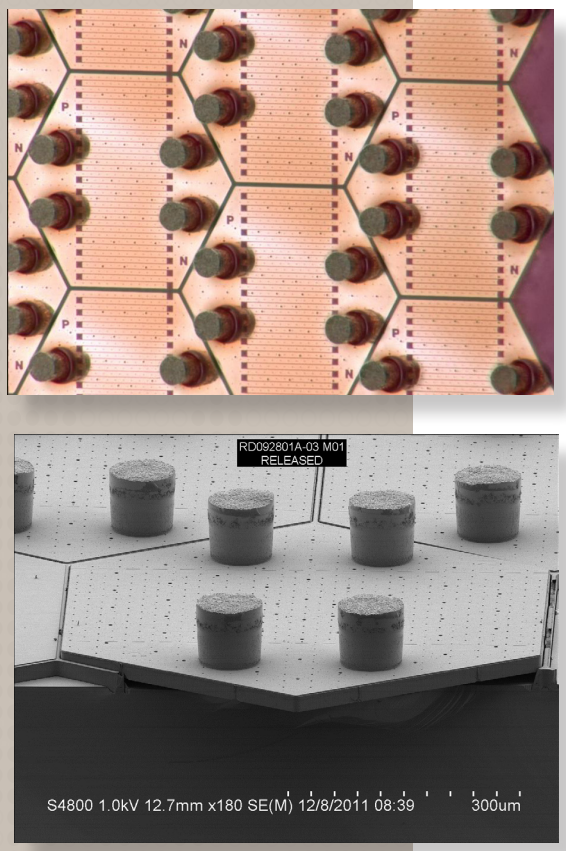


Figure 11. *(top) An array of microscale PV cells with bump bonds attached to the wafer; (bottom) A detailed SEM image of the cells with solder bumps. (Source: Sandia)*

The tethered cells are fabricated using SOI wafers. The junctions are created with ion implantations through masking layers created with photolithography. Once the junction is created, anchors that connect the cell to the wafer are defined with a deep reactive ion etch (DRIE). A prerelease step suspends the cells over the wafer handle. These anchors allow passivation and antireflection (AR) coatings to be deposited on the front, back, and sides of the cell while the cell is still attached to the wafer. After passivation, the contact formation and metallization steps follow.

The final process creates solder bumps that can be used for mechanical and electrical connections to other substrates. The solder bumps are created using standard wafer bumping processes available to the microelectronics industry. In this process, a seed metal is deposited and then a photoresist layer is patterned across the wafer. Inside the features, copper and standard tin-lead solder are plated over the seed metal. Once the bumps are formed, the photoresist that was used as a template is removed. Figure 11 shows an array of microscale c-Si PV cells with bump bonds attached to the wafer and a detailed SEM image of the cells with solder bumps.

After the tethered cells with solder bumps are fabricated, the cells are transferred onto a tape for pick-and-place assembly or are directly attached to an interconnected substrate. Figure 12 illustrates this detachment process whereby the cells are attached to an ultraviolet (UV) releasable tape or an interconnected substrate.

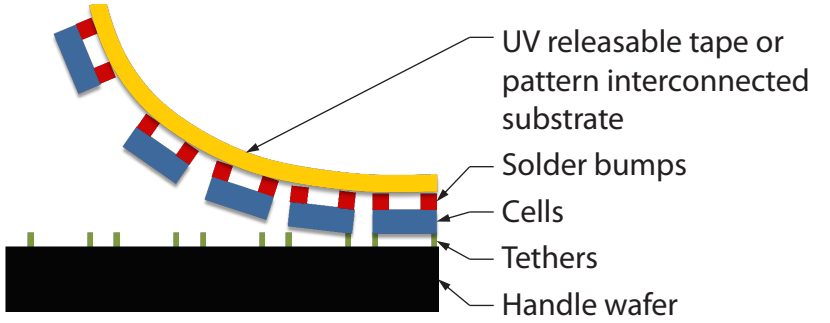
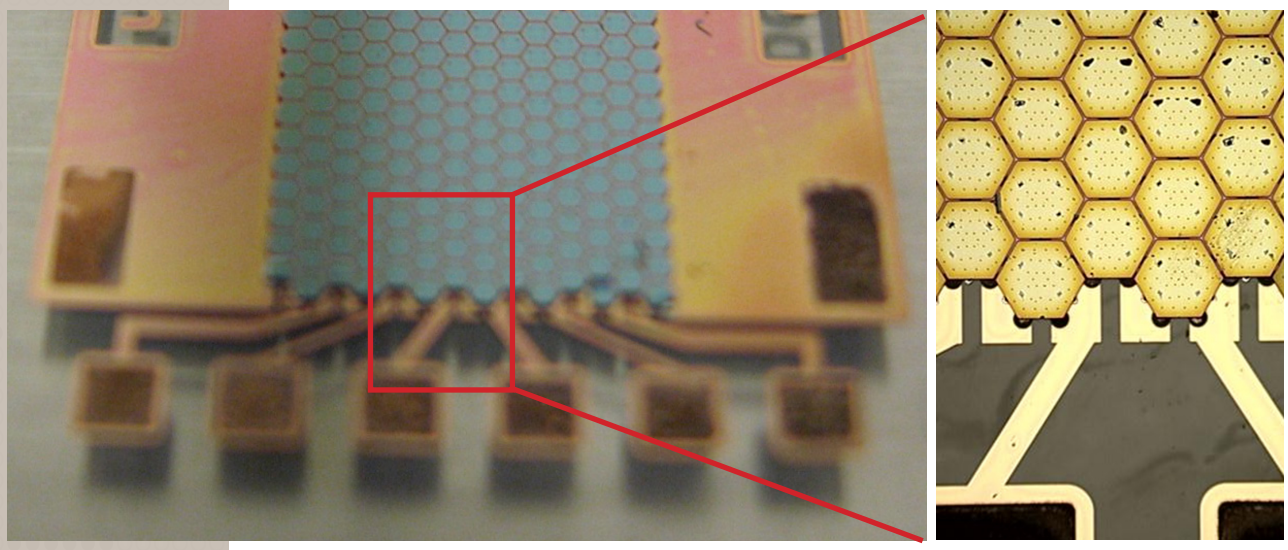


Figure 12. *Detachment process of bumped cells onto tape or an interconnected substrate. (Source: Sandia)*



(a) (b)

Figure 13. *(a) MEPV one-sun module consisting of 500-µm wide cells. (b) Magnified image of a MEPV one-sun module. (Source: Sandia)*

If a receiving substrate with metal interconnections is used (e.g., a flex circuit with patterned polyimide), an alignment of the features in the cells with the metal traces is necessary before detachment. After alignment, the receiving substrate and the cells are heated up to 250°C to reflow the solder. After cooling, the electrical and mechanical connections are in place. The final step is detaching the handle wafer from the cells to leave the front of the cells exposed. Figure 13 shows an operational MEPV module consisting of microscale c-Si PV cells interconnected through the solder bumps. The receiving substrate has 14 columns of cells in series, and each column has 47 cells in parallel.

Production of Gallium Arsenide Cells

The single-junction, crystalline GaAs cells are created through epitaxial growth followed by processing to create the metallized contacts. This approach creates a horizontal junction which normally requires a front and back metal contact. By making the cells very small, it is possible to use a backside contact method that moves all of the metal outside of the optical aperture. In addition to avoiding optical losses, the backside contacts facilitate the packaging of the cells since only one side needs to be interconnected. To our knowledge, these are the first fully backside-contacted GaAs solar cells practically produced and demonstrated.

The initial epitaxial layers are illustrated in Figure 14. It should be noted that the cell is designed to be inverted, which allows the backside of the cell to be available for the microprocessing required to create backside contacts. The cell is also designed to be incorporated into a 3D integrated multijunction stack with

a microscale InGaP cell above it. The epitaxy to create the layers comprising the cell was performed at the National Renewable Energy Laboratory (NREL). The microprocessing and cell release were performed at Sandia National Laboratories. The release of the cells is accomplished by including an AlAs sacrificial layer in the epitaxial stack. The AlAs was selectively etched using a solution of 49% HF in water with Tergitol™ added to reduce the surface adhesion effects that can cause cells to stick to the wafer after release.

In addition to avoiding optical losses, the backside contacts facilitate the packaging of the cells since only one side needs to be interconnected. To our knowledge, these are the first fully backside-contacted GaAs solar cells practically produced and demonstrated.

Because of the small size of the cells, the lift-off process can be completed in eight minutes (in contrast to the approximately day-long release times required for full wafer epitaxial lift-off). As with the c-Si processes, the watts-per-gram output from the entire wafer can be boosted dramatically by reprocessing the handle wafer to grow and release subsequent batches of cells.

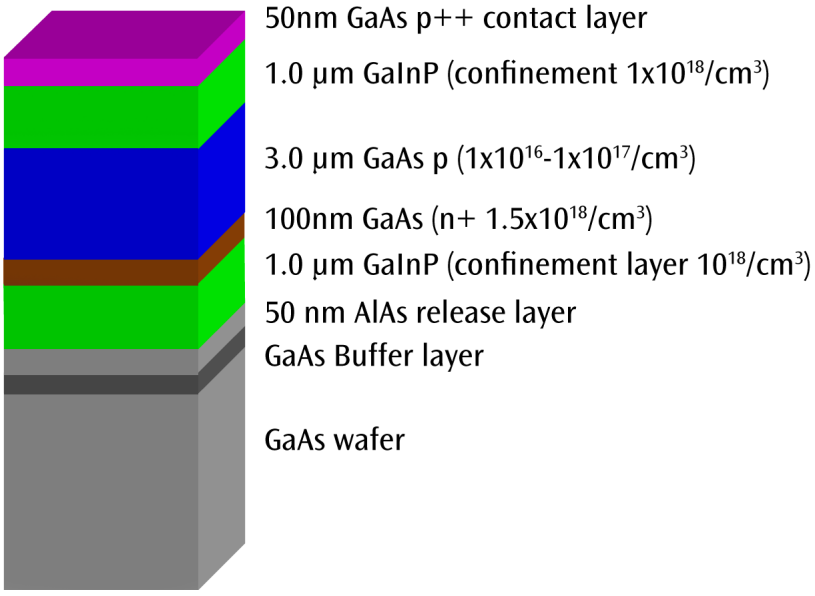
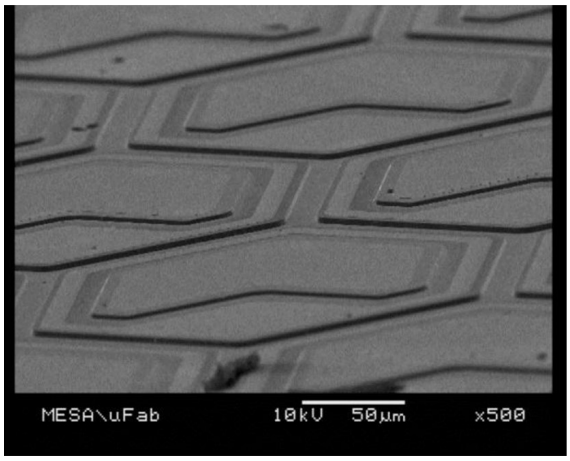
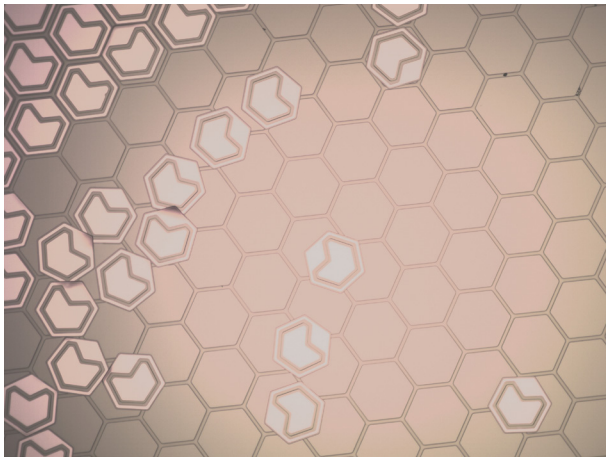


Figure 14. *Epitaxial layer stack for the inverted GaAs single-junction cell. (Source: NREL)*

Recent developments associated with Sandia's microscale GaAs cells include a new residual strain-balanced cell design to reduce the curvature of the cells after release. Our III-V process engineers also increased the doping levels in the InGaP window layer used for one of the contacts; this led to reduced contact resistance between the metallization and the InGaP layer resulting in improved performance. Finally, our III-V designers increased the thickness of the absorbing layer of the GaAs cells yielding further performance improvements. Figure 15 shows representative images of the single-junction GaAs PV cells fabricated at Sandia.

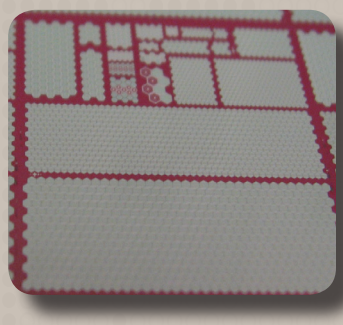




(a) (b)

Figure 15. *(a) An SEM image of 250-µm wide, single-junction GaAs PV cells just prior to release. (b) Magnified image of 250-µm wide GaAs PV cells in the process of being released from the wafer. (Source: Sandia)*

(i)



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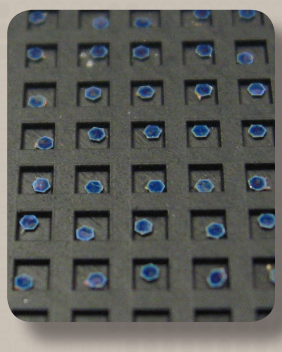
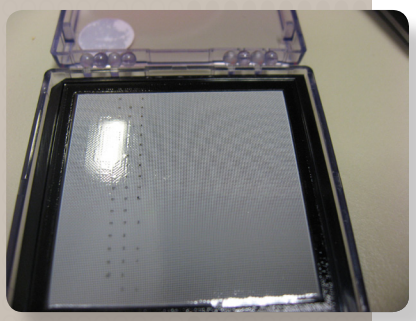


(iii)



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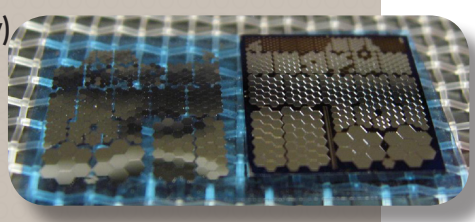


Packaging Microscale Photovoltaic Cells

Whichever of the three cell manufacturing processes is used, the fabricated cells can be shipped using packaging methods that readily accommodate a variety of end uses:

- Cells can be sent on wafer and released by the end user (i). In this case, the end user would have special tools for cell release or for directly picking cells off the wafer.
- Cells can be sent singulated and placed in waffle packs (ii) which is a well-suited delivery approach for sparse arrays, quality control testing, and sorting.
- Cells can be delivered on gel packs (iii) or transferred onto tape (iv). In this format, standard pick-and-place tools from the integrated circuit and microsystems industry can be used to incorporate the cells into specific devices.
- Cells can be shipped in solution (v). This may be the best form of delivery for end users who wish to operate the cells in a liquid or use new types of directed self-assembly techniques for massively parallel placement of the cells onto a receiving substrate.

(v)

12. Product Comparison

A. List your product's competitors by manufacturer, brand name, and model number.

- Global Solar, PowerFLEX, BIPV 300W
- Unisolar, PowerBond, PVL-144
- Konarka, Power Plastic 40, BIPV 300W Series 1140
- SunPower, E20 Series, 327

B. Comparison Matrix

	Materials	Microscale Dimensions	3D Moldable	Non-Lattice Matched	Flexibility	Shading Tolerance	Module Output Voltage	Thickness	Shown Module or Cell Efficiency	Potential Efficiency	Watts/Kg
Sandia MEPV	**c-Si and III-V**	✓	✓	✓	**HIGH**	**HIGH**	**.5 to 1000 V**	**1-20 µm**	**15% (cell)**	**>50%**	**>400**
Commercial Products											
Global Solar (PowerFLEX BIPV 300W)	CIGS	×	×	×	LOW	LOW	53.9 V	1.7 µm (thin film)	12.6% (module)	22-24%	30.3
Unisolar (Power Bond PVL-144)	a-Si	×	×	×	LOW-MED	LOW	33 V	1-5 µm (thin film)	6.7% (module)	15-20%	18.7
Konarka (Power Plastic 40 Series 1140)	Organic	×	×	×	HIGH	LOW	15.2 V	1-5 µm (thin film)	1.7% (module)	10-15%	Not listed
SunPower (E20 327)	c-Si	×	×	×	NO	LOW	54.7 V	180 µm	20.1% (module)	26-28%	17.6
R&D Activities											
Alta Devices	GaAs	×	×	×	MED	LOW	Not listed	1-2 µm	28% (cell)	28-30%	Not listed
Semprius	III-V	✓	×	✓	NO	LOW	≈50 V	10 µm	41% (cell)	42-44%	Not listed
Origin Energy	c-Si	✓	×	×	MED	MED	40 V	50 µm	~18% (cell)	26-28%	220
Rogers Research Group, Univ. of Illinois	c-Si and III-V	✓	×	×	MED	MED	Not listed	15 µm	4-8% (cell)	26-28%	Not listed
Kyosemi (Spherlar F12-12S1P)	c-Si	✓	✓	×	NO	Not listed	6 V	1-2 mm (round)	6%	26-28%	≈10
Ampulse	c-Si on Metal	×	×	×	LOW-MED	Not listed	Not listed	Not listed	Not listed	12-20%	Not listed
Twin Creeks	Cleaved c-Si	×	×	×	MED	Not listed	Not listed	10-20 µm	Not listed	15-22%	Not listed
Si-Gen	Cleaved c-Si	×	×	×	MED	Not listed	Not listed	20-100 µm	Not listed	15-22%	Not listed
National Renewable Energy Lab (NREL)	III-V	×	×	✓	NO	Not listed	Not listed	10 µm	41% (cell)	40-45%	Not listed

Table 2. *Comparison of our microscale PV technology in 11 distinct categories with 13 products in the commercial or R&D stage. The materials column refers to the main active material used to convert light into electricity: CIGS is copper indium gallium diselenide, a-Si is amorphous silicon, c-Si is crystalline silicon, and III-V refers to combinations of compound semiconductors made of elements from the third and fifth column of the periodic table of elements such as GaAs, InGaP, AlInGaP, and GaN. The microscale dimensions column indicates whether the PV cells have a width or length less than one millimeter. The 3D moldable column refers to the ability of the cells to be molded into arbitrary shapes. Non-lattice match refers to the use of electrically decoupled, mechanically stacked cells. Flexibility refers to the smallest radii of curvature obtainable without damaging the photovoltaic functionality of the cell: high flexibility refers to resulting radii of curvature of 4 mm or less, med refers to radii of curvature from 5 mm to about 4 cm and low to greater than 4 cm. High shading tolerance indicates that up to 75% of the module could be shaded and still be functional, medium tolerance is between 25 to 75% and low tolerance below 25%. Module output voltage is the voltage correspondent to the maximum power point of the module. The thickness column only considers the active part of the cell. The shown cell or module efficiency was obtained from published data in journals or from vendor websites. The potential efficiency was obtained from predictions in the literature and the Watts/kg was obtained from data sheets.*

C. Improvements over Competitive Products

Compared with existing commercial PV products and PV technologies under development, Sandia's microsystems enabled PV technology offers new functionality, improved performance, and reduced cost.

New Functionality

In contrast with macroscale c-Si and III-V PV cells, miniaturized c-Si and III-V PV cells can fit within the intricate shapes and contours of objects. Sandia's microscale PV cells can be incorporated into the molding process of rigid products or into highly flexible substrates, providing built-in electricity generation capability.

In addition, our microscale c-Si PV cells can be color customized through small changes in the thickness of the deposited passivation/AR layer (see Figure 16). While color c-Si PV cells have lower conversion efficiency than dark blue or black c-Si PV cells, the performance would still be superior to color organic PV cells (see Konarka in Section 12B). More importantly, color customization would invite architects, industrial designers, and marketers to integrate microscale c-Si PV cells into products that presently don't use commercial PV cells because of their "ugly" look and feel.

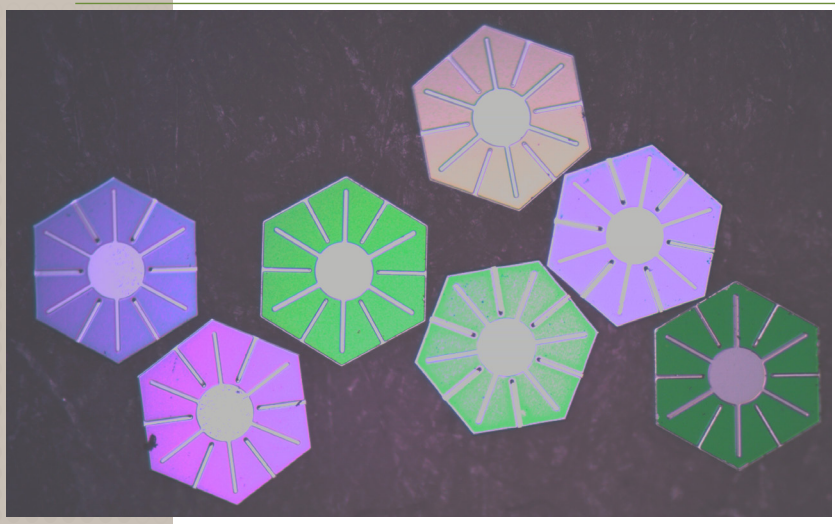


Figure 16. *Seven 500-µm wide microscale c-Si PV cells shown in a variety of colors. The color variation is set by different thicknesses of the nitride layer deposited for passivation. (Source: Sandia)*

Improved Performance

Miniaturizing PV cells opens up new ways to enhance performance at the cell, module, and system level. The Sandia MEPV team has created module designs using microscale PV cells to generate high voltages (>100 V) within small areas (<1 cm^2). High voltage modules with our microscale PV cells can operate without DC-to-DC converters, reducing resistive losses, improving shading performance, and enhancing robustness to individual cell failures.

The miniaturized individual cells also open up the design space for developing high-efficiency PV systems. Using 3D integration processes from the microelectronics industry, our microscale PV cells can be configured with

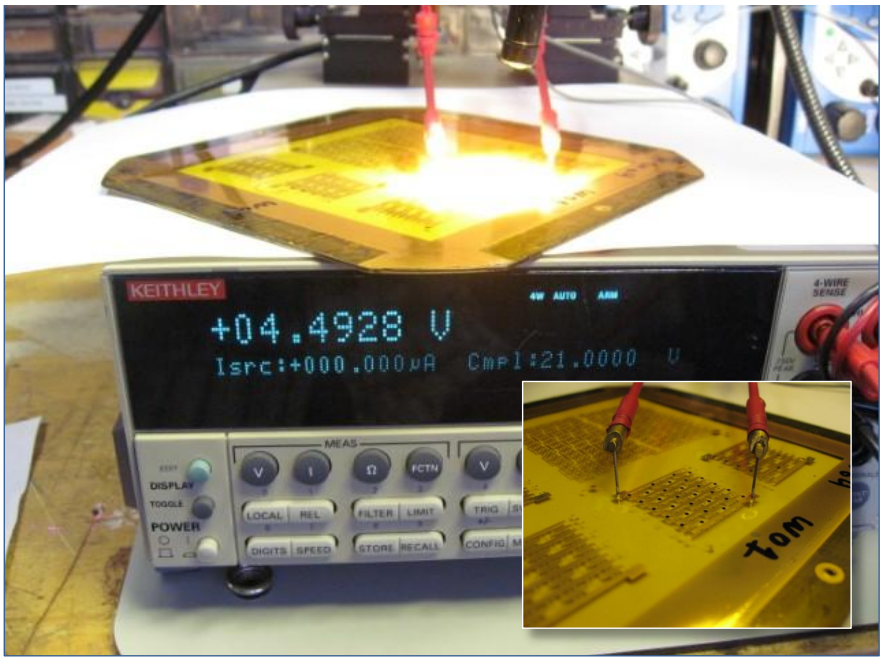


Figure 17. *MEPV sparse array under illumination producing 4.5 Volts (0.45 V per cell) over an active area of 0.18 cm². The inset shows the MEPV module before illumination. (Source: Sandia)*

independent electrical connections thereby overcoming the operational handicaps of lattice and current matching found in commercial multijunction PV cells. As a result, Sandia's microscale PV technology provides not only the building blocks, but also a viable path for developing PV systems with greater than 50% conversion efficiency.

Reduced Cost

While there are multiple ventures attempting to reduce semiconductor material usage and waste in PV cell fabrication (see Comparison Matrix in Section 12B), semiconductor material costs are only 15-25% of the overall PV system cost. In addition to reducing semiconductor material costs by boosting watts-per-kilogram output to greater than 400 and increasing system efficiency to greater than 50%, Sandia's microscale PV technology can reduce costs through the adoption of manufacturing processes familiar to the semiconductor, LCD, and microsystems industry. Most of the ventures listed in the Comparison Matrix have to develop PV production tools and processes that are particular to the technology they are developing. Our microscale PV technology can take full advantage of the tools and methods that have produced systematic and significant cost reductions in other high-tech industries that also use c-Si and III-V materials for the mass production of electronic products (see Principal Applications and Benefits in Section 13A for more technical details).

D. Limitations of Microsystems Enabled Photovoltaics

While MEPV technology has increasingly become known for its versatility, the adoption of this technology ultimately depends on the monetary value placed on the electricity provided. This is illustrated in Figure 18, which is a zero profit margin cost model graph produced by our team for the MEPV technology.

For one-sun applications (i.e., no optical concentration), the dollar-per-watt cost associated with our microscale PV technology is \$3.50-\$4.00/$Watt_{peak}$. At this cost point, MEPV technology is most suitable for mobile power applications (e.g., handheld devices, soldier power, off-grid deployments) where the consumer has already demonstrated a willingness to pay \$20-\$40/$Watt_{peak}$ and the device designers and manufacturers can yield a profit margin comparable with that of the semiconductor industry (i.e., >20%). For residential rooftops which require a \$1.00-\$2.00/$Watt_{peak}$ price point to be competitive with grid power, MEPV is not realistically viable for this market since homeowners prefer fixed PV systems over sun tracking PV systems.

"At ARCH, we like platform technologies (that is, technologies that can address multiple applications), and this is definitely a platform technology."

—Clinton W. Bybee,
Co-Founder and Managing Director, ARCH Venture Partners, July 13, 2009

For 60-100 sun applications (i.e., moderate optical concentration), the dollar-per-watt cost associated with our microscale PV technology reaches \$0.40/$Watt_{peak}$ (see Figure 18). At this cost point, MEPV technology becomes financially compelling for low profit margin utility farms that provide wholesale electricity as well as big box and warehouse rooftops for production of retail electricity. For regional markets with extremely low utility rates (e.g., Pennsylvania, Utah), MEPV even in concentrating systems may not be the lowest cost electricity option.

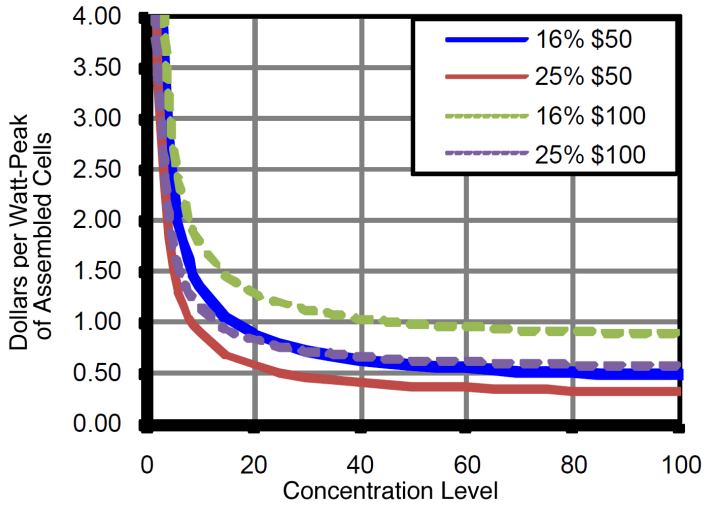


Figure 18. *Cost projections at zero profit margin for \$100/m² and \$50/m² panel assembly costs. These assume eight-inch wafer production, 95% cell yield, 15% incoming light loss due to diffuse light, 6% optical lens loss and standard silicon processing tools. (Source: Sandia)*

13. Product Use

A. Principal Applications and Benefits

With the development of a decentralized electricity grid, the emerging electrification of personal transportation, growing dependence on mobile devices, and persistent concerns about atmospheric emissions from fossil fuel use, there is a drastic need for clean and convenient ways to generate electricity. Our microscale PV cells have the ability to produce this electricity from a variety of light sources, the scalability for multi-megawatt to gigawatt electricity generation, and the versatility to be incorporated directly into devices that need power. These building blocks can be installed in flexible, moldable, or flat-plate formats in sizes that conform to the shapes and contours of natural terrain, large structures, vehicles, and mobile electronics. The benefits associated with miniaturizing PV cells to microscale sizes can be seen at the cell, module, and system level.

"The introduction of MEPV cells will enable ground, flight, and space based units to engineer the geometry of their power systems to the constraints of their platforms and associated payloads."

— Jeffrey H. Hunt
Boeing Technical Fellow, Editor-in-Chief of Boeing Technical Journal, and American Physical Society Fellow at the Boeing Company

At the cell level,

- A single 725-µm thick, eight-inch wafer can be used as a base substrate to produce multiple lots of microscale PV cells since only 5-25 µm of the wafer are consumed in each batch.
- Small scale hexagonal cells better utilize the available wafer area by reducing edge die losses.
- The MEPV cell fabrication process eliminates the semiconductor material waste that is an inherent part of wafer-saw PV production.
- Small cell dimensions with effective passivation improve carrier collection.
- To facilitate handling, all high-temperature processing steps (patterning,

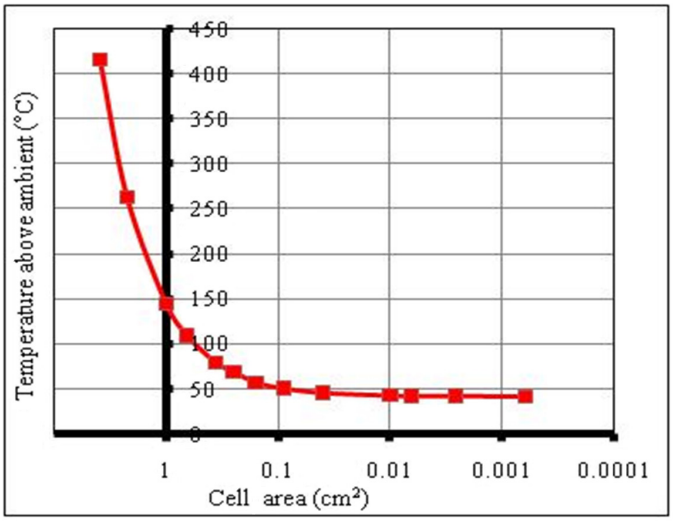


Figure 19. *Finite element analysis of thermal behavior of a 500X concentrator system, cooled by convection. The figure gives the cell operating temperature above ambient for cells of decreasing size. This indicates that for cells less than about 1 mm², the operating temperature is essentially that of a one-sun module. (Source: Sandia)*

diffusion, passivation, and metallization) are done on wafer using an MEPV suspension and tethering process.
- Semiconductor manufacturers can use any wafer size, enabling the use of older fabrication lines that handle 4-8 inch wafers.
- In contrast with present wafer silicon PV cell fabrication processes which have inherent limitations on wafer size due to current collection and wafer handling, microscale PV cell fabrication takes full advantage of the cost benefits associated with ever larger wafer sizes.

At the module level,
- Assembly can be performed at the rate of 130,000 parts per hour for concentrator applications using standard pick-and-place tools for microelectronics assembly.
- Materials selection for the module is less temperature constrained, and can therefore be lower cost, since all high-temperature processing can be done on the wafer.
- Concentration can be performed with 93-96% optically efficient refractive microlens arrays instead of 75-80% efficient Fresnel lenses.
- Microscale cell sizes decrease focal lengths for concentrating optics, allowing direct lamination of optics to the PV cells.
- Microscale PV cells operate at lower temperatures compared with macroscale PV cells at the same concentration ratios thereby simplifying thermal management (see Figure 19).

At the system level,
- High voltage output directly from modules is possible due to the use of up to 15,000 cells/m^2, eliminating the need for DC-to-DC converters as well as thicker, more expensive system wiring.
- Incorporation of monitoring and power conditioning integrated circuits within the device can be done using the same pick-and-place tools used for the microscale PV cell assembly.
- Small relative displacements between the microscale PV cell array and the microlens array can provide high accuracy and high-bandwidth sun tracking, reducing the cost and complexity of sun tracking and providing pointing accuracy in windy conditions (due to the low profile of single-axis tracking and the high-speed response of in-plane tracking).
- Using these microscale PV cells, ultrathin (<20 μm) and flexible c-Si sheets can be created with the capability to bend at a radius of curvature of 2 mm without damaging the silicon structure.

"Sandia's microscale photovoltaics provide a chance to create a revolutionary change in cost effective solar generation that is flexible enough for large-scale utility installations to smaller distributed applications. This flexibility is important to utilities to best provide renewable generation at the best prices for our customers."

— Jonathon Hawkins,
Manager of Advanced Technology and Strategy, Public Service Company of New Mexico

"In my almost 40 years of solar cell research, which includes creating the AMPS computer code used worldwide for solar cell design and the writing of the book Solar Cell Device Physics, I have seen few truly new visions for improving solar cell costs and efficiency; Sandia's microscale photovoltaics is the most recent one I place into this special category."

— Stephen Fonash,
Director of the Center for Nanotechnology Education and Utilization and the Kunkle Chair Professor of Engineering Sciences, Pennsylvania State University

B. Other Applications

In addition to being used as building blocks for larger PV devices incorporated into mobile electronics and vehicles or installed on commercial rooftops and utility farms, the small size offers new capabilities to utilize light for powering processes and devices at microscales in a highly decentralized way.

Immersive Hydrogen Production

When our cell release team immersed batches of microscale PV cells in fluid for safe and convenient transport, this piqued the curiosity of our applications team members. Could electricity and electric fields generated by microscale PV cells immersed in fluid do useful work? From this posed question, the chemist on our team conducted an experiment where small patterned substrates (mimicking the small distance between electrodes) were submersed in a saline solution. These substrates were connected to an external power source (9 V battery) that provided the necessary power for electrolysis, resulting in the production of hydrogen and oxygen bubbling to the surface of the working fluid. In future experiments, our team will immerse and connect several microscale PV cells in series to provide sufficient voltage and power for electrolytic production of hydrogen.

Miniaturized, Self-Powered Devices

The LED, integrated circuit, and microsystems industries have produced a variety of miniaturized sensors, lights, and computational devices that are presently tied to the grid or powered with batteries. Our team has designed semiconductor

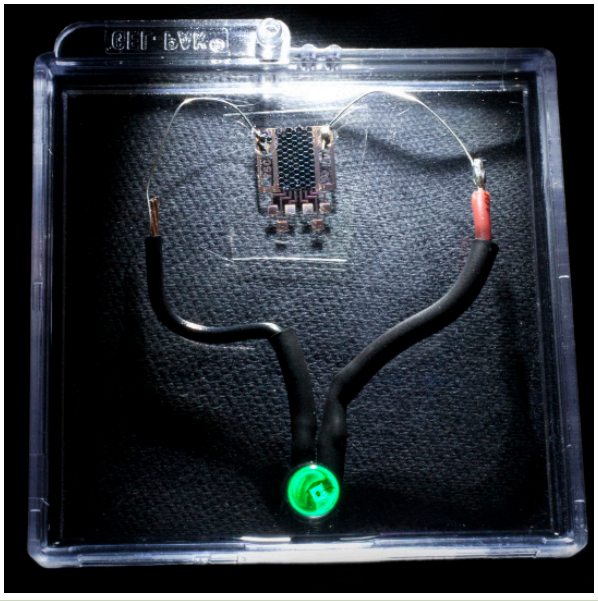


Figure 20. *LED device powered by a Sandia MEPV module. (Source: Sandia)*

assembly processes to integrate our microscale PV cells into these devices, providing usable or storable power of indefinite duration. To demonstrate the concept, our team has developed and tested ultrathin charge controllers that could be used as part of the design for a miniaturized self-powered device.

To cite one example, the concept of miniaturized, self-powered devices has attracted the interest of jewelry designers who would like to use microscale PV cells to power the rotation of set gemstones, subtly enhancing the sparkle without revealing the underlying power source. In addition to jewelry, microscale PV cells could be designed to fit aesthetically or unnoticeably into any miniaturized object.

14. Summary

The world is filled with various shapes and contours: natural terrain, large manmade structures, vehicles, handheld devices, and even the human body. Miniaturized PV cells can be designed to fit aesthetically and cost effectively into many of these objects, providing power automatically without human thought or attention.

The Sandia team's development of microsystems enabled PV shows specific ways to use tools and techniques from the semiconductor, LCD, and microsystems industries to design, simulate, fabricate, assemble, package, and characterize microscale PV cells. Through this methodical process for mass production, the conversion efficiency of commercial microscale PV cells can be improved to the full potential of the semiconductor material and evolving system designs.

In addition, the material costs of the overall PV system can become of lesser significance than manufacturing costs. If and when that happens, PV technology can migrate from its currently shallow cost reduction trajectory as shown in Figure 21 to one that is noticeably steeper. While that transition may never attain the cost reduction slope of the integrated circuit or LCD industry, it can ultimately make microscale PV cells the lowest cost electricity option for at least three application markets — mobile power, wholesale electricity from solar utility farms, and retail electricity from flat commercial rooftops.

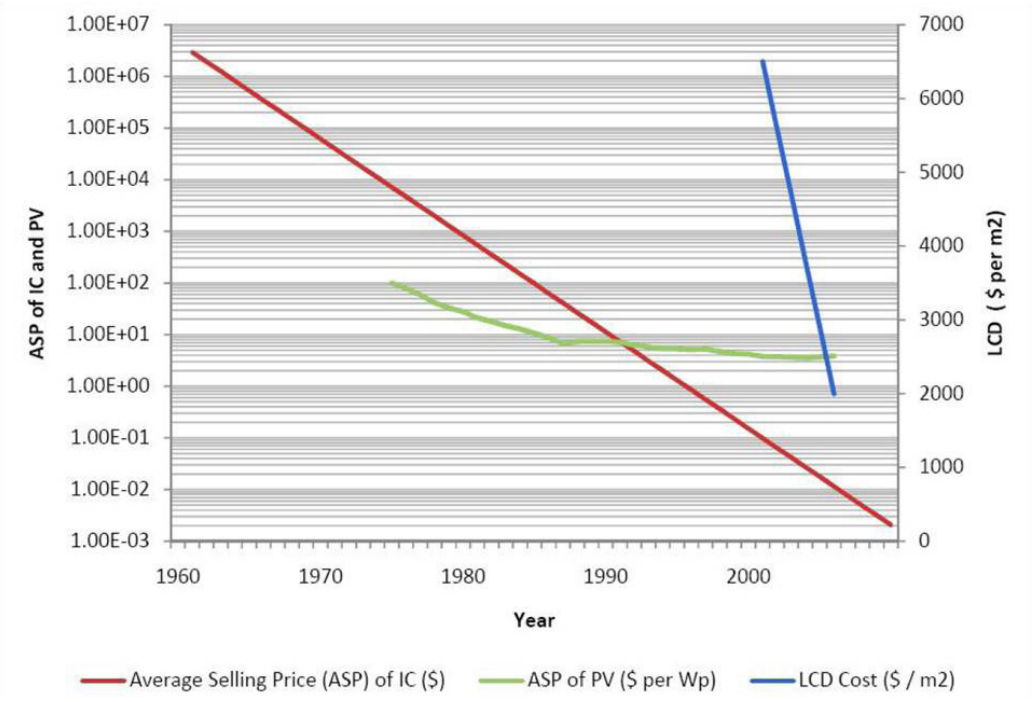
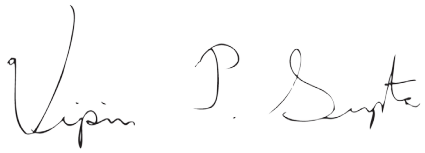


Figure 21. *Average selling price cost reduction of integrated circuit, PV, and LCD products. (Source: R. Singh, Journal of Nanophotonics, vol. 3, 2009)*

In contrast with the current policy- and subsidy-driven market for photovoltaics, these three distinct applications provide a diversified and consequently less capricious market to nurture the emergence of a microscale PV industry. Just as lithium ion battery development for the laptop computer industry enabled the migration of this energy storage technology to electric vehicles, microscale PV products for these three distinct applications can provide the scale and necessary revenue stream to develop new microscale PV technologies for other nascent applications that presently reside only in our minds. If done right, the powering of almost anything could become as simple as exposing it to light.

15. Affirmation

By submitting this entry to R&D Magazine, I affirm that all information submitted as a part of, or supplemental to, this entry is a fair and accurate representation of this product.



Vipin P. Gupta

For a summary recap of Sandia's microsystems enabled photovoltaics, watch the short video at: http://mepv.sandia.gov or click the image above to play.

Appendices

Appendix A:	Submitter Information
Appendix B:	Development Team
Appendix C:	Publications
Appendix D:	Awards
Appendix E:	Letter of Support From Three Years Ago
Appendix F:	Letter of Interest Now
Appendix G:	MEPV Licensing Information
Appendix H:	Process Flow for the Creation and Release of c-Si PV Cells Using an SOI Wafer
Appendix I:	Process Flow for the Creation and Release of c-Si PV Cells Using a (111) Oriented Wafer

Appendix A: Submitter Information

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"These guys are a talented bunch and are the type of scientists we like to follow because they will absolutely produce something interesting."

— Clinton W. Bybee,
Co-Founder and Managing Director, ARCH Venture Partners, July 13, 2009

Appendix B: Development Team (cont.)

Our MEPV Team

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Vipin Gupta
Jose Luis Cruz-Campa
Bill Sweatt

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Bradley Jared
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Ben Anderson
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Vipin Gupta
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Gerry Girard
InGaAsP Device Testing

Tammy Pluym
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Dan Koleske
InGaN Growth

Igal Brener
Photonics for low Eg PV cells/Light Trapping

Willie Luk
Photonics for low Eg PV cells/Light Trapping

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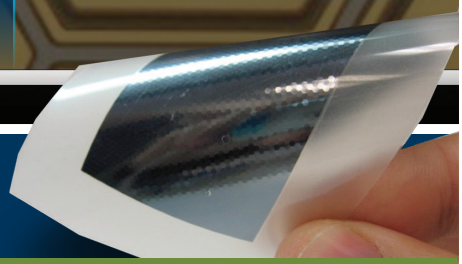

Appendix C: Publications

1. Nielson, G. N., Okandan, M., Cruz-Campa, J. L., Resnick, P. J., Wanlass, M. W., Clews, P. J., Pluym, T. C., Sanchez, C. A., Gupta, V. P., "Microfabrication of microsystem-enabled photovoltaic (MEPV) cells," SPIE Proc. Advanced Fabrication Technologies for Micro/Nano Optics and Photonics, vol. 7927, no. 4, CID No. 79270P (2011).

Out of 292 entrants, this technical article was one of eight to be selected for the SPIE Green Photonics Award at the 2011 Photonics West Conference in San Francisco, CA.

Microfabrication of microsystem-enabled photovoltaic (MEPV) cells

Gregory N. Nielson*[a], Murat Okandan[a], Jose L. Cruz-Campa[a], Paul J. Resnick[a], Mark W. Wanlass[b], Peggy J. Clews[a], Tammy C. Pluym[a], Carlos A. Sanchez[a], Vipin P. Gupta[a],
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ABSTRACT

Microsystem-Enabled Photovoltaic (MEPV) cells allow solar PV systems to take advantage of scaling benefits that occur as solar cells are reduced in size. We have developed MEPV cells that are 5 to 20 microns thick and down to 250 microns across. We have developed and demonstrated crystalline silicon (c-Si) cells with solar conversion efficiencies of 14.9%, and gallium arsenide (GaAs) cells with a conversion efficiency of 11.36%. In pursuing this work, we have identified over twenty scaling benefits that reduce PV system cost, improve performance, or allow new functionality.

To create these cells, we have combined microfabrication techniques from various microsystem technologies. We have focused our development efforts on creating a process flow that uses standard equipment and standard wafer thicknesses, allows all high-temperature processing to be performed prior to release, and allows the remaining post-release wafer to be reprocessed and reused. The c-Si cell junctions are created using a backside point-contact PV cell process. The GaAs cells have an epitaxially grown junction. Despite the horizontal junction, these cells also are backside contacted. We provide recent developments and details for all steps of the process including junction creation, surface passivation, metallization, and release.

Keywords: Microsystems enabled photovoltaics, micro solar cells, miniature solar cells, fabrication

1. INTRODUCTION

This paper describes the design and fabrication of miniature silicon solar cells that are created using microsystem tools and techniques. These miniature solar cells create a new class of photovoltaics with potentially novel applications and benefits such as dramatic reductions in cost, weight, and material usage.

We discuss the fabrication details of cells fabricated in two different types of crystalline silicon and crystalline GaAs. Each cell type takes advantage of a mechanism for detaching the first 1-20 μm of material from the top of the wafer to create the cells, leaving the rest of the material for future reuse. The crystalline silicon cells are released using either hydrofluoric acid (HF) with silicon-on-insulator (SOI) wafers (referred to as the radial electrode design), or potassium hydroxide (KOH) with (111) oriented wafers (referred to as the linear electrode design). The gallium arsenide cells are released using an aluminum arsenide release layer and a HF release chemistry, similar to epitaxial lift-off (ELO)[1], but without the supporting release handle typically used. Figure 1 provides an image of a representative crystalline silicon cell.

There is an obvious advantage to creating very thin solar cells, particularly with high-cost crystalline semiconductor materials. By reducing the thickness to the minimum required to obtain adequate absorption, significant materials savings can be realized. Figure 2 illustrates the cost savings realized by reducing the thickness of the silicon cells.

In addition, by reducing the lateral dimension of the solar cells, other scaling benefits are realized[2,3,4,5,6]. These benefits improve PV cell, module, and system performance; lead to new functionality not available with traditional cell technologies; and ultimately lead to multiple pathways to reduce cell, module, and system costs.

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Appendix C: Publications (cont.)

2. Cruz-Campa, J. L., Nielson, G. N., Resnick, P. J., Sanchez, C. A., Clews, P. J., Okandan, M., Friedmann, T., Gupta, V., "Ultrathin flexible crystalline silicon: microsystems enabled photovoltaics," IEEE Journal of Photovoltaics, DOI: 10.1109/JPHOTOV.2011.2162973 (2011).

This technical article was selected for the debut issue of the IEEE Journal of Photovoltaics.

Ultrathin Flexible Crystalline Silicon: Microsystems-Enabled Photovoltaics

Jose L. Cruz-Campa, Gregory N. Nielson, Paul J. Resnick, Carlos A. Sanchez, Peggy J. Clews, Murat Okandan, Tom Friedmann, and Vipin P. Gupta

***Abstract*—We present an approach to create ultrathin (<20 μm) and highly flexible crystalline silicon sheets on inexpensive substrates. We have demonstrated silicon sheets capable of bending at a radius of curvature as small as 2 mm without damaging the silicon structure. Using microsystem tools, we created a suspended submillimeter honeycomb-segmented silicon structure anchored to the wafer only by small tethers. This structure is created in a standard thickness wafer enabling compatibility with common processing tools. The procedure enables all the high-temperature steps necessary to create a solar cell to be completed while the cells are on the wafer. In the transfer process, the cells attach to an adhesive flexible substrate which, when pulled away from the wafer, breaks the tethers and releases the honeycomb structure. We have previously demonstrated that submillimeter and ultrathin silicon segments can be converted into highly efficient solar cells, achieving efficiencies up to 14.9% at a thickness of 14 μm. With this technology, achieving high efficiency (>15%) and highly flexible photovoltaic (PV) modules should be possible.**

***Index Terms*—Crystalline silicon, microsystems-enabled photovoltaics, photovoltaic modules.**

I. Introduction

REDUCING the thickness of crystalline silicon wafers has been a long-term goal in the solar industry. As of 2010, most of the silicon solar cell companies were working with 6-in wafers with thicknesses between 180 and 200 μm. In addition, a significant portion of the crystalline silicon material is lost during sawing. The effective material usage is equivalent to a wafer with a thickness of 310–475 μm depending on the thickness of the saw wire. Aside from the material and cost savings [1], there has been an interest in using thin silicon films due to other positive benefits such as improvements of the spectral response, open-circuit voltage, fill factor, and higher tolerance for radiation in outer space [2].

Although there is a strong cost driver to use thinner wafers, handling wafers thinner than 180 μm is challenging while maintaining adequate yield. Another problem with thin wafers is the need for higher quality passivation. Due to the closer proximity of surfaces to collection points in thin wafers, well-passivated surfaces are crucial for high efficiencies.

Methods used to create thin wafers for solar cells include using detachment planes created from thermomechanical stress [3], hydrogen implantation [4], recrystallization of polysilicon deposited in an SiO_2/Si stack [5], and the creation of a porous layer [6], [7]. In these approaches, large-area wafers of thickness between 20 and 50 μm are created with or without a supporting frame. The method proposed here is different because it allows for all the processing (including high-temperature steps) done on a standard thickness wafer before the thin silicon is released as film. This enables compatibility with current tools and enhances yield. In addition, the segmented structure allows for a very small (2 mm) radius of curvature making it more flexible than other crystalline technologies. We intend to implement the learned concepts presented here with a back-junction cell design with a suspended structure to create a highly flexible thin-film-like high-efficiency solar cell.

Microsystems-enabled photovoltaics (MEPV) is a technique to create solar cells relying on tools and techniques from the microsystems and integrated circuit industry [8]. The use of these tools could improve yield, efficiency, and uniformity of solar cells with a mature and scalable material base and processing know-how. Other groups in university [9] and industry [10], [11] around the world have taken advantage of these techniques to produce small and thin solar cells with high efficiencies. Some groups, like ours, have used silicon-on-insulator (SOI) wafers to create thin solar cells.

In previous efforts [12], our group produced functional ultrathin silicon solar cells. Their size ranged from 250 μm to 10 mm in diameter with a thickness range of 14–20 μm. Fig. 1 shows a scanning electron microscope (SEM) picture of a 1 mm by side, 20-μm-thick, back-contacted crystalline silicon solar cell with interdigitated radial contacts.

Throughout our research, it was seen that one of the most critical parameters for high efficiency in these ultrathin structures is surface passivation. The process on the first generation of cells was only capable of passivating the backside of the cell, leaving the frontside unpassivated. Further processing of the cell after release was needed to create a front passivation layer. After optimization of designs and passivation techniques, we were able to obtain efficiencies as high as 14.9% in thicknesses as thin as 14 μm [13].

Passivating the front of MEPV cells after release is challenging and cannot be done with standard processing tools. Thus,

Manuscript received June 8, 2011; revised July 15, 2011; accepted July 18, 2011. Date of publication August 22, 2011; date of current version October 27, 2011. This work was supported by the Department of Energy Solar Energy Technology Program Seed Fund and by Sandia, a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's NNSA under Contract DE-AC04-94AL85000.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JPHOTOV.2011.2162973

Appendix C: Publications (cont.)

3. Cruz-Campa, J. L., Okandan, M., Resnick, P. J., Clews, P., Pluym, T., Grubbs, R. K., Gupta, V. P., Zubia, D., and Nielson, G. N., "Microsystem enabled photovoltaics: 14.9% efficient 14 μm thick crystalline silicon solar cell," Solar Energy Materials and Solar Cells 95(2), 551-558 (2011).

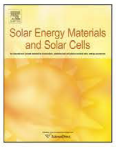
This technical article describes how crystalline silicon generated more than 1% efficiency for each micron used in a microscale 14 μm c-Si PV cell.

Solar Energy Materials & Solar Cells 95 (2011) 551–558

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat



Microsystems enabled photovoltaics: 14.9% efficient 14 μm thick crystalline silicon solar cell

Jose L. Cruz-Campa [a,b,*], Murat Okandan [a], Paul J. Resnick [a], Peggy Clews [a], Tammy Pluym [a], Robert K. Grubbs [a], Vipin P. Gupta [a], David Zubia [b], Gregory N. Nielson [a]

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ARTICLE INFO

Article history:
Received 14 April 2010
Received in revised form
14 September 2010
Accepted 16 September 2010
Available online 25 October 2010

Keywords:
Miniature solar cells
Microsystems enabled photovoltaics
Back contacted solar cells
Ultrathin solar cells
Silicon nitride optimization

ABSTRACT

Crystalline silicon solar cells 10–15 times thinner than traditional commercial c-Si cells with 14.9% efficiency are presented with modeling, fabrication, and testing details. These cells are 14 μm thick, 250 μm wide, and have achieved 14.9% solar conversion efficiency under AM 1.5 spectrum. First, modeling results illustrate the importance of high-quality passivation to achieve high efficiency in thin silicon, back contacted solar cells. Then, the methodology used to fabricate these ultra thin devices by means of established microsystems processing technologies is presented. Finally, the optimization procedure to achieve high efficiency as well as the results of the experiments carried out with alumina and nitride layers as passivation coatings are discussed.

1. Introduction

Reducing the amount of photovoltaic material used in solar cell production is a common goal for the solar cell industry, due to its significant contribution to the overall cost of a photovoltaic (PV) system. Depositing thin films on inexpensive materials, thinning the wafers, or using small cells in combination with concentration optics are approaches taken to minimize the use of the active semiconductor material.

Systems based on silicon wafers are currently the dominant technology of the PV market [1]. Thus, in this paper, we present a wafer compatible fabrication solution that saves up to 30 times the amount of silicon used (including Kerf loss) as compared with current crystalline silicon (c-Si) photovoltaic modules. This paper presents the design, simulation, fabrication, optimization, and testing of sub-millimeter and ultrathin solar cells.

Previous research efforts in the industry and academia have shown interest for creating thin wafers. As a proof of concept, a 47 μm thinned wafer using a passivated emitter with rear locally diffused design (PERL) was able to obtain an efficiency of 21.5%.[2] Since the wafer was thinned, this technique did not save material. Another technique, called direct transfer [3] produced 13.2% efficient solar cell with 40 μm thick wafers. This technique saves material through hydrogen assisted cleaving, releasing only the first thin layer. Other groups [4] proposed a thermo-mechanical process able to release silicon foils with a thickness between 30 and 50 μm in a relatively large area (25 cm^2). Efficiencies around 10% were reported. The disadvantages of such thin wafers are the handling challenges introduced when processing them with standard fabrication tools.

Another approach is using small silicon cells in conjunction with concentration optics to create low profile concentration modules with highly efficient solar cells from standard thickness wafers. In one technique [5], the die are cut with a saw into 2.3×2.3 mm^2. In order to reduce recombination at the sawed edges, they are heavily doped to create an electric field that repels carriers. This technique produced 18.4% efficient cells, with a regular thickness. Currently, the record for silicon cells under concentration is at 27.6% using a small 1 cm^2 back contacted cell under 92 suns [6]. Small silicon cells of standard thickness are currently used by the industry to create low concentration, low profile modules [7].

Other efforts combine using thin substrates and small cells [8]. These efforts report the production of small lateral dimension rectangular silicon cells with efficiencies between 4% and 10%,

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doi:10.1016/j.solmat.2010.09.015

Appendix C: Publications (cont.)

4. Cruz-Campa, J. L., Nielson, G. N., Okandan, M., Wanlass, M. W., Sanchez, C. A., Resnick, P. J., Clews, P. J., Pluym, T., and Gupta, V. P., "Back-contacted and small form factor GaAs solar cell," Proc. 35th IEEE Photovoltaic Specialists Conference (PVSC), 001248-001252 (2010).

To the best of our knowledge, this technical article describes the first practically produced and demonstrated fully backside-contacted GaAs PV cell.

BACK-CONTACTED AND SMALL FORM FACTOR GaAs SOLAR CELL

Cruz-Campa, J. L.[1]; Nielson, G. N.[1]; Okandan, M.[1]; Wanlass, M. W.[2]; Sanchez, C. A.[1];
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ABSTRACT

We present a newly developed microsystem enabled, back-contacted, shade-free GaAs solar cell. Using microsystem tools, we created sturdy 3 µm thick devices with lateral dimensions of 250 µm, 500 µm, 1 mm, and 2 mm. The fabrication procedure and the results of characterization tests are discussed below. The highest efficiency cell had a lateral size of 500 µm and a conversion efficiency of 10%, open circuit voltage of 0.9 V and a current density of 14.9 mA/cm^2 under one-sun illumination.

INTRODUCTION

Silicon solar cells that possess all back contacts have been extensively explored [1,2]. This type of cell has the advantage of all metallization residing on the back of the cell, giving the opportunity to independently optimize the front and back of the cell for optical and electrical performance, respectively [3]. Back-contacted solar cells are ideal for concentration applications and researchers have been able to create 27.5% efficient silicon cells under 100 suns [4]. This technology has been developed for silicon, an indirect bandgap semiconductor, which requires a thick layer of material to absorb the solar spectrum.

GaAs, on the other hand, is a direct bandgap material capable of absorbing 99% of the solar spectrum (above 1.42 eV) in the first few micrometers. GaAs is used extensively as one of the primary junctions for multi-junction photovoltaic (PV) cells for space applications and concentrator modules. Despite the advantages outlined above, GaAs cells with all back contacts have not been widely explored or reported. Some of the impediments to achieving a GaAs back-contacted solar cell are the complex layered structure and the difficulties involved in doping GaAs from external sources.

Microsystems-enabled photovoltaics is an emerging area that allows the application of reliable and precise manufacturing processes used in the microsystem arena to develop high quality, ultrathin, small form factor PV cells [5]. At these small dimensions, the material usage is drastically reduced and carrier collection is improved [6].

Other efforts to reduce the size of the cells have been undertaken by groups in industry [7,8] and academia [9,10], aiming mainly to interface the small scale cells with mini-concentrators. Using our approach, the cells can be used with micro-concentrators in even smaller packages that would be virtually flat.

In this paper, we present the fabrication, characterization, and testing of a newly developed, all back-contacted GaAs single junction solar cell.

CELL FABRICATION

The initial semiconductor stack was grown by metal organic vapor phase epitaxy at the National Renewable Energy Laboratory (NREL). This structure is presented in Figure 1. Absorption

Figure 1. Initial GaAs layer stack for the solar cell provided by NREL.

The design of the photolithographic masks that define the shape, size, and metallization of the wafer was done using AutoCAD 2008. Hexagonal solar cells were designed in 4 different sizes: 2 mm, 1 mm, 500 µm, and 250 µm. Each size had two design variations with different densities of etch release holes. The release holes are perforations that go all the way from the front of the wafer to the release layer so the chemistry can access the release layer. A section of the AutoCAD design for 500 µm cells is shown in Figure 2. Each colored outline in the figure represents a process performed to the stack to achieve a back-contacted solar cell.

978-1-4244-5892-9/10/$26.00 ©2010 IEEE

Appendix C: Publications (cont.)

5. Gupta, V. P., Cruz-Campa, J. L., Okandan, M., and Nielson, G. N., "Microsystems enabled photovoltaics, a path to the widespread harnessing of solar energy," Future Photovoltaics 1(1), 28-36 (2010).

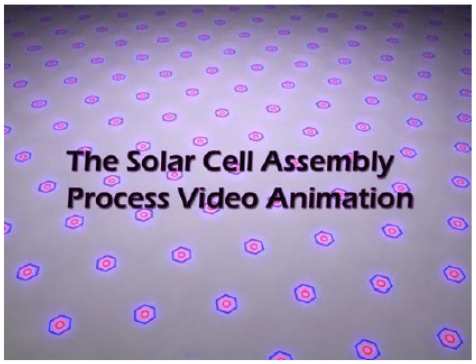
This technical article was selected for the debut issue of the Future Photovoltaics journal.

Microsystems-Enabled Photovoltaics: A Path to the Widespread Harnessing of Solar Energy

Vipin Gupta, Jose Luis Cruz-Campa, Murat Okandan, Gregory N. Nielson
Sandia National Laboratories

Abstract

If solar energy is ever going to become a mainstream power source, the technologies for harnessing sunlight have to become cheaper than all other forms of energy, be easy and quick to install, and work more safely, reliably and durably than present-day grid power. Our research team is striving to make this happen by utilizing microdesign and microfabrication techniques used in the semiconductor, LCD and microsystem industries. In this article, we describe microsystems-enabled photovoltaic (MEPV) concepts that consist of the fabrication of micro-scale crystalline silicon and GaAs solar cells, the release of these cells into a photovoltaic (PV) "ink" solution, and the printing of these cells onto a substrate using fluidic self-assembly approaches. So far, we have produced 10 percent efficient crystalline GaAs cells that are 3 µm thick and 14.9 percent efficient crystalline silicon cells that are 14 µm thick. The



costs associated with this module assembly approach in conjunction with optical concentration can be well below $1/Watt_{peak}$ while retaining the superior conversion efficiency and durability of crystalline silicon and III-V materials.

Our Vision

With the emerging electrification of personal transportation, decentralization of energy generation in places that lack a

Appendix C: Publications (cont.)

6. Lentine, A. L., Nielson, G. N., Okandan, M., Sweatt, W. C., Cruz-Campa, J. L., and Gupta, V. P., "Optimal cell connections for improved shading, reliability, and spectral performance of microsystem enabled photovoltaic (MEPV) modules," Proc. 35th IEEE Photovoltaic Specialists Conference (PVSC), 003048-003054 (2010).

This technical article shows how MEPV cells can be interconnected to generate high voltages (>100 V) in small areas (<1 cm^2) reliably.

OPTIMAL CELL CONNECTIONS FOR IMPROVED SHADING, RELIABILITY, AND SPECTRAL PERFORMANCE OF MICROSYSTEM ENABLED PHOTOVOLTAIC (MEPV) MODULES

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ABSTRACT

Microsystems enabled photovoltaics (MEPV) is a recently developed concept that promises benefits in efficiency, functionality, and cost compared to traditional PV approaches. MEPV modules consist of heterogeneously integrated arrays of ultra-thin (~2 to 20 μm), small (~100 μm to a few millimeters laterally) cells with either one-sun or micro-optics concentration configurations, flexible electrical configurations of individual cells, and potential integration with electronic circuits. Cells may be heterogeneously stacked and separated by dielectric layers to realize multi-junction designs without the constraints of lattice matching or series connections between different cell types. With cell lateral dimensions of a few millimeters or less, a module has tens to hundreds of thousands of cells, in contrast to today's PV modules with less than 100. Hence, MEPV modules can operate at high voltages without module DC to DC converters, reducing resistive losses, improving shading performance, and improving robustness to individual cell failures.

Because these 'multi-junction' cells are integrated heterogeneously versus monolithically, different cell types need not be directly connected in series, improving the efficiency under conditions where different cell outputs are not ideally matched, for example with high incident angles in late afternoon. Instead, different numbers of same cell types are first connected in series, producing an intermediate common voltage, and then these 'micro-strings' of different cell types are connected in parallel. Further series and parallel connections enable module voltages of a few hundred volts in small areas (~ 18 x 20 cm) and allow nearly ideal linear degradation with shading across an installation of multiple modules.

We present details of these cell interconnection designs and performance under spectral and shading variations of the incident solar radiation for MEPV modules designed with heterogeneously stacked cells and single cell designs, and simulations of the relative efficiency of MEPV modules versus the probability of open and shorted cells.

INTRODUCTION

Microsystem enabled photovoltaic (MEPV) modules, comprised of many thin (few μm), small (few hundred μm to few mm, laterally) cells, build on micro-fabrication concepts developed in other technology areas (e. g., MEMS, ICs) to potentially yield modules with higher efficiency, lower cost, and enhanced functionality compared to today's photovoltaic modules [1,2]. One sun and concentrating systems with integrated micro-optical lenses have been proposed. Thin cells have been recently fabricated using epitaxial-lift off in Si and GaAs with efficiencies exceeding 10% [1,2]. Heterogeneously integrating (i.e., vertically stacking) different cell types with dielectric layers between them can yield high performance 'multi-junction cells' with superior performance by freeing the designer of both the lattice matching and series connection constraints of monolithic multi-junction cells. MEPV systems also can offer better thermal management, and new and simpler methods for optical solar tracking, and concepts that allow large scale, low-cost assembly of the cells into modules [2].

Here, we extend the cell connection concepts presented in [3] for conventional PV arrays to electrically connecting the cells within a MEPV module that can achieve improved performance under spectral and shading variations of the incident solar radiation, and show simulated shading performance of PV installations consisting of multiple modules of these types. We will also present simulations of the relative efficiency of an example MEPV module as a function of probabilities of individual cell open and short circuit failures.

CELL CONNECTIONS

It is well known that each cell type under solar radiation will approximately operate at a given known voltage and the cell's current will vary with solar intensity, With MEPV's flexible connections, we can connect different numbers of each cell type in series to arrive at a nearly matched intermediate higher voltage and connect those independent cell micro-strings in parallel effectively adding the currents. Further series and parallel connections enable module voltages greater than a few hundred volts in a small area (~ 18 x 20 cm) and allow nearly linear degradation with shading across an installation of multiple modules. An example MEPV module might be comprised of the cells listed in Table 1.

Cell Type	Eg	Vop	Ser Cells	Ideal V	Par Str	Cells / Grp	Ser Grp	Par Grp
Ge	0.7	0.3	36	10.8	2	72	20	24
Si	1.1	0.57	18	10.26	4	72	20	24
GaAs	1.4	0.9	12	10.8	6	72	20	24
InGaP	1.9	1.3	8	10.4	12	72	20	24

Table 1: Cell types, band gap, and operating voltages for the cells used in the analysis and simulations, and a summary of the cell numbers and connections. The module that was analyzed had 192 x 180 = 34560 cells of each type and operated at 205.2V.

The first step is to pick the intermediate operating voltage for a group of cells, so as to minimize the operating

Appendix C: Publications (cont.)

7. Nielson, G. N., Okandan, M., Resnick, P., Cruz-Campa, J. L., Pluym, T., Clews, P., Steenbergen, E., Gupta, V. P., "Microscale c-Si PV cells for low-cost power," Proc. 34th IEEE Photovoltaics Specialists Conference (PVSC), 001816-001821 (2009).

This was the first technical article produced by our team that showed the performance results from our first batch of fabricated microscale PV cells.

MICROSCALE C-SI (C)PV CELLS FOR LOW-COST POWER

Gregory N. Nielson, Murat Okandan, Paul Resnick, Jose L. Cruz-Campa,
Tammy Pluym, Peggy J. Clews, Elizabeth Steenbergen, Vipin P. Gupta
Sandia National Laboratories

ABSTRACT

We are exploring fabrication and assembly concepts developed for Microsystems/MEMS technology to reduce the cost of solar PV power. These methods have the potential to reduce many system level costs of current PV systems including, among others, silicon material costs, module assembly costs, and installation costs. We have demonstrated a direct c-Si material reduction of approximately 20X (including wire-saw kerf loss and polishing loss). The cells have achieved efficiencies of almost 9% and J_{sc} of 30 mA/cm^2. We are currently using integrated-circuit (IC) fabrication tools that will lead to higher efficiencies and improved yield. These advantages and the material reduction are expected to reduce the current module manufacturing costs.

1. INTRODUCTION

Standard single-crystal or multi-crystalline solar cells consume approximately 380 to 400 microns of material of the ingot (combining wafer thickness, polishing loss, and kerf loss). Thin silicon photovoltaics have advantages over their thick counterparts such as increased spectral response, open circuit voltage (V_{oc}), and fill factor (FF); mainly due to a decreased bulk recombination [1]. Among the approaches found in the literature to create thin crystalline silicon films are: film growth on native substrates [2-3]; film growth on foreign substrates (like glass); and techniques that create a thin film separately from the wafer (which will be the starting material) either by layer transfer or lift-off [4,5].

Thin starting material (<50 µm thick) may be used to reduce the amount of silicon that is required for PV cell fabrication [6]. However, thin semiconductor layers resulting from these techniques require unique fabrication techniques to create the final PV cells. Large areas (>1mm across) of thin silicon are fragile and thus hard to handle and process under normal solar cell procedures.

Two newly developed methods have been demonstrated in which the p-n junction is fabricated before obtaining a thin layer. The first approach is the one used to produce Sliver® cells [7,8]. In this method, the junction is created in 0.5-2 mm thick wafers; the wafer is then processed to form narrow, parallel trenches through the thickness of the wafer, perpendicular to the wafer surface. Once the processing is finished; the Sliver® cells are released from the frame, interconnected, and encapsulated into a module. The second approach creates thin PV cells transferred to a substrate with an elastomeric stamp [9]. The cells are of a long rectangular shape and are processed and defined through lithographic steps. This is followed by a partial under-etch that leaves the cell "anchored" to the wafer. The electrical interconnection is done and finally a stamp adheres to the cells and breaks them free from the wafer. The stamp provides a receiving substrate for the cells. Both approaches lead to cells with thicknesses from 20µm to 50 µm.

By using processes that have been adapted from microelectromechanical systems (MEMS) technologies, we have created 14-20 µm thick layers of c-Si with p-n junctions that function as PV cells (see Fig. 1). Our approach performs as many steps as possible on full thickness wafers, allowing direct use of currently available manufacturing tools. In this scheme doping, diffusion, and metallization steps are performed before separating the devices from the c-Si wafer substrate.

These cells are designed to be very small, on the order of several hundred microns across. This small form factor allows the use of self-assembly methods that use energy minimization concepts for the placement of small die onto a substrate. The benefits of this approach include significant reduction of c-Si usage, the use of inexpensive "roll-to-roll" module manufacturing available to thin-film PV manufacturing, and high-efficiency and high-reliability possible with c-Si PV cells. We will also be able to use concentration to further reduce costs (either low-concentration with non-tracking or high-concentration with tracking).

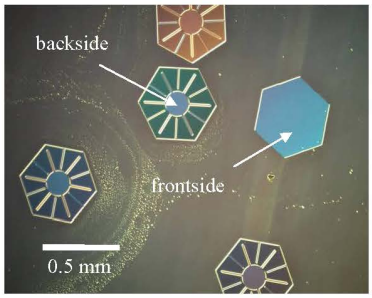

Fig. 1. Optical image of 500 micron wide, 20 micron thick cells.

2. CELL FABRICATION

The process to create arbitrarily thin crystalline silicon PV cells uses standard integrated circuit fabrication techniques combined with MEMS release techniques. The cells are created using standard processing steps followed by a deep etch to define the dimensions of the cells. While we are using lithography, implantation, and reactive ion etching (RIE), laser machining and spin on dopants could

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Appendix C: Publications (cont.)

8. Cruz-Campa, J. L., Zubia, D., Okandan, M., Resnick. P. J., Grubbs, R. K., Clews, P., Pluym, T., Young, R. W., Gupta, V. P., Nielson, G. N., "Thin and small form factor cells: simulated behavior," Proc. 35th IEEE Photovoltaic Specialists Conference (PVSC), 1348-1351 (2010).

9. Sweatt, W. C., Jared, B. H., Nielson, G. N., Okandan, M., Filatov, A., Sinclair, M. B., Cruz-Campa, J. L., and Lentine, A. L., "Micro-optics for high-efficiency optical performance and simplified tracking for concentrated photovoltaics (CPV)," Proc. SPIE 7652, 765210-765217 (2010).

10. Jared, B. H., Gill, D., Sweatt, W. C., Nielson, G. N., Okandan, M., and Filatov, A., "The use of elastic averaging for fabrication of micro-optics in a high-efficiency photovoltaic system," Optical Fabrication and Testing, Optical Society of America Technical Digest, Paper OWC4 (2010).

11. Nielson, G. N., Okandan M., Resnick, P., Cruz-Campa, J. L., "Microscale PV cells for concentrated PV applications," Conference Record of the 24th EU PVSEC 170-173 (2009).

Appendix D: Awards

In recognition for Sandia's Microsystems Enabled Photovoltaics project, Physicist Vipin Gupta receives the 2011 Federal Lab Consortium Mid-Continent Region Award for Excellence in Technology Transfer.

For the conference submission titled "Microfabrication of microsystem-enabled photovoltaic (MEPV) cells," Principal Investigator Greg Nielson receives the 2011 Green Photonics Award from the International Society for Optics and Photonics (SPIE). Out of 292 entrants, SPIE issued eight Green Photonics Awards at the 2011 Photonics West Conference in San Francisco, CA.

Appendix E: Letter of Support From Three Years Ago

ARCH Venture Partners

July 13, 2009

U.S. Department of Energy

Re: Roll-to-Roll Mass Assembly of Ultra-Thin c-Si PV Cells into Lower Cost PV Modules

Dear Distinguished Members of the Merit Review Committee:

On behalf of ARCH Venture Partners, I write in support of the application of Greg Nielson, Murat Okandan, and Vipin Gupta to you. My colleagues and I have reviewed their work at Sandia National Laboratories and have met with them several times over the past 18-months. We met them initially as part of our DOE-EERE-sponsored Entrepreneur-In-Residence effort at Sandia National Laboratories. I was initially skeptical of their work's potential, having looked in some depth at a private company pursuing fluidic self-assembly for semiconductor applications (and ultimately other applications like RFID). I shared my concerns with Greg and Murat and have been impressed that they have been able to address key issues of repeatability, manufacturability, and other practical aspects of the technology that are essential for this approach to work at a commercial scale (something the private company never achieved). Their progress to date has been impressive, and I am optimistic that with some additional funding and focused effort on this, they could prove beyond question the workability of their approach. And I believe that if their approach works at scale, it has the potential to be truly disruptive from a cost perspective. At ARCH, we like platform technologies (that is, technologies that can address multiple applications), and this is definitely a platform technology. In addition to a compelling application in thin, efficient, c-Si PV, this technology will have a number of other interesting commercial applications.

Since we began in the mid-1980s at the University of Chicago, ARCH Venture Partners has helped bring to market over 120 companies formed around the work of leading scientists and academics. We have helped organize and build companies out of the leading academic research universities and national laboratories in the U.S. We now manage over $1.5 billion in capital and operate with offices in Austin, Chicago, San Francisco, and Seattle. In addition, we have an entrepreneur-in-residence at Sandia National Laboratories as well as one at Los Alamos National Laboratory. Our organization consists of 17 investment professionals with backgrounds in physical sciences, information sciences, and life sciences. Our focus is on finding world-class scientific innovations and innovators, and helping to organize and build successful enterprises out of that core scientific work. Our track record is unmatched in this regard. We have significant expertise in semiconductor device technologies, assembly capabilities, and solar technologies. Example portfolio companies include Semprius (UIUC), Innovalight (U Texas), MicroOptical Devices (SNL), Alfalight (U Wisconsin), Surface Logix (Harvard), Amberwave (MIT), Nanosys (Berkeley, Harvard), Nitronex (NC State) and Cambrios (UCSB, MIT). The work of Nielson, Okandan and Gupta shares many of the same important characteristics of these successful companies. These guys are a talented bunch and are the type of scientists we like to follow because they will absolutely produce something interesting.

As a leading national seed and early-stage venture capital firm, we are interested in investing in this technology and its commercial potential, provided it can demonstrate its capabilities. The grant dollars that are subject of this proposal are critical to making that happen.

Sincerely,

Clinton W. Bybee
Managing Director

Appendix F: Letter of Interest Now

The Boeing Company
P.O. Box 3707
Seattle, WA 98124

April 9, 2012
BRT-AKK-12-040512

Vipin Gupta
Principal Member of Technical Staff
Materials, Devices, and Energy Technologies
PO Box 5800, MS-1080
Albuquerque, NM 87185-1080
vpgupta@sandia.gov

Subject: Letter of Interest for Microsystems Enabled Photovoltaics (MEPV)

Dear Dr. Gupta,

The Boeing Company, acting through its Boeing Research & Technology business unit, is interested in your proposal and the Microsystems Enabled Photovoltaics (MEPV) technology your team is developing. In particular, Boeing has interest in solar cells, introducing physical flexibility in the photovoltaic application space, specifically as the photovoltaics find application in transportation or mobile platforms. Present systems still rely on large heavy monolithic structures. The result is that applications to mobile ground units, airborne platforms, and space assets continue to depend on engineering the power to fit the system, rather than logically fitting the power to the application requirements.

The microsystems enabled photovoltaic (MEPV) cells are the only technology capable of bridging this important technical gap. The introduction of microscale photovoltaic cells will enable ground, flight, and space based units to engineer the geometry of their power systems to the constraints of their platform and associated payloads. New technical areas, such as autonomous ground vehicles, long duration fixed wing systems and micro/nano satellites can have their solar power system made into arbitrary shapes, allowing for their incorporation into the platform structure instead of hanging off of it. The microstructure of the cells, along with accompanying micro-wiring, greatly reduces the cost of engineering, packaging and fabrication. In addition, the Sandia team is enabling multi-junction devices, fully optimized across the solar spectrum, so that very high efficiencies will become commonplace.

As a large systems integrator, Boeing functions as a systems developer or as a general contractor, and is responsible for total system-of-systems engineering and integration; development of the core network and architecture; and identification, selection, and procurement of the program's major systems and subsystems. As such we are constantly looking for technologies that will enhance the performance and lower the cost of these systems and the components and subsystems that comprise these systems.

In the event Sandia National Laboratories moves to Phase II in its Microsystems Enabled Photovoltaics (MEPV), and upon your invitation, Boeing would be willing to consider submitting a proposal to you for Boeing's specific support of your effort. Any resulting contractual arrangement will be subject to mutually agreeable terms and conditions within the Microsystems Enabled Photovoltaics (MEPV) program guidelines. In addition, a Proprietary Information Agreement (PIA) is required to be executed prior to any discussions involving either party's proprietary or confidential information; further, ITAR/Export Control requirements will also need to be satisfied.

This Letter of Interest does not constitute a commitment, contract, or agreement, nor does it obligate the parties to perform any actions mentioned herein.

We look forward to hearing from you in the future. Please address technical questions to Dr. Jeffrey H. Hunt at 310-335-6494 or questions of a contractual or business nature to undersigned at (425) 237-5217, email amy.k.kahler@boeing.com.

Sincerely,

Amy K. Kahler
Contracts Manager
Boeing Research & Technology,
Engineering, Operations & Technology
The Boeing Company

Appendix G: MEPV Licensing Information

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

EERE Home | Programs & Offices | Consumer Information

ENERGY INNOVATION PORTAL
Linking Energy Technologies with Market Opportunities

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Glitter™ Photovoltaic Technology

Sandia National Laboratories

GO BACK

Solar Photovoltaic

Technology Marketing Summary

Revolutionary microsolar technology utilizes glitter-sized photovoltaic cells to change how we generate and use solar power. The significantly reduced size and 100 times less silicon used, allows for increased versatility of photovoltaic applications. Traditional solar cells are 6" square wafers which restricts location, performance, and manufacturing. Other unique factors to this technology include solar tracking, self assembly, and power management techniques.

Interested in this technology?
Contact Us ▸

Description

Despite the significantly reduced size, the cells perform comparably to traditional solar cells which can allow for installation in more non-conventional areas such as tents and possibly clothing to recharge small electronics while in the field or outdoor recreation. The glitter-sized cells can also be used on more traditional applications such as roofing.

Glitter Photovoltaic Technology (1,057 KB)

Benefits

- 10 times thinner than conventional solar cells
- More versatility
- Highly efficient microsolar devices
- Lower costs in manufacturing and installation
- Can be fabricated from any size of commercial wafer
- More resilient and reliable

Applications and Industries

- Solar energy generation
- Energy storage
- Battery charging applications
- Satellites
- Remote Sensing
- Integrated solar on unusual, non-traditional items
- Solar energy harvesting

More Information

Multiple patents pending.

Technology ID

SDs: 10496, 10510, 10610, 10631, 10787,10957, 11242, 11288, 11337, 11339, 11345, 11371, 11387, 11451, 11510, 11511, 11515, 11540, 11543, 11600, 11608

Development Stage

Prototype - Sandia estimates the TRL at approximately 3-4. Early laboratory prototypes exist which demonstrate "proof-of-concept" and that the key elements work together.

Availability

Available - Various license and partnering options are available. Please contact the Intellectual Property department to discuss.

Published

06/16/2011

Last Updated

02/14/2012

Availability

Available - Various license and partnering options are available. Please contact the Intellectual Property department to discuss.

Published

06/16/2011

Appendix H: Process Flow for the Creation and Release of c-Si PV Cells Using an SOI Wafer

The microscale design for the radial c-Si PV cell requires five photolithographic masks for the SOI process. The first and second masks define the p- and n-implantation areas, respectively; the third defines the small windows that allow the metal to contact the implanted silicon areas through the silicon nitride passivation layer; the fourth defines the radial interdigitated metal contact pattern; and the fifth defines the lateral size and hexagonal shape of the cell.

The fabrication process is illustrated in Figure A-1 and begins with a six-inch, 20–30 Ω-cm, p-type, (100)-oriented wafer to create the junctions. The device layer is 20-µm thick and the buried oxide layer (BOX) is 1-µm thick.

The first two process steps are the p- and n-type dopant implants. Implantations of boron (energy = 45 keV) and phosphorus (energy = 120 keV) are made with a dose of $3x10^{15}$ cm^{-2}, tilt of 7°, and range of 0.15-µm for both dopants. A dielectric stack is deposited that consists of a 300 nm low pressure chemical vapor deposited (LPCVD) silicon nitride on top of a 500 nm CVD silicon oxide. Then, a photolithographically patterned 1.8-µm thick photoresist layer is used to mask the implantations selectively. A drive-in step is performed for 30 minutes at 900°C in an N_2 atmosphere.

The third process step uses a reactive ion etch (RIE) to open windows in the dielectric stack for the electrical point contacts to the silicon below. Once the windows are opened, the metallization layer is deposited by sputtering. The metallization is a stack of titanium silicide (titanium is deposited and then annealed to react with the silicon), aluminum/silicon, and titanium nitride (52 nm, 720 nm, and 50 nm in thickness, respectively). Titanium silicide reduces contact resistance and provides a barrier to avoid spiking of aluminum through the doped silicon contact. Aluminum/silicon is the main conductor, and titanium nitride serves as protection from the subsequent wet HF release etch. The metal stack is patterned and etched to define the radial interdigitated metal contacts.

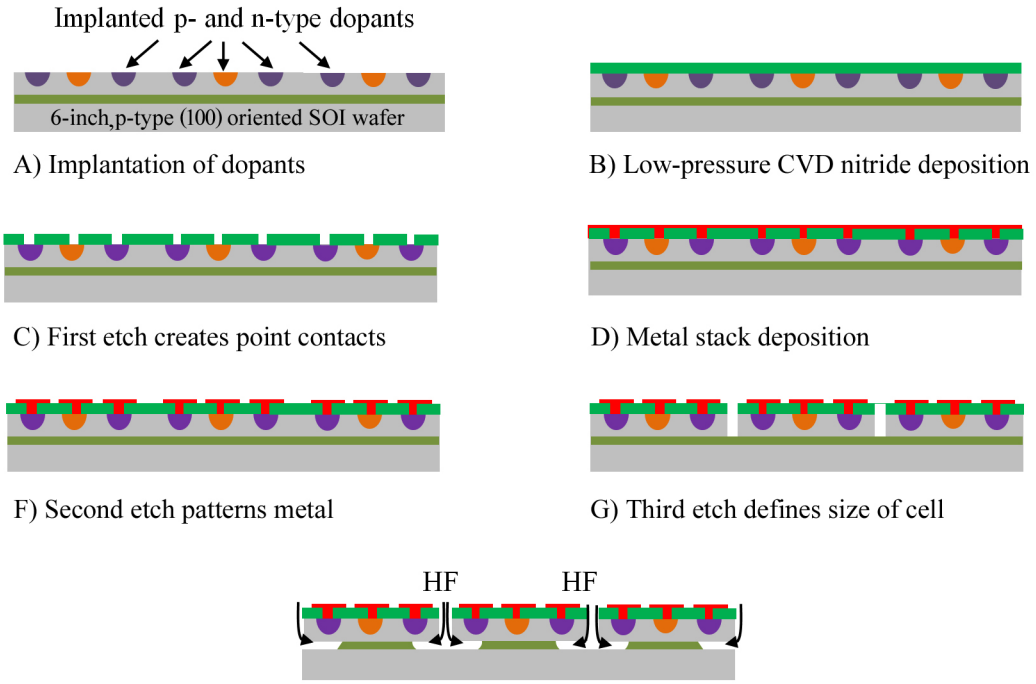


Figure A-1. *Cross section illustration of the process flow for the creation and release of the cell using an SOI wafer. (Source: Sandia)*

The fourth process step is a deep reactive ion etch (DRIE), or "Bosch process," to define the sidewalls of the cells. The etch process, optimized for an etch depth of 20 µm, uses sulfur hexafluoride (SF_6) as the etchant, and a 2.2-µm thick patterned photoresist as a mask. The etch is designed to land on the buried oxide layer without substantial overetch to avoid footing effects.

After metallization and the creation of the 20-µm deep trench, the final release etch is performed. For this step, the wafer is submerged in a 49% HF solution with Tergitol™ (non-ionic surfactant used to wet silicon surfaces). The solution accesses the buried oxide through the trenches and release holes. Depending on the spacing between the trenches and etch release holes, the release can take from 30 to 90 minutes. The substrate is suspended so that the cells fall away from the substrate due to gravity. Finally, the cells are filtered and rinsed with water until the pH is neutral and then transferred to a vial with isopropyl alcohol.

Appendix I: Process Flow for the Creation and Release of c-Si PV Cells Using a (111) Oriented Wafer

The microscale design to fabricate c-Si PV cells with the KOH silicon etchant requires six photolithographic masks. The first mask defines small, circular p-implantation areas, while the second defines the n-implantation areas. The third mask defines the sidewalls of the cell, the fourth the windows for the point contacts from the metal to the implanted areas through the passivation layer, and the fifth the linear interdigitated metal contact pattern. The sixth mask defines the KOH access trenches for the subsequent release.

The fabrication process for the linear contact cells, illustrated in Figure A-2, begins by implanting alternating p- and n-type dopants on a six-inch, 700-µm thick, 3–20 Ω-cm, Czochralski grown, semiconductor grade, p-type, (111)-oriented wafer to create the junctions. Implantations of boron (energy = 45 keV) and phosphorus (energy = 120 keV) are used with a dose of $1x10^{15}$ cm^{-2}, tilt of 7°, and range of 0.15 µm for both dopants. A photolithography-patterned 2.2-µm thick photoresist is used to mask the implantations selectively. A drive-in step is performed for 30 minutes at 900°C in an N_2 atmosphere.

After the junction is completed, a deep reactive ion etch (DRIE) step is performed with a target depth of 20 µm using SF_6 as the etchant and a 2.2-µm thick, photolithography patterned photoresist as a mask. This etch creates trenches that are 1.5-µm wide, which define the sidewalls of the cells. These trenches are filled with a 1-µm thick, conformal silicon nitride (SiN) layer deposited by LPCVD. The objective of this film is twofold: (1) form the wall that protects the cell from the wet chemistry during the KOH release etch, and (2) passivate the sidewalls of the cell.

The next process step is a reactive ion etch of the SiN layer through a 1.8-µm thick patterned photoresist mask. This opens small windows for metal contacts to be made to the doped silicon regions. After the windows are opened, a 200 nm layer of low-stress tungsten is deposited using plasma enhanced chemical vapor deposition (PECVD). The tungsten is subsequently patterned and reactive ion etched to define the interdigitated metallization structure on the cell.

The next step of the process is a second DRIE etch with a targeted depth of 25 µm. This etch uses a 1.8-µm thick layer of photoresist and a 500 nm oxide layer, creating a trench around the periphery of each cell to allow the release etchant access to the sacrificial silicon.

The release of the silicon cells is accomplished by submerging the wafer in a KOH 6M solution held at 85°C for three hours and 45 minutes and then left for 24 hours at room temperature to detach the cells from the wafer. The solution accesses the unprotected silicon through the channels formed during the third etch. Due to the orientation-dependent etch rates, the (111) planes (parallel to the surface of the wafer) are etched very slowly. The SiN walls defined earlier protect the silicon that ultimately becomes the microscale PV cell. The average etch rate selectivity observed between the (111) and other crystal planes was 1:19, making the fabricated cells 13.7-μm thick.

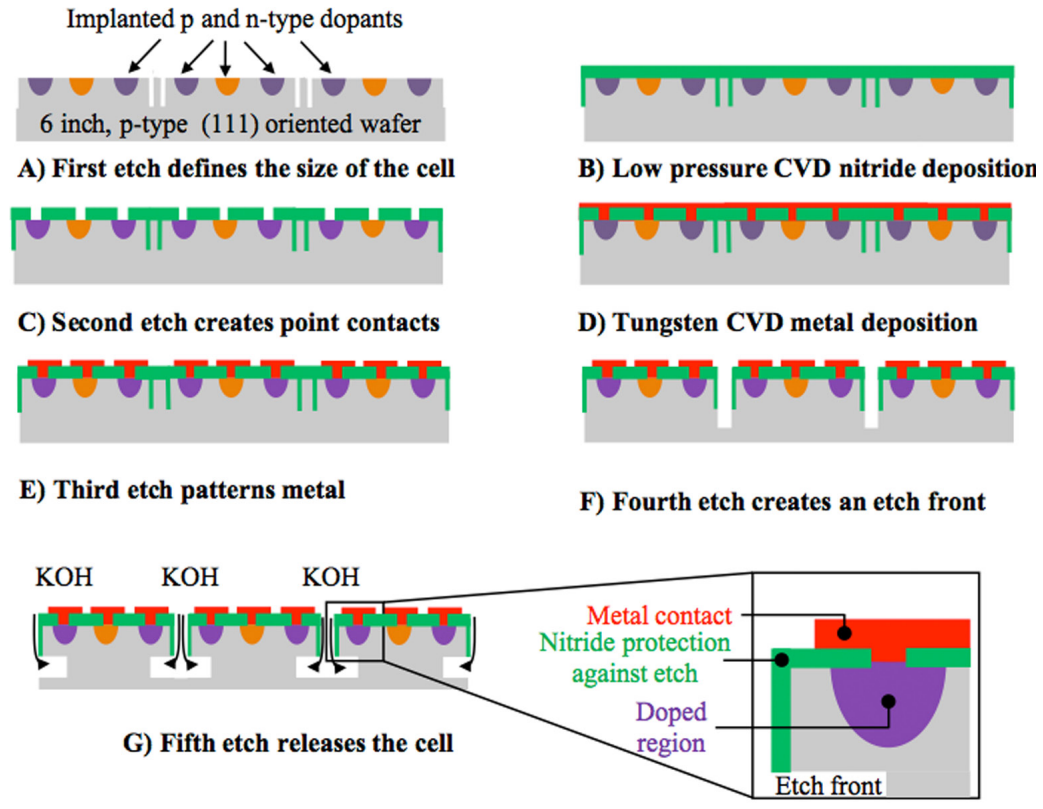
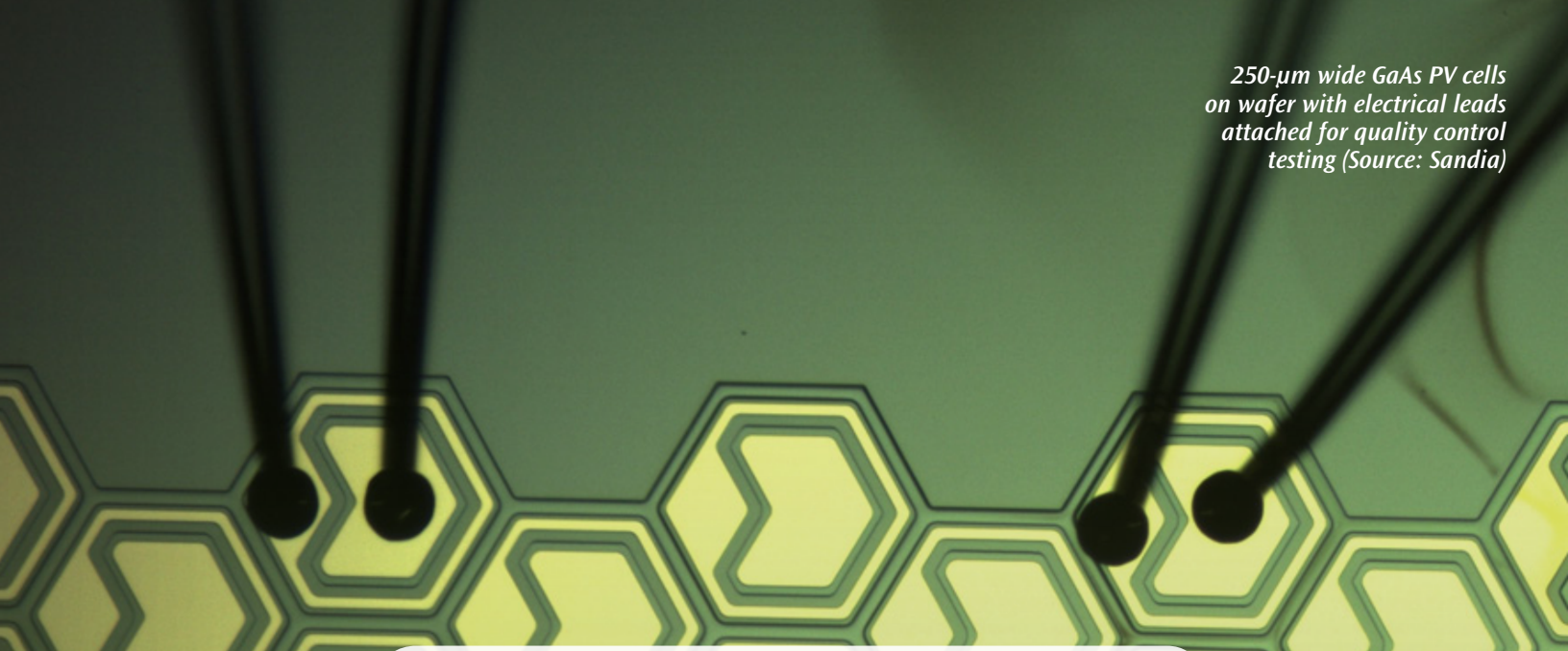


Figure A-2. *Cross section illustration of the process flow for the creation and release of the cells using a (111) oriented wafer. (Source: Sandia)*



250-µm wide GaAs PV cells on wafer with electrical leads attached for quality control testing (Source: Sandia)

O swallows, swallows, poems are not
The point. Finding again the world,
That is the point, where loveliness
Adorns intelligible things
Because the mind's eye lit the sun.

— Howard Nemerov,
The Blue Swallows, 1967

To see the minds behind Sandia's microsystems enabled photovoltaics, watch their short story at: http://mepv.sandia.gov

Sandia National Laboratories

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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