High-Current Linear Transformer Driver Development at Sandia National Laboratories

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(Invited Paper)

***Abstract*—Most of the modern high-current high-voltage pulsed power generators require several stages of pulse conditioning (pulse forming) to convert the multimicrosecond pulses of the Marx generator output to the 40–300-ns pulses required by a number of applications including X-ray radiography, pulsed high-current linear accelerators, Z-pinch, isentropic compression, and inertial fusion energy drivers. This makes the devices large, cumbersome to operate, and expensive. Sandia, in collaboration with a number of other institutions, is developing a new paradigm in pulsed power technology: the linear transformer driver (LTD) technology. This technological approach can provide very compact devices that can deliver very fast high-current and high-voltage pulses. The output pulse rise time and width can be easily tailored to the specific application needs. Trains of a large number of high-current pulses can be produced with variable interpulse separation from nanoseconds to milliseconds. Most importantly, these devices can be rep-rated to frequencies only limited by the capacitor specifications (usually 10 Hz). Their footprint, as compared with current day pulsed power accelerators, is considerably smaller since LTD do not require large oil and deionized water tanks. This makes them ideally suited for applications that require portability. In this paper, we present Sandia National Laboratories' broad spectrum of developmental effort to design construct and extensively validate the LTD pulsed power technology.**

***Index Terms*—Accelerators, high-current devices, linear transformer drivers (LTDs), pulsed power.**

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I. Introduction

SANDIA, in collaboration with the High Current Electronic Institute (HCEI), Tomsk, Russia, is developing new fast high-current high-voltage induction accelerators based on the linear transformer driver (LTD) technology [1], [2]. LTD-based drivers are currently considered for many applications including X-ray radiography, very high current Z-pinch drivers, isentropic compression drivers, and Z-pinch inertial fusion energy (IFE). LTD is a new method for constructing high-current high-voltage induction pulsed accelerators. The salient feature of the approach is switching and inductively adding the pulses at low voltage straight out of the capacitors through low-inductance transfer and soft iron core isolation. The pulse forming capacitors and switches are enclosed inside the accelerating cavity. High currents can be achieved by feeding each cavity core with many capacitors connected in parallel in a circular array. High voltage is obtained by inductively adding the output voltage of many cavities in series. Utilizing the presently available capacitors and switches, we can envision building the next generation of fast radiographic and Z-pinch drivers without large Marx generators and voluminous oil–water tanks, pulse-forming and pulse compression networks as is the case with the present technology drivers. Most importantly, they can be multipulsed with a repetition rate, in principle, up to the capacitor specifications. This makes LTD the driver of choice for IFE where the required repetition rate is estimated to be 0.1 Hz [3]–[5]. Presently, we have in the High Current LTD Laboratory of Sandia a larger 0.5-MA 100-kV LTD cavity in a rep-rated operation, and an even larger 1-MA LTD cavity operating in a single-shot mode at the University of Michigan. In parallel, we are preparing a new LTD laboratory, named MYKONOS, to house our ten 1-MA 100-kV LTD cavities recently constructed and received from the HCEI, Tomsk, Russia. The cavities are stackable and will be assembled in a 1-MV 1-MA voltage adder configuration enclosing deionized water as an insulator. This will be the first induction voltage adder constructed and operated with a water-filled coaxial transmission line. In this experimental work, we aim to test the advantages of water insulation as compared to self-magnetic insulated transmission line (MITL) transport. It is hoped that the vacuum sheath electron current losses will be avoided without any new difficulties caused by the deionized water. Special care has been taken to eliminate air bubbles in the voltage adder. In the following sections, we present our already built and operated high-current fast LTD cavities and voltage adders, we briefly describe the basic circuit theory underlying the LTD operation, and we give results of the experiments done with individual cavities and LTD voltage adders.

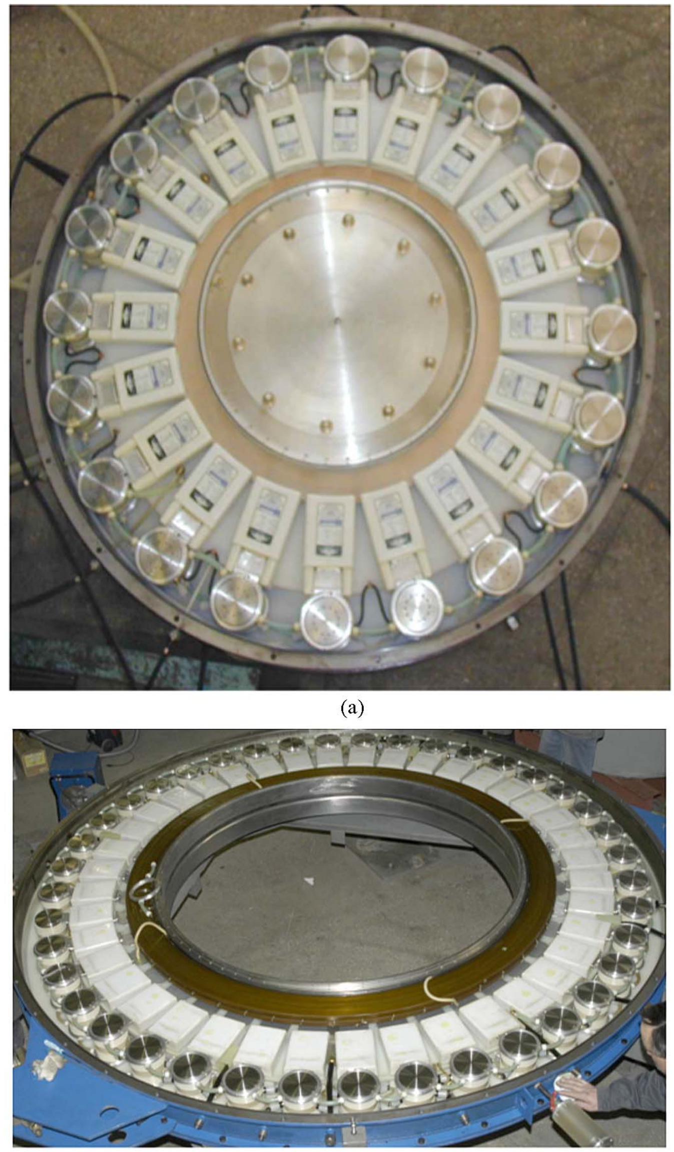
In Section II, we describe the first two types of LTD cavities constructed and operated. In Section III, we describe the basic circuit theory underlying the LTD operation. In Section IV, we present experimental results with individual cavities. Section V describes the experimental work done with a five-1-MA cavity voltage adder. Finally, in Section VI, we summarize our up-to-date LTD developmental progress, give the status of the new 1-MV 1-MA MYKONOS laboratory and present future plans.

II. Fast 70–100-ns LTD Cavities

An LTD cavity is basically an induction accelerator cavity that encloses the entire pulse-forming network that generates the output pulse. This pulse is applied across the insulator that separates the anode and cathode output electrodes (A–K gap) of the cavity. The LTD cavities studied here are flattened doughnut shape with the axial A–K gap at the center of the inside cylindrical surface. At all times, the walls of the cavities are at ground potential. In Fig. 1, two different size LTD cavities are presented with the top metal cover and plastic insulator that insulates the charged parts from the cavity top wall removed.

The cavity of Fig. 1(a) can deliver a 0.5-MA 100-kV pulse to a matched 0.2-Ω load. It contains two circular arrays of 40-nF 25-nH single-ended capacitors. In Fig. 1, only the top array is shown. The bottom array is separated from the top by a $\sim$1-cm plastic insulator plate. The top capacitors can be charged up to $+100$-kV maximum charge and the bottom ones up to -100 kV. Each pair of negatively and positively charged capacitors is connected in series with a separate switch positioned vertically and capable of holding 200-kV potential difference. This basic unit, "brick," composed of two capacitors and one switch connected in series, defines the rise time, current, and period of the cavity output pulse. The capacitors and switches are the only two active elements, which are repeated many times in a cavity interior depending on the required output current pulse amplitude. In Fig. 1(a), the cavity is fitted with a liquid resistive load enclosed in two concentric plastic cylinders located in the central hole of the cavity toroid. In testing the cavities, we utilized KBr water solutions. Fig. 2 shows the side section of an LTD cavity where the load is now the coaxial line formed by the inner cylindrical surface of the cavity (anode) and the central (cathode) cylindrical electrode. This is how the cavities are configured in a voltage adder assembly.

In order to achieve fast 70–100-ns rise-time output pulses, the capacitance and inductance of the brick must be kept as low as possible. However, the inductance budget of a brick is not as tight since a large number of bricks are connected in parallel to the output high-voltage terminals. The brick capacitance is more rise time defining. Hence, in addition to keeping the inductance as low as possible, smaller capacitance capacitors in a brick can provide faster rise times. Unfortunately, the output peak current then becomes smaller. The 0.5- and 1-MA cavities [Fig. 1(a) and (b)] contain 40-nF capacitors. The switches are pressurized with dry air. Depending on the capacitor charging voltage, the switch operating pressure can vary between a few atmospheres and up to 6 atm. The air following each shot is removed fast by connecting the switch chambers with a large vacuum chamber that is continuously pumped down to



(a)

(b)

Fig. 1. Two types of LTD cavities constructed and extensively tested.

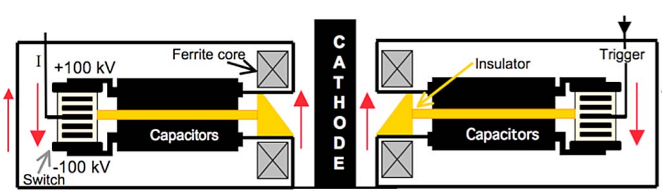


Fig. 2. Side section of an LTD cavity as configured in a voltage adder.

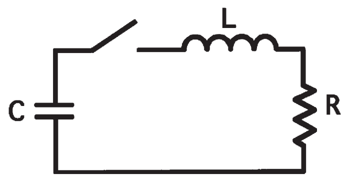


Fig. 3. LTD simplified circuit. The resistance R is the sum of the load and internal circuit impedance. This circuit neglects the core losses.

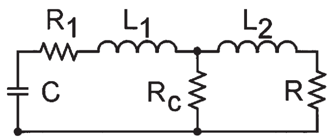


Fig. 4. LTD II equivalent circuit including core losses.

a 10-torr pressure. This turbulent flow prevents the products of air breaking down from leaving deposits on the plastic inside surface of the cylindrical switch wall during the arcing and conducting stage of the switch.

We have developed a repetition system that can recycle the switches very fast [6], [7]. The limiting factor in our up-to-date experiments was not the switches but the capacitor charging power supply software. With a faster communicating power supply with our LabVIEW [8] program, we could have exceeded the 0.1-Hz repetition rate required for the IFE driver. Both constructed cavities have the same axial length of $\sim$22 cm. The 1-MA cavity is the largest (3 m in diameter), while the two 0.5-MA LTD I and LTD II cavities have a smaller diameter and approximately equal to 2 m. Cavities LTD I and LTD II have 20 bricks. The 1-MA cavity contains 40 bricks. Each brick provides a maximum of approximately 25-kA current to a matched load.

III. LTD Principle and Its Equivalent Circuit

Fig. 3 shows the equivalent simplified circuit of an LTD cavity neglecting the core losses, which in a very finely laminated Metglass core are practically equal to zero. It contains a switch, a capacitor C, an inductance L, and a resistance R. We assume that the switch represents all the parallel-connected switches of the cavity; the capacitor is equal to the sum of the capacitance of all the capacitors; the inductance is equal to the total inductance including that of the switches, capacitors, and load; and finally, the resistance R includes the load plus the internal resistance of the cavity. A more realistic equivalent circuit usually considered in numerical simulations is shown in Fig. 4, where the resistance (R_1) and inductance (L_1) of the LTD cavity are separately included from the respective parameters L_2 and R of the load. In addition, and this is the main and important difference from the circuit of Fig. 3, the core losses due to induced Eddy currents are included in the form of a parallel resistor to the load R_{c}.

The second-order differential equation that governs the circuit behavior of Fig. 3 is that of the typical damped oscillation which is given by the familiar expression of

$$L\,di^2/dt^2 + R\,di/dt + i/C = 0. \tag{1}$$

This equation can be solved analytically, and, in its general form, the solution has a rather complicated trigonometric expression for the load voltage, current, power, and energy as a function of time [2]. Numerical solutions are necessary to simplify these expressions. Specifically, the load resistance that maximizes the circuit power output has been estimated numerically for both the circuit of Figs. 3 and 4 in [9] and [10], respectively. For example, the numerical solution of the load resistance R_{load} which optimizes the output power in the circuit of Fig. 3 is estimated approximately as $R_{\mathrm{load}} = 1.10\sqrt{L/C} + 0.80R_{\mathrm{cav}}$ in [9]. Here, R_{cav} is only the internal resistance of the cavity which in most cases is very small. However, there are two special cases where the solution has simple forms: when the total resistance of the circuit of Fig. 3 is $R = \sqrt{L/C}$ and when $R = 2\sqrt{L/C}$. The first is the "matched" case where the load resistance is equal to the characteristic impedance of the circuit, and the second is the critically matched case where the solution does not exhibit any oscillation. In the matched case, the time to peak current and voltage and the values at that particular time of the voltage, current, and energy transferred to the load are given by the following expressions:

$$t_{\mathrm{peak}} = \frac{2\pi}{\sqrt{3^3}}\sqrt{LC} \equiv 1.21\sqrt{LC} \tag{2}$$

$$i_{\mathrm{peak}} = \frac{2V_0}{\sqrt{3}R}e^{-\frac{\pi}{3\sqrt{3}}}\sin(\pi/3) = 0.546293\frac{V_0}{R} \tag{3}$$

$$V_{\mathrm{peak}} = Ri_{\mathrm{peak}} = 0.546293V_0 \tag{4}$$

$$E(t_{\mathrm{peak}}) = 0.4031279. \tag{5}$$

In the critically matched case, the peak current is smaller by 33% and the energy transferred to the load at peak time by 20%. However, the rise time is shorter and the peak voltage higher

$$t_{\mathrm{peak}} = \sqrt{LC} \tag{6}$$

$$V_{\mathrm{peak}} = 0.73576V_0. \tag{7}$$

From the aforementioned arguments and expressions, it is obvious that for certain applications like radiographic machines where X-ray output is proportional to a higher than quadratic exponent of the electron beam voltage, and where the output current requirements are relatively modest, the critically $(R = 2\sqrt{L/C})$ or higher overmatched load conditions are the choice. Indeed, the first radiographic LTD machine currently in operation in Sandia is critically matched to the radiographic diode load [11]. On the other hand, for Z-pinch drivers where large current and efficient energy transfer to the load at peak current are of paramount importance, simply matched loads of $\sqrt{L/C}$ should be the configuration of choice. However, recent current scaling experiments with the Z accelerator [12] demonstrated that faster current rise time driven pinches, and shorter implosion times (although with lower peak load current) yielded higher X-ray radiated power. Therefore, it is not inconceivable even for large Z-pinch drivers to select a critically matched design which provides faster load current rise times despite the lower peak current.

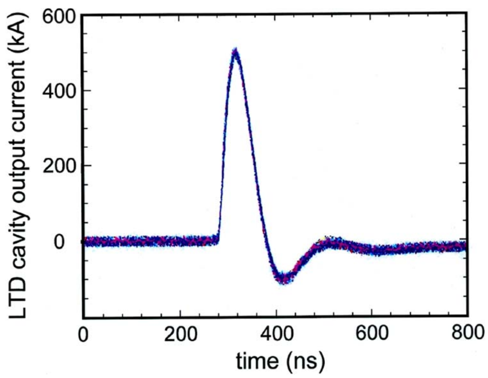


Fig. 5. Overlay of 200 consecutive shots obtained with LTD I.

IV. Experiments With Individual LTD Cavities

A. LTD I and LTD II ~0.5-MA Cavities Performance

The prototype cavity, LTD I, was the first high-current LTD cavity device ever built, and it had a specific problem. The peripheral cylindrical walls [Fig. 1(a)] were too close to the switch high-voltage terminals. This prevented us from charging the capacitors to ± 100 kV. Therefore, the first set of experiments reported here was performed at maximum charging voltage of $\sim\pm 85$ kV. In fact, these tests uncovered this minor defect, which was corrected in the newer cavity model LTD II. For the second experimental campaign, we obtained the new improved version, LTD II cavity, where the diameter of the cylindrical wall was 5 cm larger.

The LTD I cavity was constructed at the HCEI, Tomsk, Russia, as a single-shot device. It was delivered to Sandia and installed at the High Current LTD laboratory. Following single-shot testing, all the support systems such as capacitor charging, switch pressurization, switch vacuum purging, premagnetization of the ferromagnetic cores, and triggering systems were modified and made repetition rate capable [6], [7]. A "LabVIEW" [8]-based software program was written to automatically control the aforementioned operations including the data acquisition system. We can preset the number of pulses required for every experimental campaign and the interpulse separation, press the computer key, and let the system go on firing and collecting data. In the presently reported experiments, the cavity output load was a liquid resistor installed at the center of the cavity [Fig. 1(a)].

The research results with the prototype LTD I cavity are summarized as follows: 1) We fired 13 000 shots at rep-rate higher than five shots per minute without experiencing any component overheating or problems with the switches, the capacitors, and supporting automated systems. It is interesting to note that the output voltage and current pulses are extremely reproducible as witnessed by a 200 shots overlay (Fig. 5). Parallel with this study, a small circuit set-up composed of one switch and two capacitors connected in series (brick) (similar to one of the 20 parallel circuits enclosed in the LTD cavity) was fired for 37 000 times with a repetition rate of three shots per minute with no switch or capacitor failure. This later study was done in Tomsk HCEI under Sandia contract. It is obvious that the LTD technology is very reliable and is a good candidate for the next generation of large Z-pinch drivers where hundreds of thousands of LTD switches will be utilized and for the IFE driver [3]–[5] where a very large number of shots will be required. 2) The measured cavity output jitter was quite small. During the 13 000 shots, we observed a jitter better than 2 ns ($1\ \sigma$), which is much better than the one of the conventional pulsed power devices. 3) We came very close to the IFE required repetition rate. Towards the end of this campaign, we were able to fire every 10.3 s, which is equivalent to 0.097 Hz. Installation of a higher current charging power supply could increase the firing frequency up to 0.12 Hz. 4) The pulse-to-pulse reproducibility as witnessed from Fig. 5 is excellent with variation better than 1% ($1\ \sigma$). 5) Finally, we are happy to report that during the 13 000 shots following the evaluation of the switch optimum operating pressure not one switch prefire was recorded.

The number of shots we fired was, of course, arbitrary, but large enough to establish the reliability of the device. In the case of an IFE power plant where a large number of shots will be required (six shots per minute firing around the clock for years), 13 000 or 37 000 shots may not be enough to establish certification and validate operation of the device. However, for an Inertial Confinement Fusion driver like Z where we fire only once a day, 13 000 shots are more than enough to certify an LTD device.

Fig. 6 shows the comparison of a sample of the cavity output current traces with the results of the SCREAMER [13] circuit code calculations. The experimental results are in very good agreement with the simulations.

The experimental campaign with the LTD II cavity had somewhat different goals. In addition to firing a large number of shots for component longevity verification, the cavity performance for different switch pressures was studied. Namely, the switch pressure was varied from 53 psia ($= 366$ kPa) to 67 psi ($= 463$ kPa) in steps of 2 psia (~ 14 kPa). For each pressure setting, 1000 shots were fired at ± 100-kV charging. In order to avoid large temperature variations of the liquid load resistor, the shots were taken at the moderate repetition rate of three shots per minute. Fig. 7 shows the comparison of a typical output voltage trace, at ± 100-kV charging, with Pspice [14] circuit code calculations. The circuit utilized here (Fig. 4) was more realistic than the simple LRC circuit used for the SCREAMER simulations of Fig. 6. It included the core losses and the inductance of the load. Both traces are close to overlapping.

For the LTD II experimental campaign, the LabVIEW software was substantially upgraded. For every shot, the following voltage pulse output parameters were recorded and statistically analyzed: switch closure time (the time interval between the arrival of the trigger pulse on the switches and the start of the output pulse), switch closure jitter, voltage pulse rise time, output voltage shape, fall time, FWHM, and amplitude; similar parameters were recorded for the output current pulses. As the switch pressure increased above 65 psia ($= 450$ kPa), the trigger jitter, pulse rise time, FWHM, and standard deviations increased. Our data suggest that the switches perform equally well in the 360–450-kPa pressure range studied for a ± 100-kV charging operation. At this pressure range, the pulse rise and fall

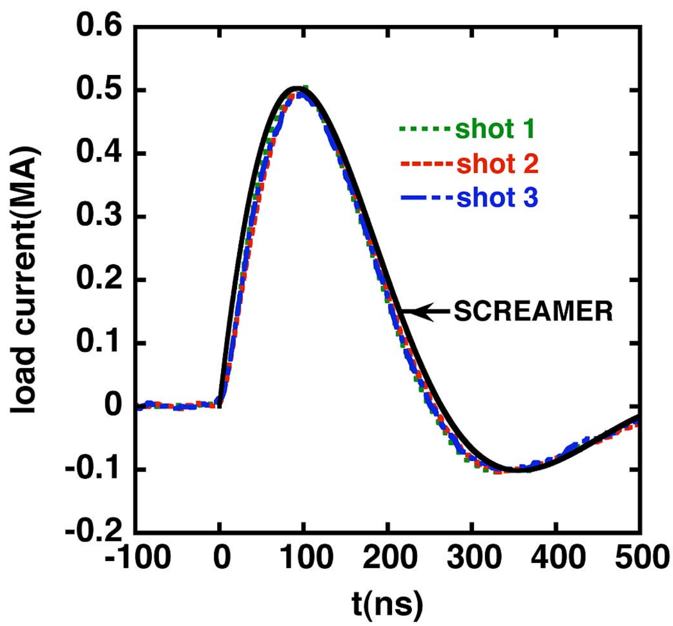


Fig. 6. LTD I. Overlay of three current traces with the SCREAMER simulation result.

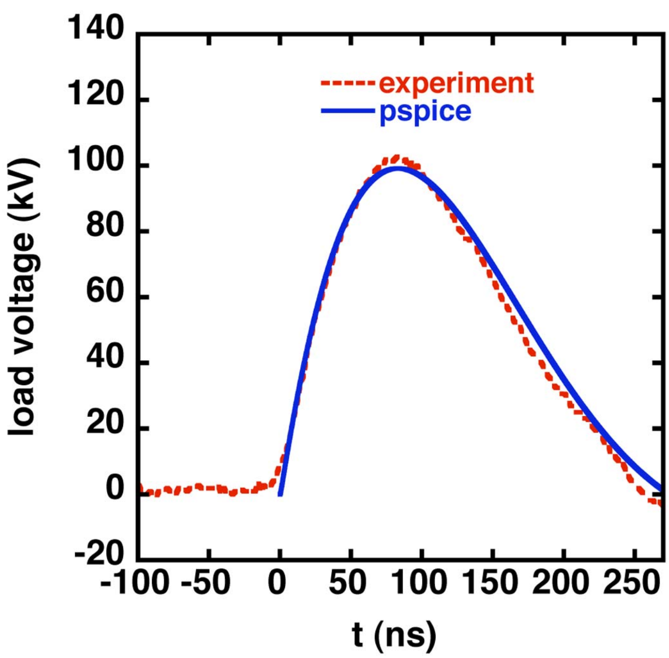


Fig. 7. LTD II load voltage trace compared with Pspice simulation.

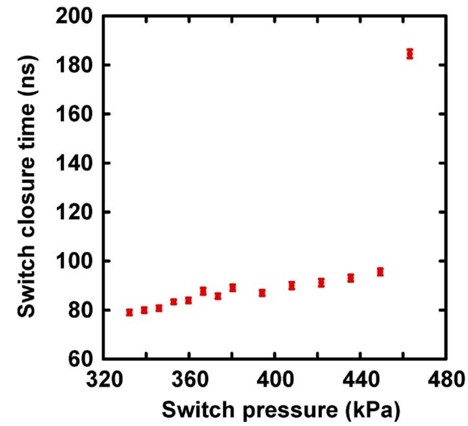


Fig. 8. Switch closure time (the time interval between the arrival of the trigger pulse on the switches and the start of the output pulse) as a function of the switch pressure. The error bars are almost invisible in the scale of the graph.

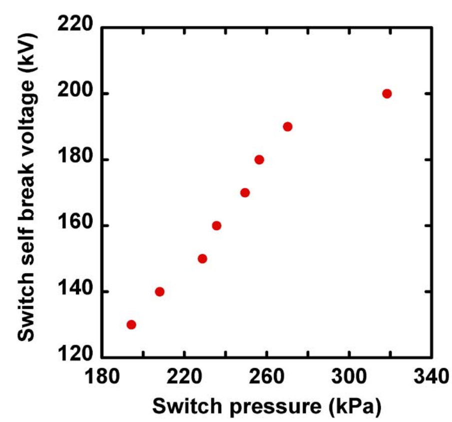


Fig. 9. Self-break curve of the 20 LTD cavity switches.

TABLE I
SUMMARY OF LTD II RESULTS

Switch closure time	80-100 ns
Switch closure jitter	1.2±0.2 ns
Pulse rise time (10%-90%)	55.5±1.4 ns
Pulse fall time (90%-10%)	124±1.4 ns
FWHM	132±2.5 ns
Pulse amplitude	98.08±0.02 kV
Number of pre-fires	0.0

times, FWHM, trigger jitter, and amplitude standard deviations were approximately the same with a very slight increase going from lower to higher pressures. However, the switch closure times (Fig. 8) increased from lower to higher pressures by approximately 10 ns. Following conditioning of the switches at the beginning of the experimentation with approximately 500 shots, no prefires were observed in the entire pressure range studied. The LTD II cavity performed equally well to the prototype cavity. At ±100-kV charging, following switch conditioning, no prefires were observed in the experimentation range of 367–463 kPa. It is interesting to note that although the studied pressure range varied from 5% to 32% above the self break pressure for a 200-kV voltage across the switches (Fig. 9), the output pulse characteristics remained practically unchanged.

A switch research program is currently underway in Sandia National Laboratories (SNL) to develop and evaluate alternative fast LTD switches. Table I summarizes the performance of LTD II cavity [15].

B. 1-MA LTD Cavity Performance

From the first tests with resistive load, the 1-MA cavity performed as expected. Fig. 10 shows the results of the first built 1-MA cavity operating with a matched resistive load of 0.1 Ω. It is impressive to note that just one LTD cavity can deliver to the load 0.1-TW power. For the experimental tests of

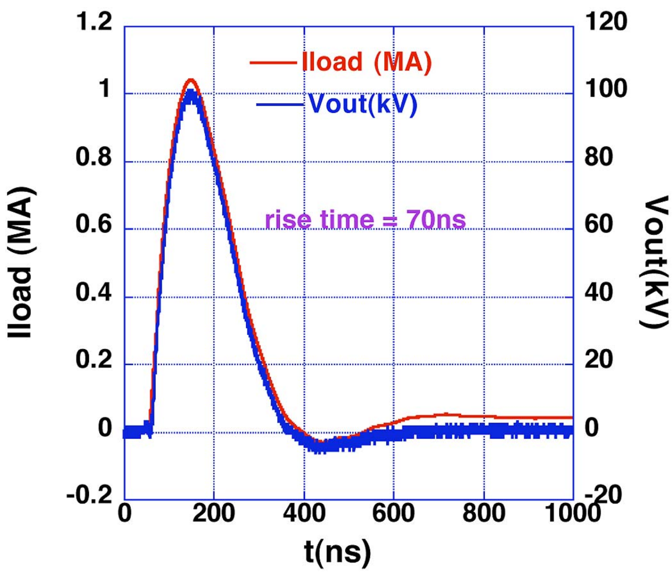


Fig. 10. Current and voltage traces of the 1-MA LTD cavity.

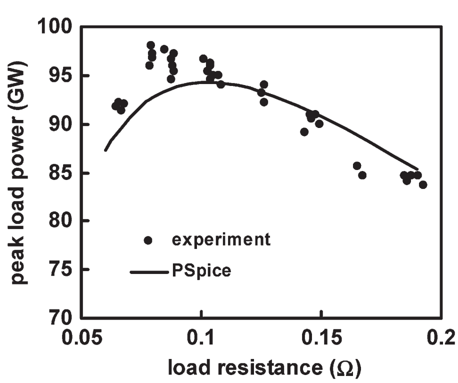


Fig. 11. One-megaampere LTD. Peak load power dependence on the load resistance.

each individual 1-MA LTD cavity, the resistive load was placed inside the cylindrical opening of the stage in a similar way as for the LTD I and LTD II cavities.

Experiments were conducted with different resistive loads at $\pm$100-kV charging. Fig. 11 shows that the optimum output cavity impedance [10], which maximizes the output power to $\sim$96 GW, is $R \sim 0.1\ \Omega$. In this case, the load voltage is $\sim$100 kV (Fig. 12) (and the power rise time (0% to 100%) is $\sim$90 ns (Fig. 13).

The simulation is in a reasonable agreement with experimental results. Assuming that all switches close simultaneously and the cores do not saturate, the discharge of an LTD stage can be represented by an equivalent RLC circuit (Fig. 4). Here, C is the total storage capacitance of all the bricks connected in parallel; R_1 is the resistance of the capacitors and the switches, and L_1 is the total inductance of the bricks. R_C is the resistance of the core which simulates the core loses, and L_2 and R are the inductance and the resistance of the load.

The best fits of the experimental data with the Pspice code simulations were obtained using this circuit with $U_{\mathrm{CH}} = 200$ kV, $C = 800$ nF, $R_1 = 0.0165\ \Omega$, $R_C = 0.65\ \Omega$, $L_1 = 6$ nH, and $L_2 = 1.05$ nH.

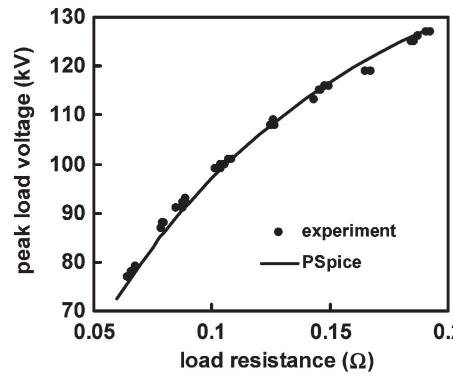


Fig. 12. Peak load voltage dependence on the load resistance. The dots are the experimental results while the solid curve is the Pspice simulation.

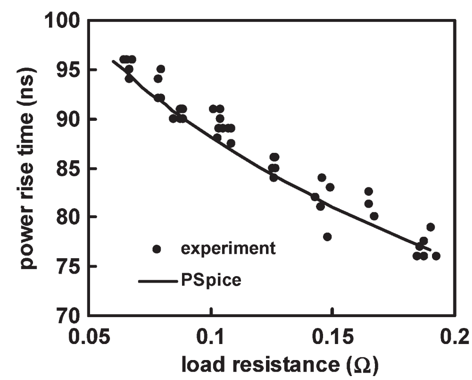


Fig. 13. Power rise time dependence on the load resistance. The experimental data points are compared with (solid curve) the Pspice numerical simulation.

Fig. 14 shows results of the 1-MA cavity recently installed at the University of Michigan LTD laboratory named MAIZE. The Michigan cavity was also constructed at the HCEI and is the first 1-MA cavity to be installed and set into operation in the U.S. As Fig. 14 shows, this cavity performs equally well as the ones tested previously at the HCEI in Tomsk. The output current traces through a resistive load are in very good agreement with numerical simulations.

V. Five-Cavity 1-MA LTD Voltage Adder Experiment

Five 1-MA LTD cavities were assembled in series into a voltage adder and tested with electron beam diode (e-beam diode) and resistive loads (Figs. 15 and 16) [10]. Because of the short transit time to the load in both experiments, the cavities were triggered simultaneously. Here, we present only the results with the electron beam diode load (Fig. 15).

The voltage reached the maximum value of $\sim$400 kV at $\sim$100 ns. At the same time, the current peaked at $\sim$800 kA, while the electron beam power became $\sim$320 GW. Since all the cavities were triggered simultaneously, the Pspice model included the inductance (18 nH) of the voltage adder coaxial line. Hence, the output voltage was limited to $\sim$400 kV. The utilized Pspice equivalent circuit was composed of five RLC

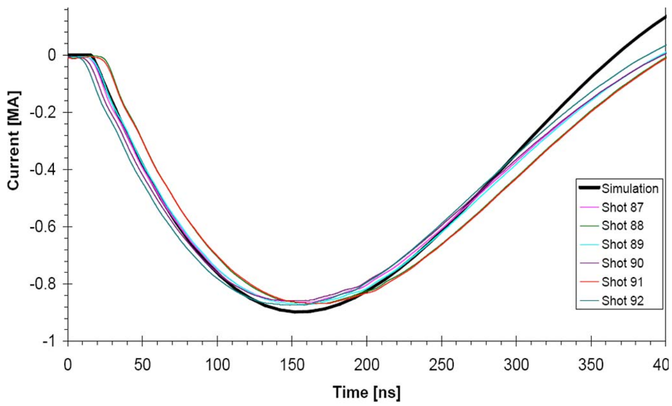


Fig. 14. Current traces of the 1-MA cavity of the University of Michigan. The black trace is simulation.

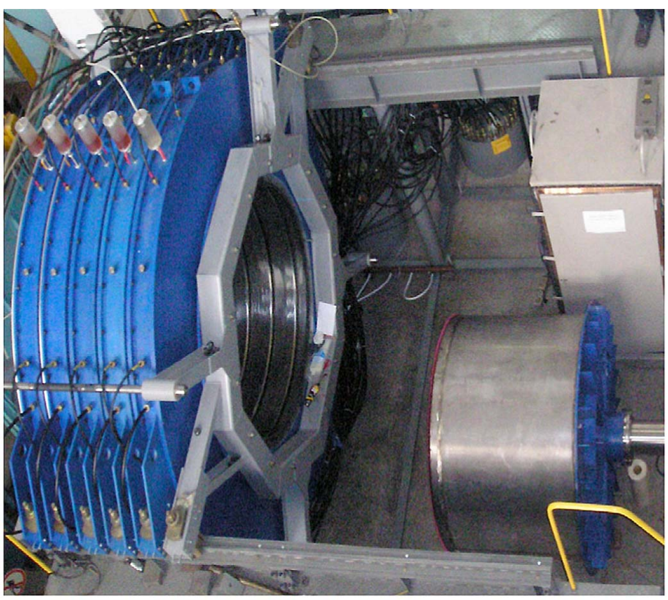


Fig. 15. View of the 1-MA five LTD cavity voltage adder with the cathode electrode near by.

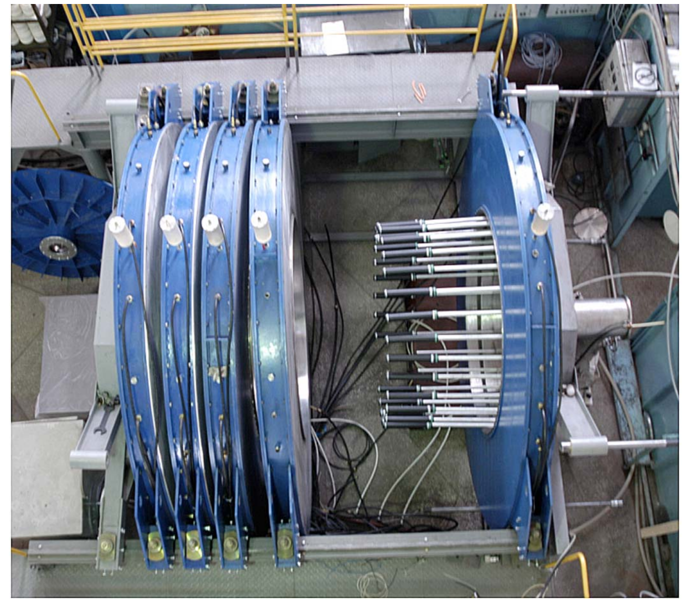


Fig. 16. Five 1-MA LTD voltage adder. The reentrant resistive load is shown out of the cavity.

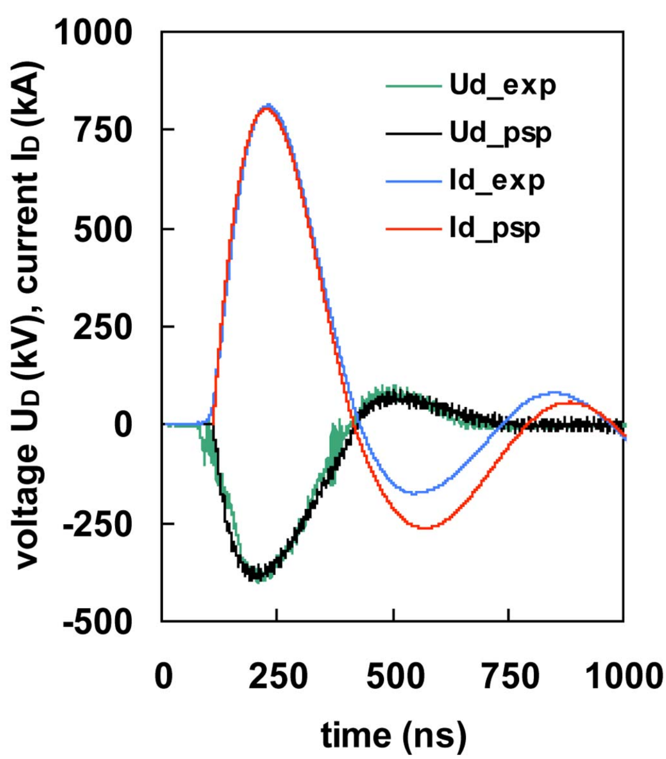


Fig. 17. Five 1-MA LTD cavity voltage adder results compared with numerical simulations. The diode voltage for clarity is inverted. The simulations were done for $U_{\mathrm{CH}} \pm 90$ kV.

circuits connected in series to the diode load through the 18-nH inductance of the voltage adder output line. The radial anode–cathode gap around the cathode stalk was 6.3 cm. The peak electric field was $\sim$65 kV/cm, which was below the vacuum emission threshold of $\sim$200 kV/cm. Therefore, the coaxial output vacuum line formed by the five-cavity LTD voltage adder and the central cathode stalk was designed to operate in the vacuum insulated regime and not in an MITL regime.

Fig. 17 shows the diode voltage U_D (in green) and current I_D (in blue) traces for an LTD cavity charge $U_{\mathrm{CH}} = \pm 90$ kV and a diode A–K gap of 1.4 cm. In black and red are the diode voltage and current traces simulated with Pspice for the same charging and diode parameters.

The five-cavity voltage adder was operated at charge voltage between ± 80 to ± 90 kV and for a number of A–K gap settings varying from 1.0 to 1.7 cm. During the resistive load experiments, we fired a total of 500 shots; 300 of them were at ± 100-kV charging.

VI. Summary and Future Plans

An extensive evaluation of the LTD technology is being performed at SNL, the HCEI, Tomsk, Russia, and the University of Michigan. Two types of High Current LTD cavities (LTD I–II, and 1-MA LTD) were constructed and tested individually and in a voltage adder configuration (1-MA cavity only). All cavities

Fig. 18. MYKONOS 1-MV 1-MA laboratory at construction in Sandia. (Blue color) The rails where the ten 1-MA LTD cavities will be suspended are installed.

performed remarkably well and the experimental results are in full agreement with analytical and numerical calculation predictions.

A large number of shots for each one of them have been logged without any component deterioration or failure. The prototype LTD I cavity was operated only up to ±85-kV charging and delivered to a matched load up to 0.45-MA current. Thirteen thousand shots were logged in with neither prefires nor any active component failure. The pulse output shape and amplitude reproducibility were excellent (Fig. 5) with amplitude variation less than 1% (1 σ). The jitter was as small as 2 ns. The achieved repetition frequency was 0.097 Hz, which is quite close to the 0.1 Hz required for IFE applications [3]–[5], [16]. The LTD II cavity performed equally well. The output current and voltage to a matched load were 0.5 MA and 100 kV, respectively. The gas switch pressure was varied, and the optimum operating pressure range where the output pulse has the fastest rise time and narrower FWHM was established.

The impressive performance of the 0.5-MA LTD cavities encouraged us to proceed with the construction of the larger 1-MA cavities. We have built in Tomsk 11 1-MA cavities. Ten of them are presently in SNL, and the 11th one is in operation at the University of Michigan. These larger 1-MA cavities were extensively tested individually and in voltage adder configurations with both resistive and vacuum electron diode loads. Their output pulse characteristics at 1-MA peak current duplicated those of the smaller 0.5-MA models. In the voltage adder experiments, we demonstrated voltage addition full-power transmission with no current losses or vacuum insulators tracking. A Pspice circuit model was constructed for the five-cavity voltage adder tested including core losses and vacuum electron diode behavior. The simulations are in very good agreement with the results.

The performance of the 1-MA LTD cavities have convinced us that they could be good candidates for constructing future high-current high-voltage accelerators possibly for Z-pinch and IFE drivers and as high-intensity X-ray radiographic sources. Experiments with a 1-TW module, which includes ten 1-MA LTD cavities connected in series, are in preparation at MYKONOS LTD Laboratory, SNL, Albuquerque (Fig. 18).

This MYKONOS voltage adder will be the first ever IVA built with a transmission line insulated with deionized water. The LTD II cavity renamed LTD III will serve as a test bed for evaluating a number of different types of switches, resistors, alternative capacitor configurations, lossy cores, and other cavity components.

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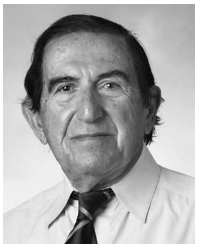

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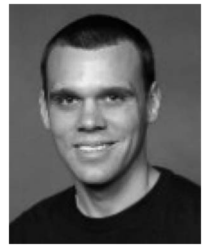

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K. Ward, photograph and biography not available at the time of publication.