

# *RF Technologies for Tagging, Tracking, and Locating*

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Presented to

## Force Tracking & Combat ID Conference

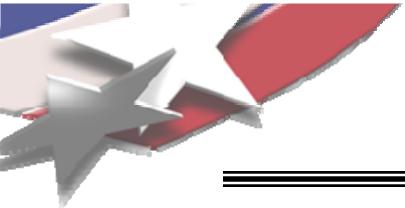
23-September-2005



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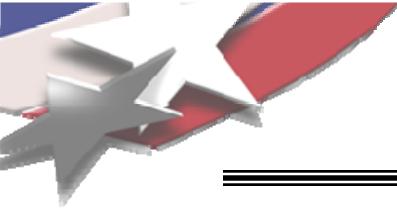


## *TT&L Background*

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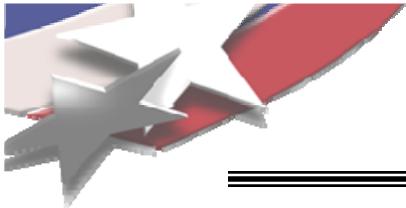
- Wide variety of tags for long-range TT&L
  - RF (MHz-GHz) → IR (near/far) → Optical
- Why **RF** for tags?
  - All-weather, day/night capable
  - Circuitry is robust, inexpensive, and shrinking
  - Supports a variety of system concepts
    - Air-Ground, Space-Ground, Ground-Ground, Air-Air
  - Applicable to static targets, vehicles, and dismount soldiers



# *Radar-Responsive RF Tags*

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- Why **radar** for RF tags?
  - Exists on many fielded platforms to *locate*, *identify*, and *track* targets of interest
  - Geo-location inherent in tag response
  - Many radars share similar bandwidth
  - Data extraction possible on some platforms
  - Radar tags are readily integrated into the mission CONOPS
- Radar tags aid pilot in “*Speak up or die*” decision making (anti-fratricide)

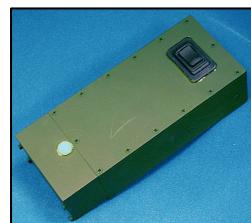


# *RF Tags at Sandia*

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- Fusing radar → SAR/MTI radar → RF tags
- Over a decade of RF TT&L programs

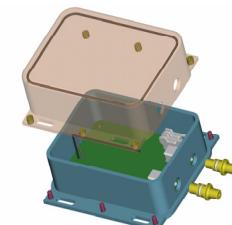
Radar-Responsive Tags

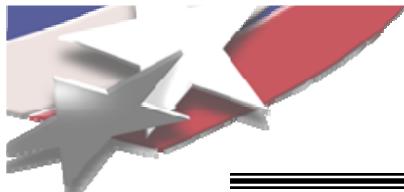


Communications Tags

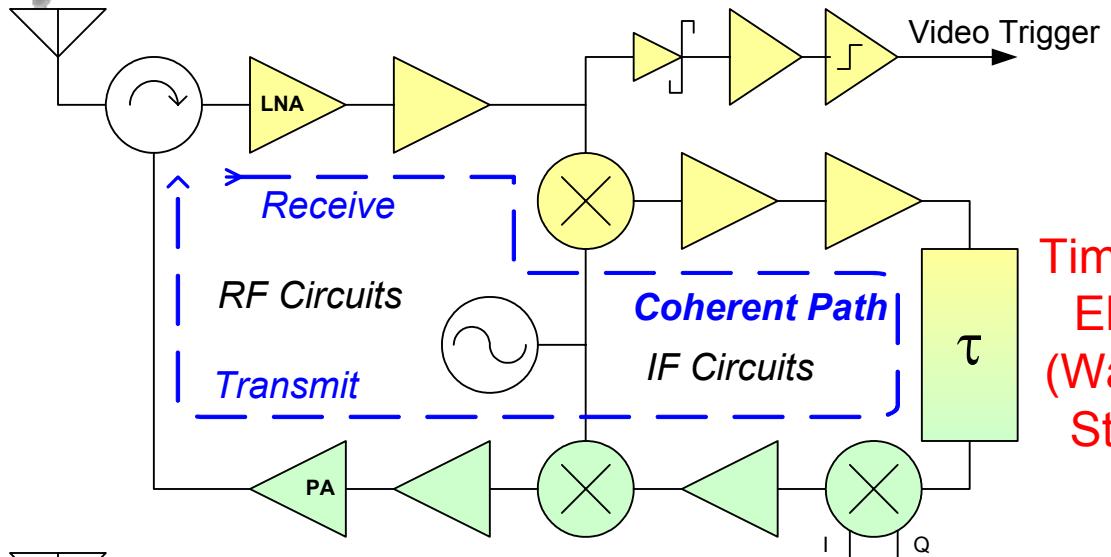


Monitoring Tags





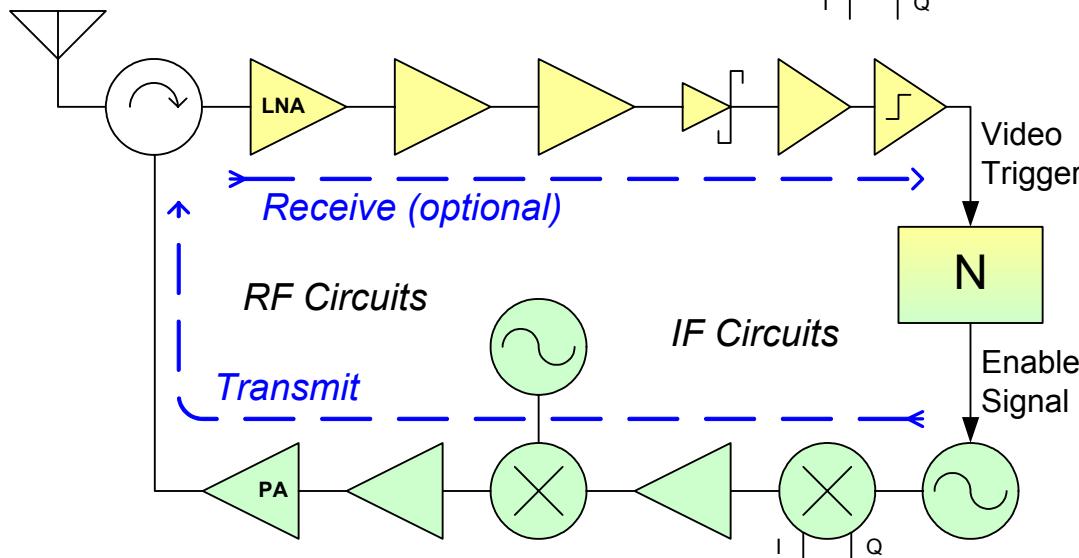
# Radar Tag Block Diagrams



**Coherent Architecture\***  
“Gain-Block” Tag

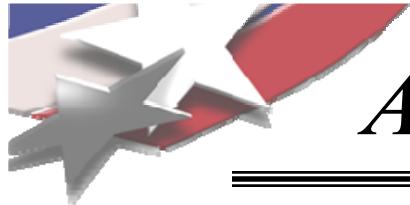
Time-Delay  
Element  
(Waveform  
Storage)

\* Sandia patent  
5,486,830, 1996



**Non-Coherent Architecture**  
“Receive/Transmit” Tag  
or “Beacon” Tag

Digital  
Timer



# *Athena Radar-Responsive Tag*

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- Blue-Force Tracking and Combat ID missions
- Responds to two different radar bands
- Based on Sandia's legacy coherent radar tags
- Includes electronics, antennas, and batteries

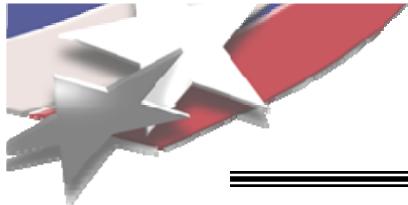


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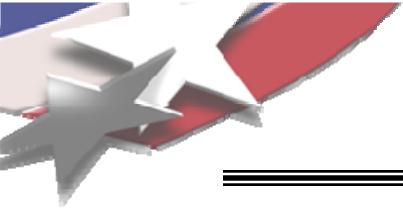


## *CCID ACTD MUA ~ UK*

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- Evaluate Radar/MMW/Optical tags & systems for air-ground and ground-ground CID
- 14 Athena tags on-site supporting air-ground
  - 10 M3 Bradley
  - 2 static sights
  - 2 spare tags





# *Next-Generation RF Tags*

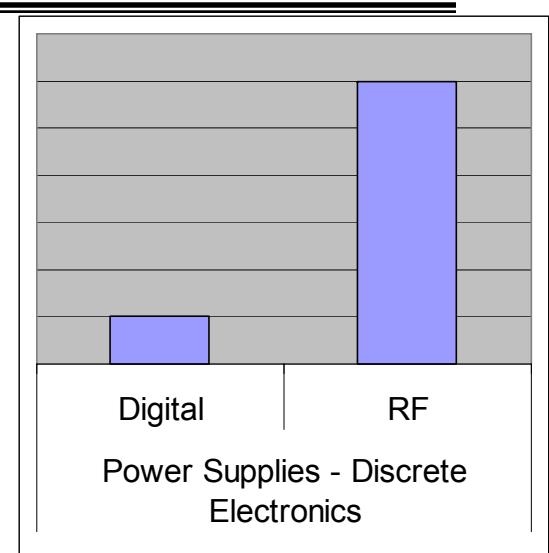
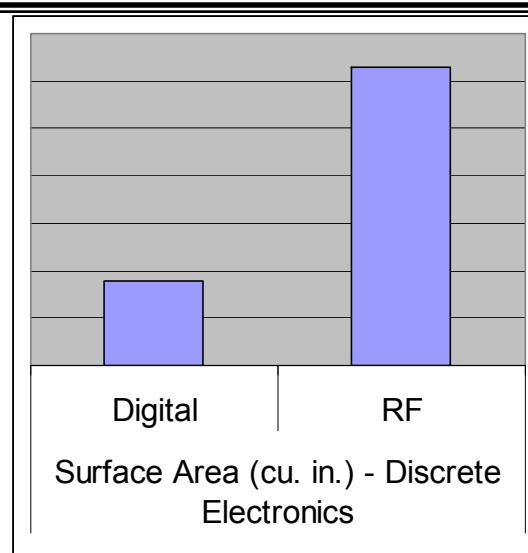
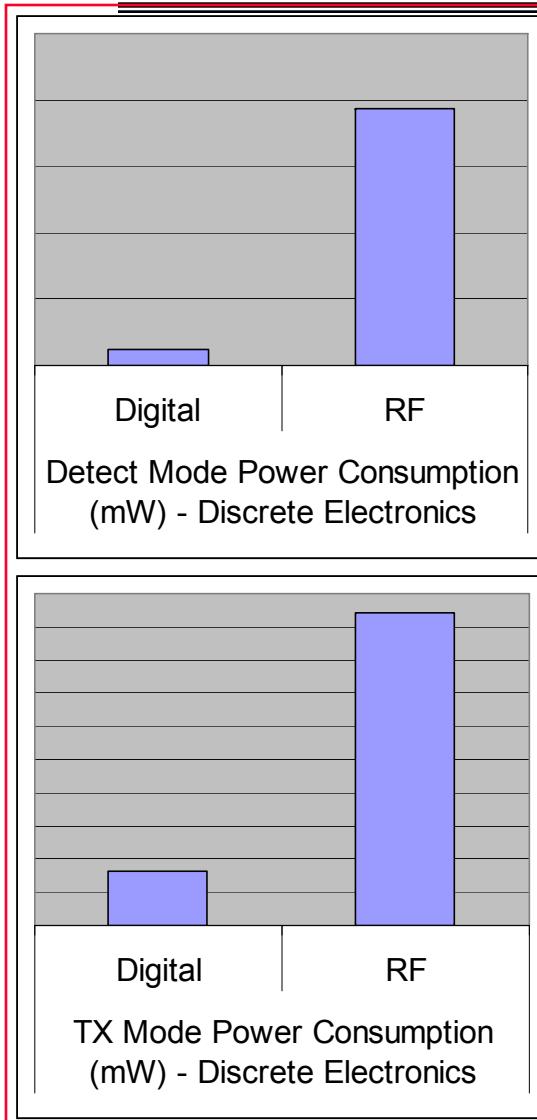
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- How can we improve today's RF tags?
  - Smaller volume... but retain ruggedness
  - Longer field life... but same or smaller battery
  - Increased functionality... but keep it simple to use
  - Increased autonomy... but retain user controls
  
- What are the challenges?
  - Decreased acquisition cost (of course!)
  - Works for all users and CONOPS (of course!)
  - Interoperable across all platforms (of course!)
  - Extensible to future systems (of course!)

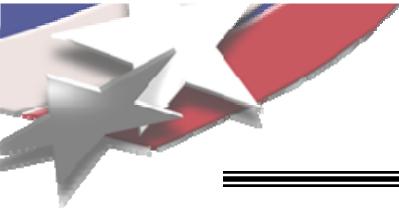


# Case Study: Athena Tag



**Clearly, RF components dominate the tag resources.**

**How can we improve on this?**

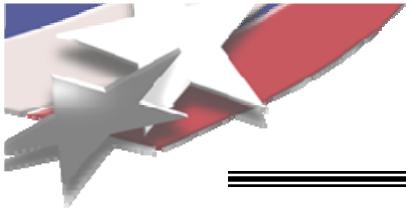


# *RF Integrated Circuits*

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- Integrate RF, IF, modulation, analog interface, etc., into a single RFIC chip or chip set
  - Maximum functionality with minimum DC power
  - Directly reduce DC power and volume
  - Overall increase in functionality
  
- Pertinent questions
  - What is the right level of integration?
  - What semiconductor technology is optimum?
  - What are the gains to be had?
  - What is the cost of such an endeavor?

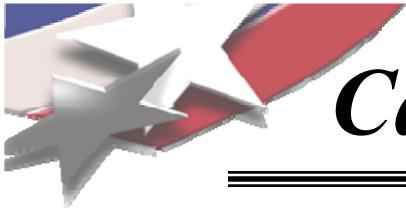


# *RFIC Technology*

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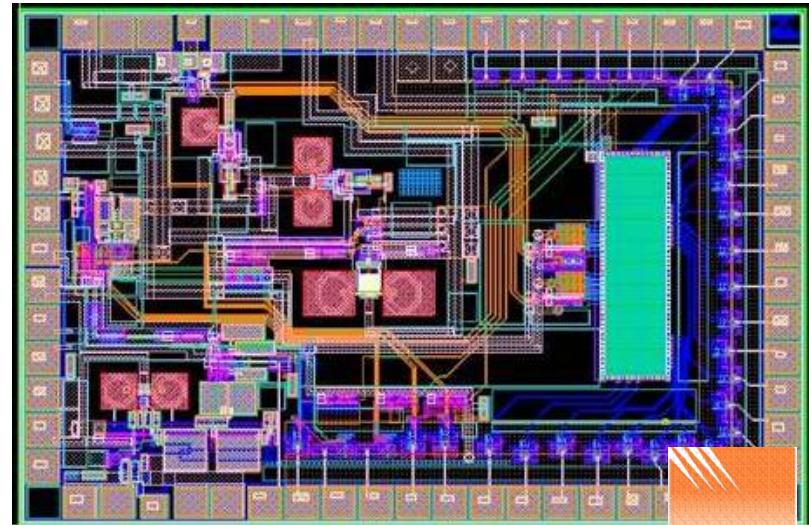
- Integrate high-frequency and complex circuits
  - Phase-locked loop and VCO
  - DDS/DAC and complex modulator
  - Digital interface/programmability
- Microwave design traditionally a III-V MMIC
  - Excellent performance at very high frequencies
  - 1s to 10s of transistors per chip typical (FET or HBT)
- Optimum technology: **Silicon Germanium BiCMOS**
  - SiGe processes easily reach airborne radar frequencies
  - 1000s of transistors including CMOS and interface circuits
  - Large-scale manufacturing for reduced cost



# *Case Study: Radar Beacon RFIC\**

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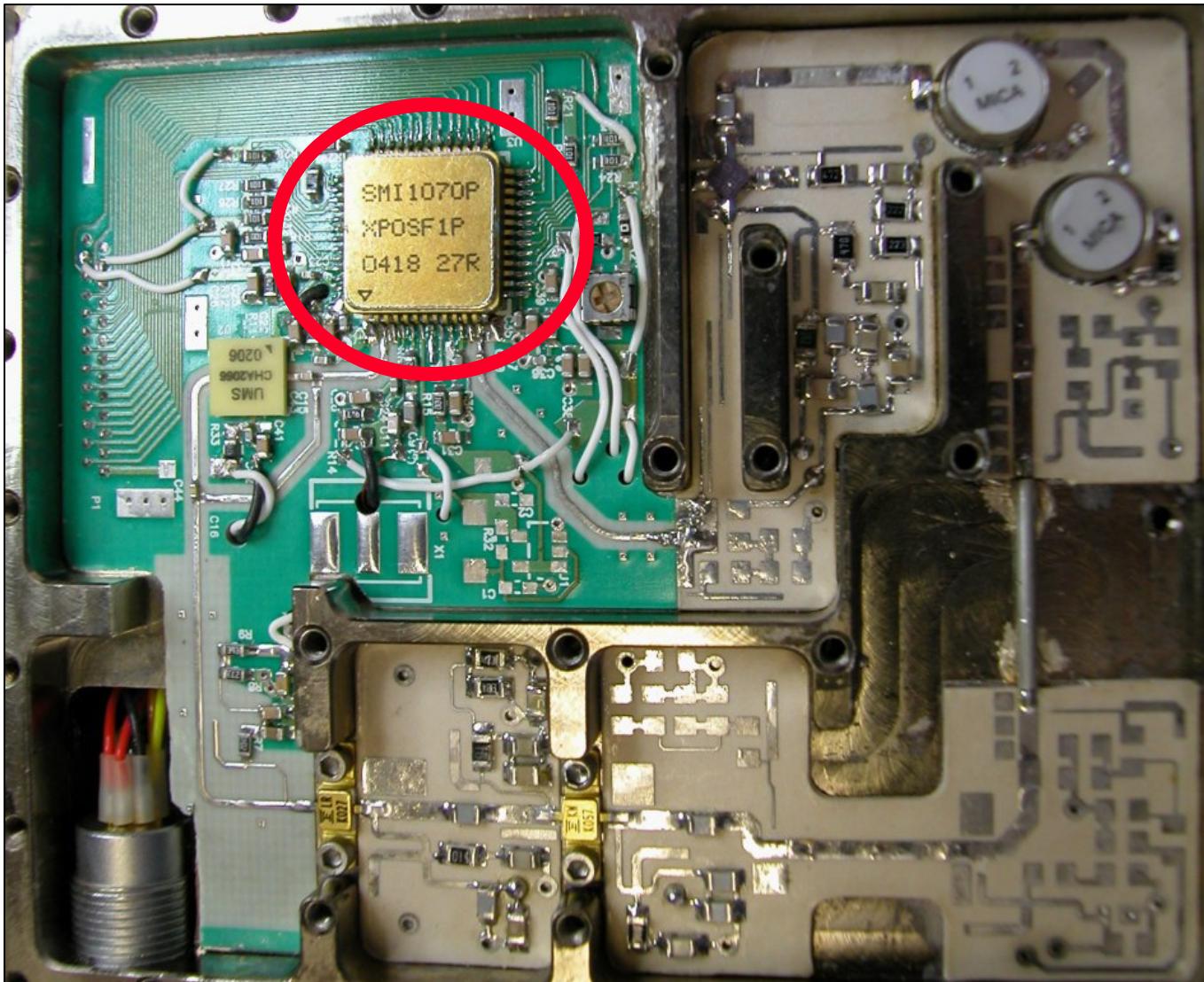
- RX/TX architecture in IBM 7HP SiGe
- Frequency and components similar to Athena
  - RF receive/transmit including video detector
  - DDS synthesizer & vector modulator (did not exist)
  - PLL w/ integrated VCO (replaced fixed-freq DRO)
- Results
  - ~ 20,000 transistors
  - > 2x less DC power
  - > 4x less board area



\* - Courtesy of Sierra Monolithics, Inc. Dave Clark, (310) 698-1030.

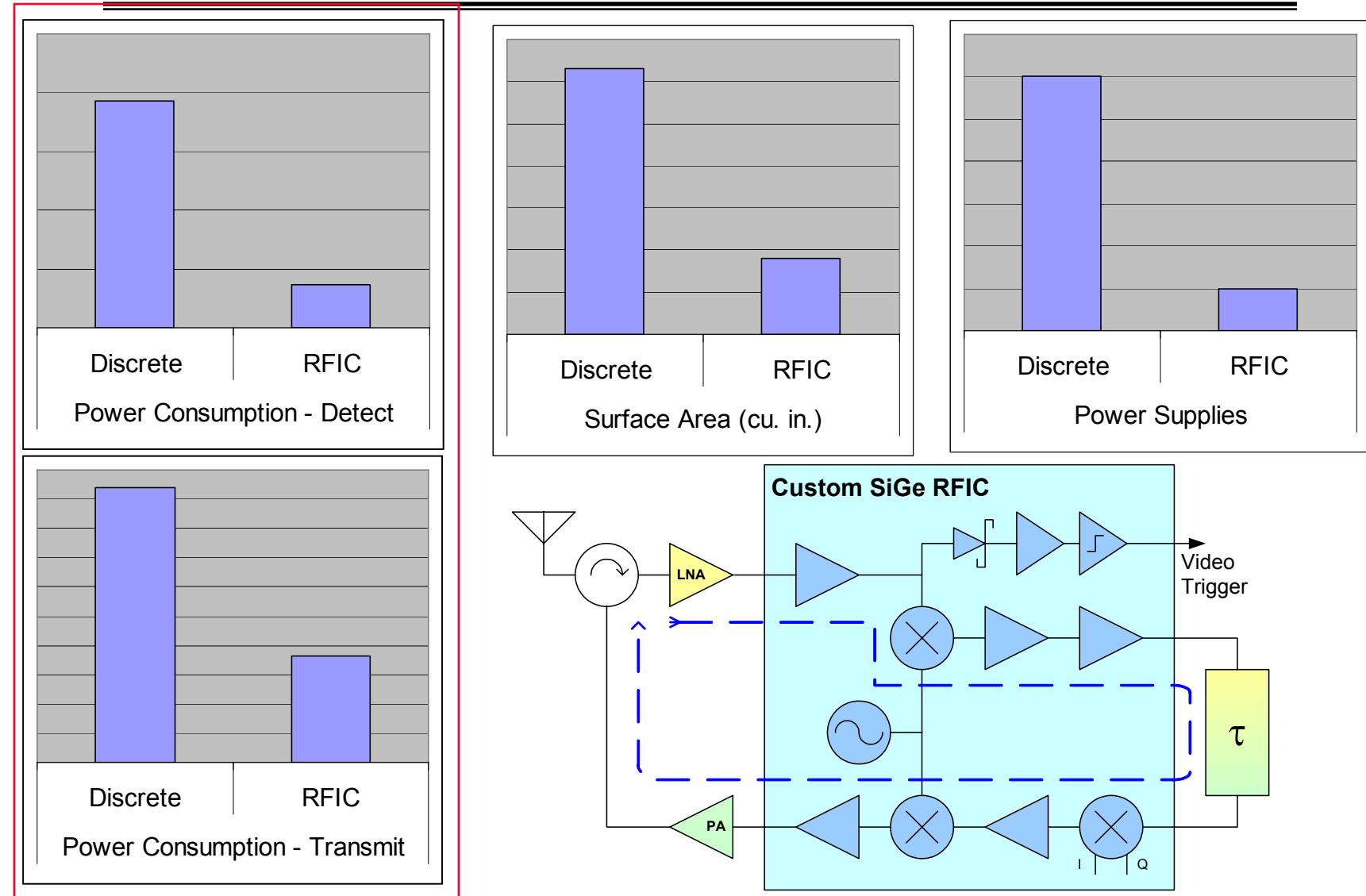


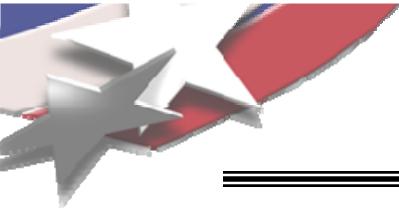
# RFIC Board Area Savings





# Applicability to Athena Tag



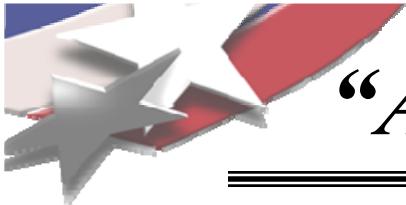


## *Impact on Tag Design*

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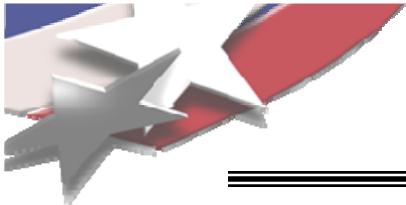
- Clearly, an RFIC allows significant reductions in tag size and DC power consumption
- Athena SiGe RFIC efforts underway
  
- SiGe RFIC cost concerns are valid
  - Affordability is a key to long-term success of tags
  - Significant NRE for design, fabrication, and test
  - Multiple design spins probable
  - Production runs expensive (but yield 1000s)



## *“Analog” vs. “Digital” RF Tags*

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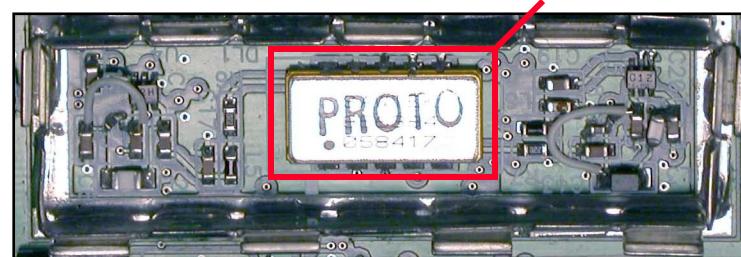
- This has been a confusing and misinterpreted topic in radar-responsive tagging
- Anti-Analogy: Cellular Telephony
  - Began w/ analog waveforms (FM/FDMA)
  - Migrated to digital waveforms (TDMA/CDMA)
- For radar tags, “Analog” and “Digital” applies to **waveform storage (time delay)**
  - Athena has “analog” time delay yet uses DAC-based digital modulation techniques

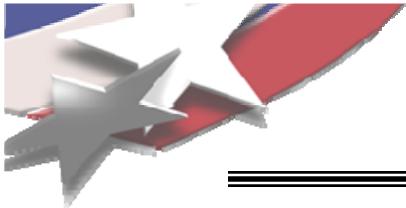


# Analog Delay Ideology

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- Time delay elements
  - RF: Coaxial cable, fiber optics, meander t-line, BAW
  - IF: SAW devices are small, inexpensive, surface-mount
- Advantages
  - Coherence stable over delay time
  - Delay stable over time and temperature
  - Very low power; overcome loss w/ low-power LNA
  - Field-proven methodology across many radar platforms
- Drawbacks
  - Fixed time delay
  - Fixed bandwidth
  - Lossy



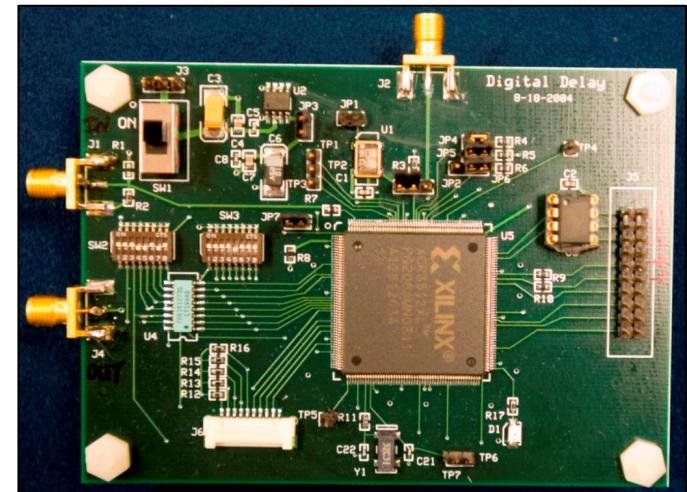


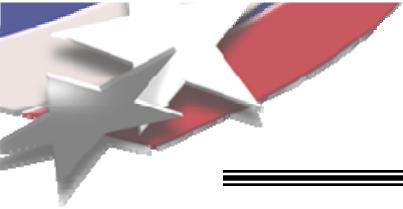
# *Digital Delay Ideology*

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- Digital RF Memory (“DRFM”)
  - Sample → store → recall → reconstruct
  - Complete DRFM includes ADC and DAC
- Advantages
  - Variable storage/playback
  - Digital filtering and modulation
  - Integrate with SiGe RFIC
- Drawbacks and TBDs
  - Power consumption of high-speed ADC/DAC vs. bandwidth
  - Coherence, delay vs. clock stability and jitter
  - Required number of bits

**Sandia 1-bit DRFM  
in COTS technology**



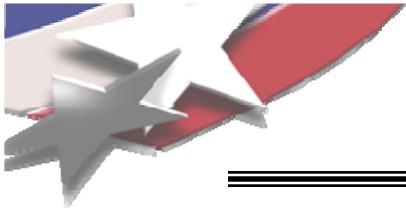


# *Impact on Tag Design*

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- Considerations for Analog vs. Digital delay
  - Limitations or capabilities of compliant radar?
  - CONOPS – what is required for the mission?
  - Available DC power: static, vehicle, or dismount?
- Plan ahead
  - Design with analog; add hooks for DRFM
  - Design with DRFM; add hooks for analog



# *Conclusions*

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- Maximizing tag usefulness requires...
  - ✓ Understanding of CONOPS and users
  - ✓ Reducing tag volume and power consumption
  - ✓ Balancing affordability with complexity
  - ✓ Pursuing advanced technologies intelligently
- “Next-generation” tags are under development

- Questions?

