HIGH CURRENT FAST 100-NS LTD DRIVER DEVELOPMENT IN SANDIA LABORATORY*

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Abstract

During the last few years Sandia is actively pursuing the development of new accelerators based on the novel technology of Linear Transformer Driver (LTD). This effort is done in close collaboration with the High Current Electronic Institute (HCEI) in Tomsk, Russia, where the LTD idea was first conceived and developed. LTD based drivers are currently considered for many applications including future very high current Z-pinch drivers like ZX and IFE (Inertial Fusion Energy), medium current drivers with adjustable pulse length for ICE (Isentropic Compression Experiments), and finally relatively lower current accelerators for radiography and x-pinch. Currently we have in operation the following devices: One 500-kA, 100-kV LTD cavity, a 1-MVvoltage adder composed of seven smaller LTD cavities for radiography, and one 1-MA, 100-kV cavity. The first two are in Sandia while the latter one is still in Tomsk. In addition a number of stackable 1-MA cavities are under construction to be utilized as building blocks for a 1-MA, 1-MV voltage adder module. This module will serve as a prototype for longer, higher voltage modules, a number of which, connected in parallel, could become the driver of an IFE fusion reactor or a high current Z-pinch driver (ZX). The IFE requirements are more demanding since the driver must operate in rep-rated mode with a frequency of 0.1 Hz.

In this paper we mainly concentrate on the higher current LTDs: We briefly outline the principles of operation and architecture and present a first cut design of an IFE, LTD z-pinch driver.

I. INTRODUCTION

LTD is a new method for constructing high-current, high-voltage pulsed accelerators [1]. The salient feature of the approach is switching and inductively adding the pulses at low voltage straight out of the capacitors through low inductance transfer and soft iron core isolation. High currents can be achieved by feeding each core with many capacitors connected in parallel in a circular array. High voltage is obtained by inductively adding many stages in series. Utilizing the presently available capacitors and switches we can envision building the next generation of fast z-pinch drivers without the usage of large deionized-water and oil tanks as is the case with the conventional technology drivers. For example, an LTD based replacement of Saturn accelerator could fit in the space now occupied only by its water tank [2]. In addition to the relative compactness, LTD has a number of very significant advantages compared to the Marx-and-water-line technologies: These drivers do not require insulating dielectric stacks for high voltage hold-off, and the coaxial voltage adders made of LTDs and the transmission MITLs are directly connected, without interface, to the reaction vacuum chamber. All the switches operate with pressurized air and not with SF6, so there are no asphyxiation hazards. The device is contained within the steel walls of the LTD cavities and is grounded at all times. Hence the electrical hazard is dramatically reduced. The gas switches are very quiet; therefore there is no mechanical shock to significantly shorten the life of the assembly. However the most important advantage of all is that the LTD drivers offer the possibility of a rep-rated operation. They can be multipulsed with a repetition rate, in principle, up to the capacitor specifications which is of the order of 10 Hz. The later makes LTD the driver of choice for IFE where the required repetition rate is 0.1 Hz. In the following

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sections we briefly describe the basic circuit theory underlying the LTD operation, present and give performance results of our fast high current LTD cavities currently in operation and under construction, and finally discuss a first cut design of an IFE driver utilizing the 1-MA, 100-kV cavity as a building block.

II. THE LTD PRINCIPLE AND ITS EQUIVALENT CIRCUIT

An LTD cavity is a simple device of which the equivalent circuit can be represented by Fig. 1. It contains a switch, a capacitor C, a total inductance L and a resistance R. We assume that the switch represents all the parallel-connected switches of the cavity, the capacitor is equal to the sum of the capacitance of all the capacitors,

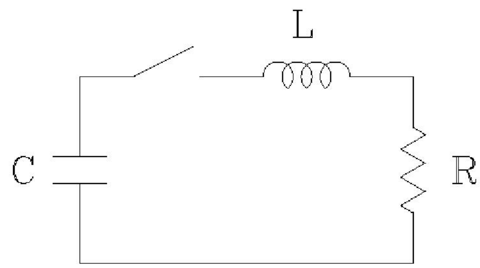

Figure 1. The simple LTD equivalent circuit.

the inductance is equal to the total inductance including that of the switches and capacitors, and finally the resistance R includes the load plus the internal resistance of the cavity.

The second order differential equation that governs the circuit behavior is the typical damped oscillation one which is given by the familiar expression of Eq. (1).

$$L \frac{di^2}{dt^2} + R\frac{di}{dt} + i/C = 0 \tag{1}$$

This equation can be solved analytically, and in its general form the solution has a rather complicated trigonometric expression for the load voltage, current and energy as a function of time [1]. However there are two special cases where the solution has simple forms: when R = √L/C and when R=2√L/C. The first is the "matched" case where the load resistance is equal to the characteristic impedance of the circuit, and the second is the critically matched case where the solution does not exhibit any oscillation. In the matched case the time to peak current and voltage and the values at that particular time of the voltage, current and energy transferred to the load are given by the following expressions:

$$t_{peak} = \frac{2\pi}{\sqrt{3^3}}\sqrt{LC} \equiv 1.21\sqrt{LC} \tag{2}$$

$$i_{peak} = \frac{2V_0}{\sqrt{3}R} e^{-\frac{\pi}{3\sqrt{3}}} \sin(\pi/3) = 0.546293\frac{V_0}{R} \tag{3}$$

$$V_{peak} = Ri_{peak} = 0.546293V_0 \tag{4}$$

$$E(t_{peak}) = 0.4031279 \tag{5}$$

In the critically matched case the peak current is smaller by 33% and the energy transferred to the load at peak time is smaller by 20%. However the rise time is shorter and the peak voltage higher:

$$t_{peak} = \sqrt{LC} \tag{6}$$

$$V_{peak} = 0.73576V_0 \tag{7}$$

From the above arguments and expressions it is obvious that for radiographic machines where the x-ray output is proportional to a higher than quadratic exponent of the electron beam voltage, and where the output current requirements are relatively modest, the critically (R= 2√L/C) or higher overmatched load conditions are the choice. Indeed the first radiographic LTD machine currently in operation in Sandia is critically matched to the radiographic diode load [3].

On the other hand, for Z-pinch drivers where large current and efficient energy transfer to the load at peak current are of paramount importance, simply matched loads of √L/C should be the configuration of choice. However, recent current scaling experiments with the Z accelerator [4] demonstrated that faster current rise time driven pinches, and shorter implosion times (although with lower peak load current) yielded higher x-ray radiated power. So it is not inconceivable even for large Z-pinch drivers to select a critically matched design which provides faster load current rise times despite the lower peak current. In the IFE Z-pinch driver design presented here we opt to be conservative and select a simply matched approach.

III. A DESIGN FOR THE NEXT GENERATION OF Z-PINCH OR IFE DRIVER BASED ON LTD

The present thinking for the future high current drivers is that in order to achieve target ignition and high gain, the drivers should provide a current to the load not less than 60 MA with a rise time of 100 ns or preferably less. The load inductance could be of the order 10-15 nH. Therefore a driver capable of driving that inductance will be necessary.

Based on the above consideration we select a 60-MA, 6-MV, driver. The building blocks are 1-MA, 100-kV, ~70-ns pulse rise time LTD cavities similar to the one shown in Fig. 2. Figure 3 presents the measured voltage and current output of these cavities. [5]

Each cavity has 40, 200-kV switches and 80 capacitors arranged in 40 individual circuits (bricks) feeding in parallel the accelerating cavity gap through an iron tape core. The capacitors of the brick are charged to opposite 100-kV polarity and are connected to the two ends of the switch.

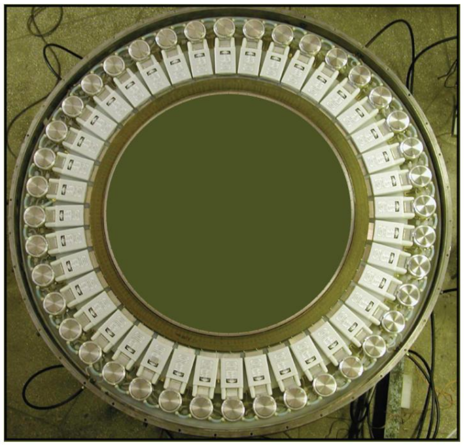

Figure 2. 1-MA, 100k-V, 70-ns LTD cavity with the top flange removed. The 40 switches and the top capacitor of the 40 individual (brick circuits) are also shown.

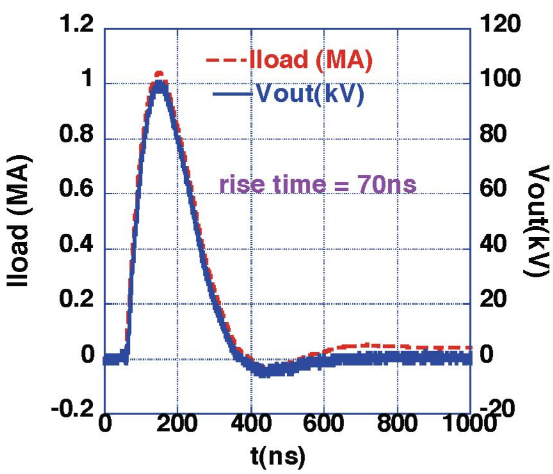

Figure 3. Voltage and current output of the 1-MA, 100-kV cavity.

When the switch closes, approximately a 100- kV voltage pulse is applied to the accelerating gap (matched case). The total inductance of one brick, including the switch inductance and that of the two capacitors connected in series, is 232 nH. The capacitance of the two capacitors is 20 nF (40 nF each), and their internal resistance is 0.600 Ohms (0.300 Ohm each). Therefore the equivalent circuit of Figure 1 for one 1-MA, 100-kV cavity will have L = 5.8 nH, C = 800 nF, internal resistance 0.015 Ohms, and matched external load resistance equal to 0.070 Ohms.

We select 60, 60-cavity voltage adders connected in parallel to a single bi-plate or tri-plate transmission line feeding the final Recyclable Transmission Line (RTL) in the center of which is located the z-pinch load and the IFE capsule. A single level arrangement of the voltage adders will be preferable for IFE since it will make the system of fast replacement of the RTLs and the power flow from the IVA to the RTL much simpler. In that case no convolutes will be required (Fig. 4).

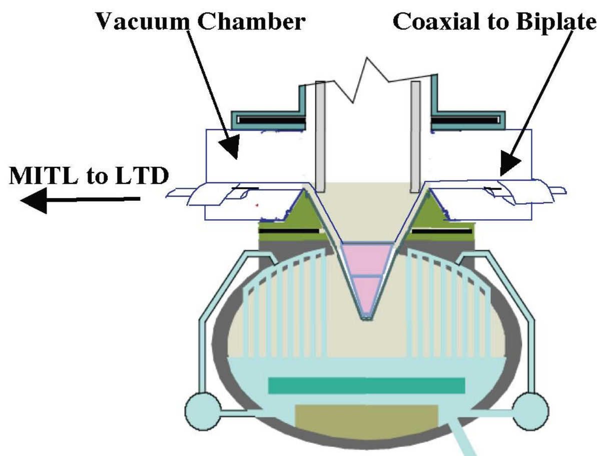

Figure 4. IFE z-pinch reaction chamber fed by LTD modules connected to the load in parallel through coaxial to bi-plate transition region (single ended wire array load).

The disadvantage of this architecture is that the driver's footprint is large. If that becomes a serious concern, especially for a Z-pinch ICF driver, a multilevel arrangement with convolutes could be considered. In the system considered here the number of cavities per module and the number of modules connected in parallel are the same. Therefore the entire 60-MV driver will have an equivalent circuit identical to that of one cavity. The total values of inductance, capacitance and resistance of the driver are estimated assuming 60 cavities connected in series in each voltage adder and 60 voltage adders connected in parallel to feed a single wire array load with final MITL inductance (L_{MITL}) of 10 nH and initial load inductance of 1 nH. Figure 5 presents a circuit model result for a total mass load of 55mg.

The cavity diameter is of the order of 3 m. The radius of closest approach of the front of 60 voltage adders cannot be shorter than 31 m, which necessitates coaxial MITLS of similar length to connect the output of the voltage adder to the load. Although this will erode the front of the pulse, it will also have two beneficial effects; first it will sharpen the pulse front and thus give the increased power output of the fast pinches; second it will time isolate the cavities from the load and make them unaffected by the load inductance increase during the final stages of the implosion.

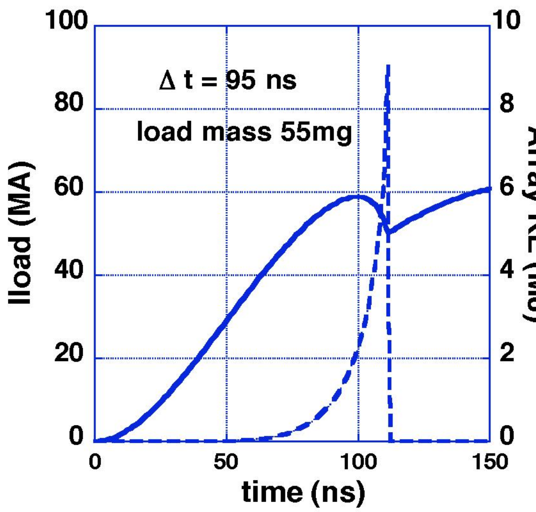

Figure 5. Load and kinetic energy of an imploding 55 mg single array load. The driver is a 60 module, 60 cavity per module LTD.

A 60 cavity voltage adder, including the length of pumping stations, will be approximately ~13-m long. Therefore the overall radius of the driver will be of the order of 44 m and the height including the support structure ~5 m. It will contain a total of 3,600 cavities, 144,000 pressurized air closing switches and 288,000 capacitors. Indeed the number of components is very large; however there are only four major components in the entire driver which repeat themselves many times: a capacitor, a switch, an iron core and a cavity housing. This also provides redundancy, the great advantage of jitter reduction, and graceful degradation. In addition of course there is a large cost reduction in purchasing many identical components.

The above design is quite optimistic and ideal. It neglects the losses in the long MITL's and coaxial to bi-plate or tri-plate transition region. In order to precisely estimate the losses, 2D and 3D particle in cell code modeling will be necessary. Previous similar system studies during the JUPITER [6] and LMF [7] projects,

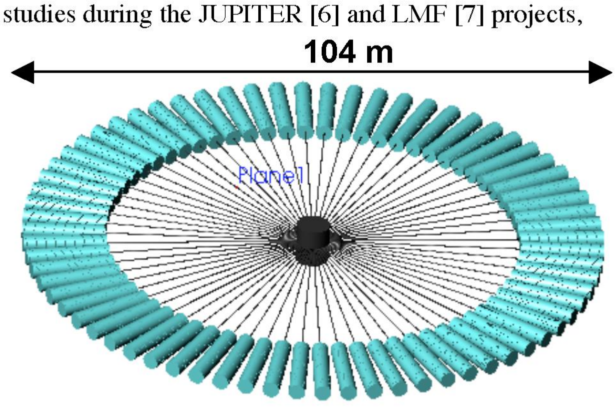

Figure 6. Top view of a 70 modules 70 cavity per module, LTD, driver. The overall diameter is 104 m.

suggest an approximate 10%-15% total current loss in the long MITLs due to front pulse erosion and losses in the transition region due to magnetic nulls. To compensate for that, in a subsequent design (Fig. 6), we increased the number of module adders from 60 to 70.

IV. SUMMARY

We have briefly presented the LTD technology, described the basic formalism that governs the LTD behavior, its components and architecture, the LTD cavity simple equivalent circuit, and described a first cut of 60-MA, 6-MV, 70-ns design for Z-pinch ICF or IFE driver. The load current and the final kinetic energy of the imploding array were also presented.

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