Theory of Charge Induction in MOS Structures

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Motivation—Silicon-On-Insulator (SOI) circuits have been considered less sensitive to single event effects (SEE) than devices made using bulk technology. It was believed in the past that charge is collected only from the active layer above the buried oxide (BOX) but not from the substrate below the BOX. Recently, as the BOX thickness decreased significantly SOI SRAMS were found to be more sensitive to SEE than expected. Model experiments showed that there is significant charge collection from below the BOX. Here we present an analytical model based on the Gunn-theorem to describe ion induced charge collection in MOS (Metal-On-Semiconductor) devices.

Accomplishment—At first we have to emphasize that although the term "charge collection" is widely used it is incorrect. Charge is never collected but rather induced. When a high energy heavy ion hits a device electron-hole pairs are generated. Those electron-hole pairs that were created in a fielded region (such as a p-n junction) start drifting apart and will induce charge on the electrodes of the device. A fraction of the electron-hole pairs that were created in a field free region will eventually diffuse to the fielded region and will drift through it. According to the Gunn-theorem the current induced by a moving charge q on the ith electrode of the device is $I_i = -q\mathbf{v}\,\partial\mathbf{E}/\partial V_i$ where $\mathbf{v}$ is the velocity of the moving charge $\partial\mathbf{E}/\partial V_i$ and is the differential of the electric field with respect to the voltage on the ith electrode while the voltage is kept constant on all the other electrodes. Applying the Gunn-theorem and the basic equations of electrostatics it can be shown that the induced charge in and MOS capacitor is

$$\frac{q_c}{q_d} = \frac{\lambda/\varepsilon_{Si}}{\lambda/\varepsilon_{Si} + x_{ox}/\varepsilon_{ox}} \text{ with } \lambda = \langle x \rangle + Q \cdot \partial\langle x \rangle / \partial Q$$

where Q is the total charge per unit area, $<x>$ is the distance from the oxide-substrate interface averaged over the charge distribution. An MOS capacitor can be in three states. In accumulation, when the majority carriers pile up the interface, in depletion when fixed impurity atoms are ionized creating a depletion layer, and in inversion where the depletion layer width is saturated and minority carriers pile up at the interface. From the above equation it is obvious that λ is significantly different from zero only in the depletion and inversion regime; therefore, we can expect charge collection in these regimes only as the experiments showed. Figures 1 and 2 show the dependence of the charge collection on the bias and BOX thickness measured with IBIC (Ion Beam Induced Charge) and calculated using the above model. The calculated curves qualitatively agree with the measurements, but they reach saturation at much lower biases than the experimental ones. It might be due to the trapped interface charge and the charge accumulating during at the interface during the charge collection process. These will be included later in the model.

Significance—SOI promises devices less sensible to SEE than those made using bulk technology. It is important to understand how the ion induced charge collection works in these devices. The above analytical model provides and easy and fast way to calculate the collected charge in MOS structures.

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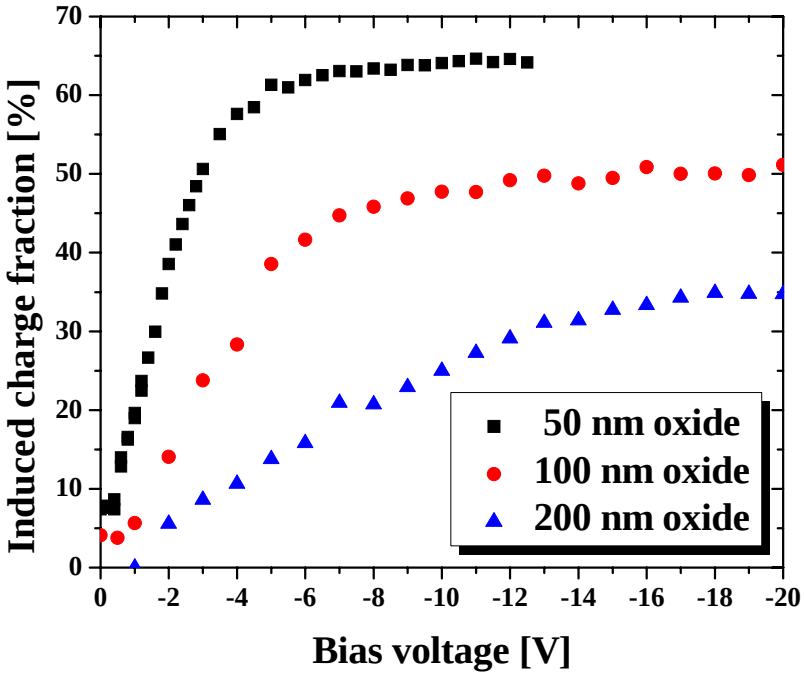

Figure 1. Measured induced charge fraction using IBIC.

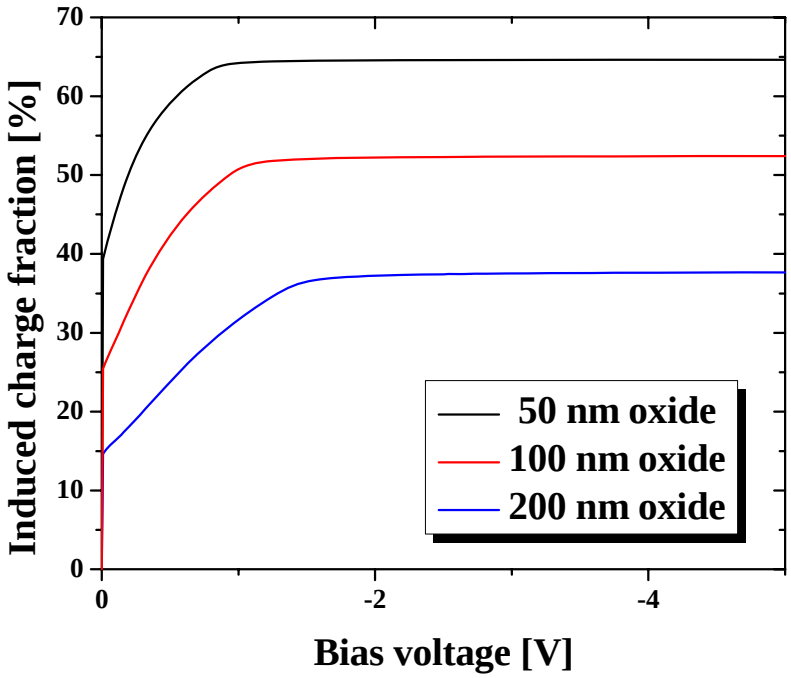

Figure 2. Calculated induced charge fraction.