Single Event Upsets (SEUs) in Silicon-On-Insulator (SOI) Technology

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Motivation—Silicon-On-Insulator (SOI) technology was thought to be less prone than bulk circuits to Single Event Upsets (SEUs) due to heavy ion hits because of its design. It was believed that the charge deposited in the buried oxide (BOX) and the substrate would not contribute to the charge collection process. Therefore, the SEU cross-sections were expected to be on the order of the gate areas. Recent measurements on Sandia National Laboratories (SNL) SOI SRAMs with thin BOX showed that these cross sections are closer to the sum of the gate and drain areas, which indicated higher than ex-pected charge collection in these circuits. We have performed charge collection and SEU experiments using the SNL nuclear microprobe on actual SRAMs and model circuits to investigate this anomalously high charge collection.

Accomplishment—SOI circuits were considered more radiation hard because the sensitive volume was thought to be much smaller than in bulk circuits. Although there were some experiments several years ago that indicated significant charge collection in MOS structures, they were overlooked because previous SOI circuits had not shown anomalously high SEU rates. That was due to the thick BOX that was several thousands of nanometers. Newer technologies required much thinner BOX layers, on the order of a few hundred nm. After discovering the anomalously high charge collection, it was thought to be due to the formation of a con-ducting "pipe" in the oxide during and shortly after the ion hit. We carried out charge collec-tion experiments on MOS capacitor structures to model the SOI circuits. We found that the charge collection has a very strong dependence on the applied bias. The charge collection was significant at negative biases and practically zero for positive biases for n-type substrates. The opposite was observed for p-type substrates. This result showed immediately that the conduc-tive pipe model was incorrect. Figure 1 shows the charge collection dependence on the applied bias for both n and p-type substrates. The same experiment carried out on p+ and n+ substrates resulted in much lower charge collection. The amount of collected charge decreased with increasing oxide thickness. Based on the above observation we could qualitatively explain the charge collection, which was later proven quantitatively by 3D device codes. When the MOS capacitor is in depletion or inversion mode (negative bias for the n-type and positive bias for the p-type substrate) there is a significant electric field at the oxide-substrate interface. This field increases with decreasing oxide thick-ness. According to the Gunn theorem when the charge generated by the ion hit moves through this field, it will induce charge on the electrodes of the device. The charge collection at zero bias in the case of p-type substrates is probably due to trapped process charge. These results led to a mitigation technique to reduce the charge collection from the substrate below the oxide. Figure 2 shows the charge collection map for SNL SRAMs with and without applying bias to the substrate.

Significance—SOI is a very promising technology to produce radiation hard circuits. It is important to understand the charge collection in these devices. Our experiments showed that, in contrast to the earlier beliefs, these devices have significant charge collection when the BOX layer is thin. The explanation of the model ex-periment helped find a mitigation technique.

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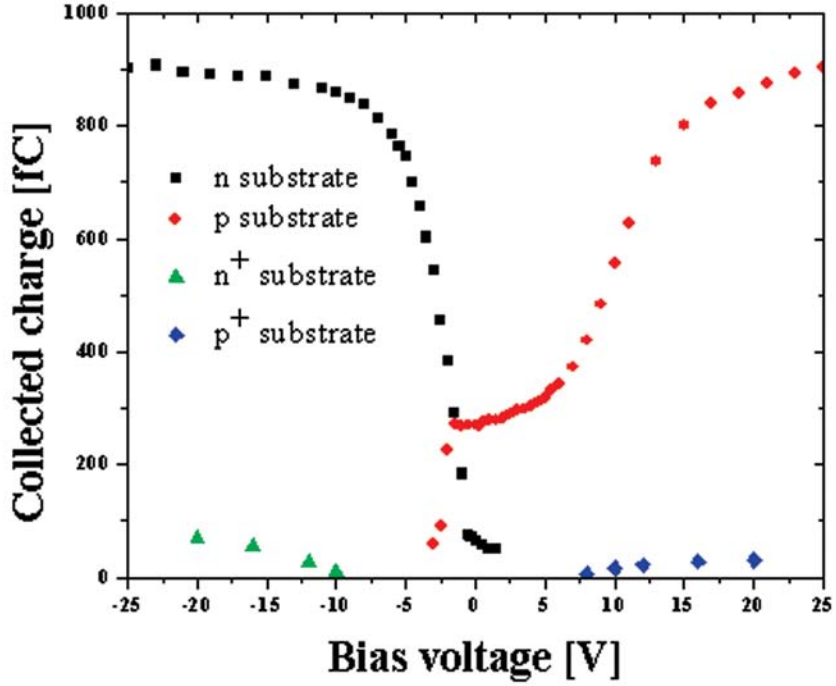

Figure 1. Charge collection as a function of applied bias for MOS capacitors on different substrates.

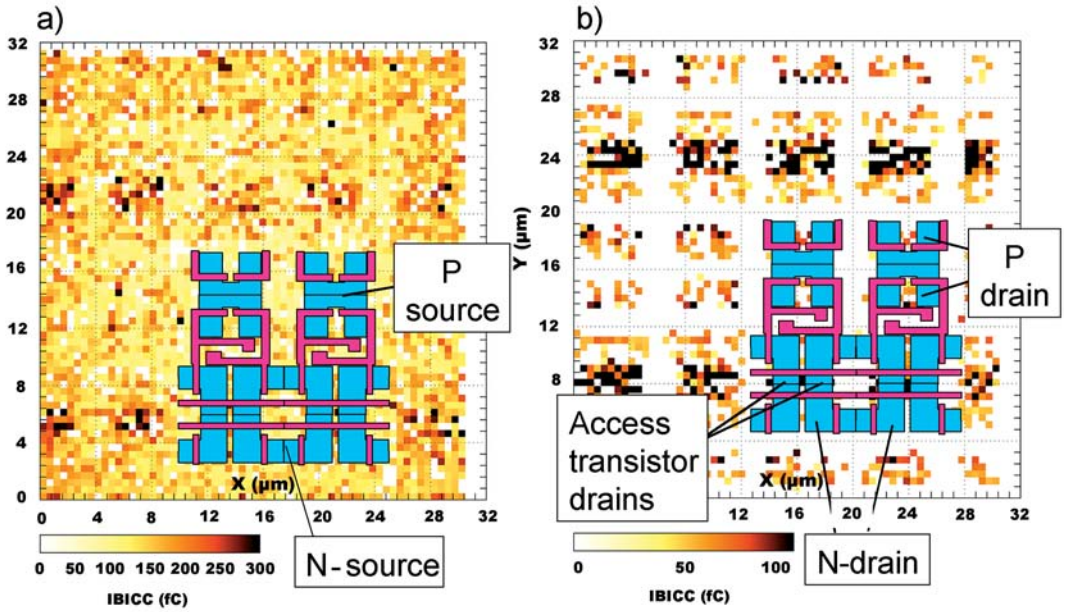

Figure 2. Charge collection maps of SNL SRAMs (n-type substrate) with different biases applied to the sub-strate. The applied negative bias significantly suppresses the charge collection.