

Novel Electrical and Optoelectronic Characterization Methods for Semiconducting
Nanowires and Nanotubes

By

AARON MICHAEL KATZENMEYER

B.S. (Ohio University) 2001

M.S. (TU Delft/U Leiden) 2006

M.S. (KU Leuven/IMEC) 2007

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DAVIS

Approved:

M. Saif Islam, Chair

François Léonard

David A. Horsley

Committee in Charge

2011

In memoriam:

Dale L. Katzenmeyer

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Abstract

As technology journalist David Pogue recounted, “If everything we own had improved over the last 25 years as much as electronics have, the average family car would travel four times faster than the space shuttle; houses would cost 200 bucks.”

The electronics industry is one which, through Moore’s Law, created a self-fulfilling prophecy of exponential advancement. This progress has made unforeseen technologies commonplace and revealed new physical understanding of the world in which we live. It is in keeping with these trends that the current work is motivated. This dissertation focuses on the advancement of electrical and optoelectronic characterization techniques suitable for understanding the underlying physics and applications of nanoscopic devices, in particular semiconducting nanowires and nanotubes.

In this work an *in situ* measurement platform based on a field-emission scanning electron microscope fitted with an electrical nanoprobe is shown to be a robust instrument for determining fundamental aspects of nanowire systems (i.e. the dominant mode of carrier transport and the nature of the electrical contacts to the nanowire). The platform is used to fully classify two distinct systems. In one instance it is found that indium arsenide nanowires display space-charge-limited transport and are contacted Ohmically. In the other, gallium arsenide nanowires are found to sequentially show the trap-mediated transport regimes of Poole-Frenkel effect and phonon-assisted tunneling.

The contacts in this system are resolved to be asymmetric – one is Ohmic while the other is a Schottky barrier.

Additionally scanning photocurrent microscopy is used to spatially resolve optoelectronic nanowire and nanotube devices. In core/shell gallium arsenide nanowire solar cell arrays it is shown that each individual nanowire functions as a standalone solar cell. Nanotube photodiodes are mapped by scanning photocurrent microscopy to confirm an optimal current collection scheme has been realized and to locate the devices' most responsive region. The devices are shown to exhibit strongly enhanced photocurrent under reverse bias proposing unexpected efficiency increases in a scalable device layout.

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1 Introduction

1.1 MOTIVATION AND BACKGROUND

Semiconducting nanowires (NWs) and nanotubes (NTs) have been shown to offer substantial promise not only in regard to the scaling trend in high performance electronics but also for enabling new technologies altogether (e.g. highly responsive sensors, solar cells, batteries, etc.). Despite this potential and some remarkable displays of NW/NT-based devices, this field remains nascent, particularly in regards to understanding and utilizing the physical properties of NWs, NTs and devices comprised thereof.

A large and comprehensive body of work has been compiled on intrinsic electrical properties and transport mechanisms in carbon nanotubes (CNTs); however, this effort has not yet been paralleled by NW studies, largely due to the myriad growth methods, atomic compositions, and resulting varied carrier behavior. Likewise, the knowledge base for useful single-wall CNT (SWCNT) devices is still limited. These areas have been identified as major roadblocks that currently prevent the realization of commercial NW and NT devices. It is therefore the purpose of this Ph.D. work to establish novel characterization methodologies for determining intrinsic properties and electrical transport mechanisms of individual NWs and optoelectronic properties of SWCNT devices.

Currently the most often used protocol for determining electrical properties of interest in individual NWs or NTs is to fabricate a NW/NT-field-effect transistor (FET) and analyze the transfer characteristics.¹ Figure 1 depicts the most common embodiment of a

NW/NT-FET, the back-gated version.²⁻³ The gate stack is comprised of a degenerately doped Si wafer (contacted through the back side) with a thermal oxide grown on top (typically 100 – 1000 nm in thickness). The NW or NT itself serves as the channel. All devices on a wafer share the global back-gate which limits the technological efficacy of this method, but the format is effective for investigating properties of single NW/NT-FETs. The devices can be fabricated using e-beam or standard photolithographic techniques; however, both techniques are labor intensive, time consuming and provide low yield. Figure 1 b) depicts a field emission scanning electron microscope (FE-SEM) image of one of our InAs NW-FETs prepared at the beginning of our investigation of these NWs. This device was fabricated by spin-casting a dilute suspension of NWs in isopropanol onto the Si/SiO₂ wafer, performing photolithography, removing residual photoresist from the contact regions with an O₂ plasma descum, performing a brief buffered oxide etch to remove oxide from the NW contact regions, metallizing (300 nm Au with a 10 nm Ti adhesion layer) and performing liftoff.

The devices are then measured in order to obtain their transconductance, dI_{sd}/dV_g , the change in source-drain current as a function of gate voltage, which enables one to deduce the carrier type based on the response and also extract the field-effect mobility according to:

$$\mu = \frac{L^2}{CV_{sd}} \left(\frac{dI_{sd}}{dV_g} \right), \quad (1)$$

where L is the length of the NW channel, V_{sd} is the source-drain voltage and C is the capacitance which is given by:

$$C = 2\epsilon_0\epsilon_r \frac{L}{\ln(2tR)}, \quad (2)$$

where ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of SiO_2 , t is the thickness of the oxide and R is the radius of the NW.

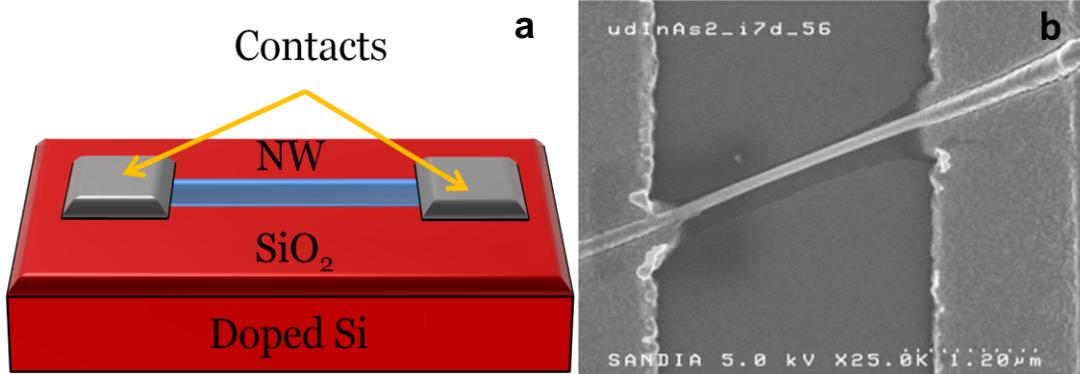


FIGURE 1 a) Schematic of a typical back-gated NW-FET. b) Top-view SEM micrograph of one of our InAs NW-FETs.

The carrier concentration, n , can be determined using the threshold voltage, V_{th} found from the transfer characteristic as:

$$n = \frac{CV_{th}}{e}, \quad (3)$$

where e is the fundamental electron charge. The carrier concentration can also be extracted from the Ohmic current equation once μ is known and the source-drain conductance is measured. This latter method is dependent on the measured mobility and the former determination is preferable being an independent measurement; however, in the case that the FET cannot be gated to its threshold, there is no other option. As such, both determinations of n are precarious.

Also it should be explicitly stated that the values extracted from NW-FETs for μ and n are *field-effect* values. These values describe the NW-FET as a device but not

necessarily the intrinsic values for the NW. Figure 2 shows a typical transfer characteristic from one of our InAs NW-FETs.

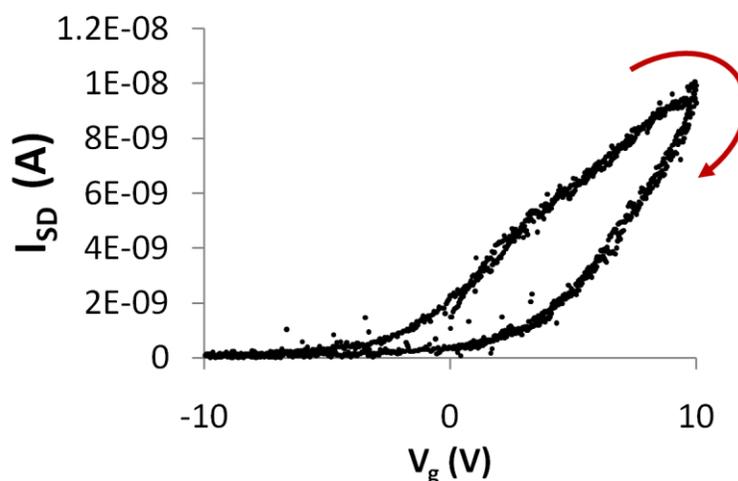


Figure 2: A typical transfer characteristic for one of our InAs NW-FETs. The large hysteresis is indicative of undesirable charging effects associated with this characterization method.

The large hysteresis indicates charging effects that may be the result of surface states, trap states, interface states and/or molecular adsorbates. Indeed, it is becoming evident in the literature that great care must be taken in the way of surface passivation, measurement parameters and environment to even yield reliable results for the field-effect mobility and carrier concentration.⁴⁻⁶ Therefore, alternative methods for characterization which enable *intrinsic* properties to be reliably extracted are certainly warranted.

Ideally a methodology for interrogating the intrinsic electrical properties of a NW should enable the wire to be probed when it is free of external perturbation, namely the substrate on which devices typically lie and molecules in the ambient, particularly at room temperature. For instance, it has been shown that suspended CNTs show distinctly

different transport behavior than those on a substrate.⁷ And the fact that certain quantum transport phenomena are only observed in suspended CNT devices further reveals the perturbing nature of the substrate.⁸⁻⁹ A method to circumvent these issues should not be fabrication intensive and it should allow the experimenter to choose specific NWs he or she may wish to measure, such as those of particular diameter or length. In our work, we have shown the feasibility of such a technique by using the *in situ* probing of vertically aligned NWs in an SEM using an electrical nanoprobe as will be discussed in detail in sections 2-4.¹⁰

Given many basic studies on CNTs, novel work in the field mainly focuses on more advanced devices than are often seen in NW work. Many times the behavior of these devices is fundamentally novel given the differences between CNTs and other semiconductor materials. Examples of this include determination of the NT bandgap using the leakage current and excitonic transitions¹¹ and the observation of multiple electron-hole pairs¹² in NT p-n junctions. Both studies employed electrostatic doping to form a p-n junction and the first also incorporated partially suspended NTs. Another study⁹ has taken the partially suspended NT structure further using three local gate electrodes and has shown tunable double quantum dots and Klein tunneling in NTs. Such studies are necessary for determining what role CNTs can and should play in future electrical and optoelectronic devices. Below we restrict the scope to Schottky and electrostatic p-n junction photodiodes which function under ambient conditions and show these devices exhibit unipolar short-circuit currents across the entire device by utilizing scanning photocurrent microscopy (SPCM). This result confirms the architecture is optimal for focused and flood lighting applications based on CNTs.

2 *In Situ Nanowire Measurement Platform*

2.1 GENERAL LAYOUT AND CONSIDERATIONS

The experimental setup for performing *in situ* electrical measurements on NWs is based on a Hitachi S4500 field FE-SEM which has been retrofit with two Kleindiek electronic “micromanipulators,” and a stage/sample holder which all may be electrically biased for electrical transport studies. The Kleindiek MM3A-EM manipulators each contain a kit which is designed to enable low-current measurement. In order to realize low current measurements, triaxial cabling is used from the source measure unit (SMU) to the vacuum feedthrough. From the vacuum feedthrough, shielding is maintained all the way to the sleeve which accepts the probe tip. Figure 3 generalizes a typical experiment using the system. The SMU contacts the heavily doped growth substrate, which serves as one electrode, via the sample holder. The NW is contacted at its tip by a W nanoprobe, the second electrode, which is held by the micromanipulator (not visible in the image). Cabling connects the micromanipulator/nanoprobe to the other terminal of the SMU to complete the circuit.

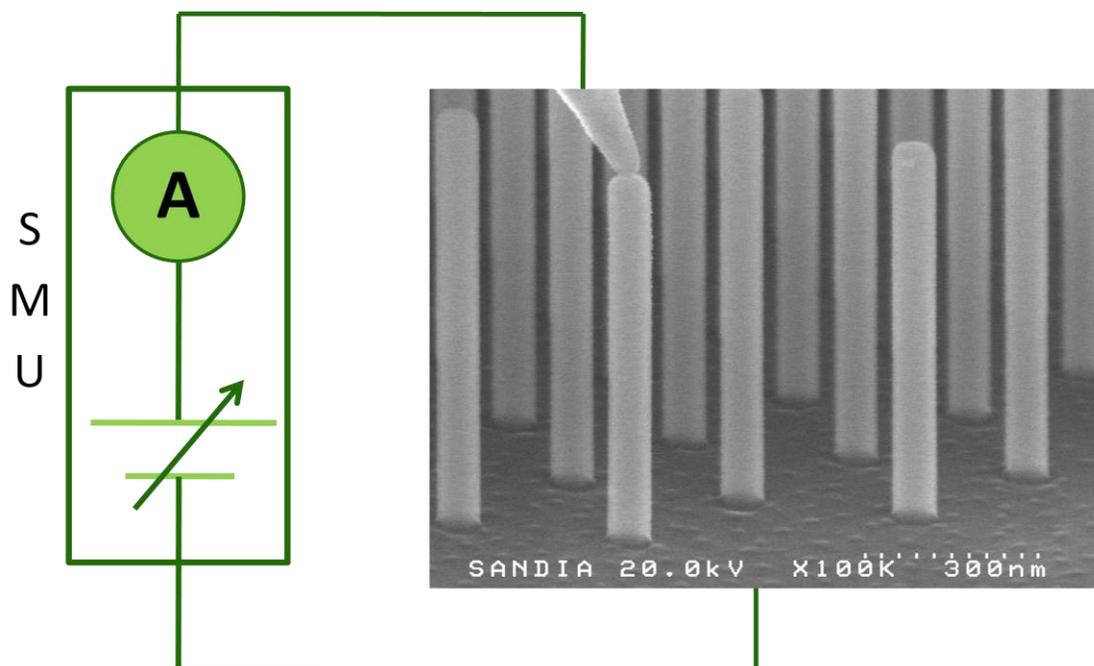


FIGURE 3: SEM micrograph incorporated into a schematic of the *in situ* measurement platform. A W nanoprobe and the heavily doped substrate serve as the electrodes in the NW transport measurements.

The SMU used here to affect the measurements is typically a Keithley 237. This series of SMUs utilizes triaxial guarding (i.e. distinct from shielding) to perform low current measurements. In guarding, the biased and ground connections are separated by a conducting layer (and the appropriate dielectric layers). In the case of a source voltage – measure current experiment, the middle conductor is biased at the same voltage as is used to affect the current through the circuit. In this way, leakage current through the dielectric is suppressed to a minimum in the cabling, whereas it would be maximal in the case of shielding. Using a coaxial connection heuristically validated the necessity of the triaxial cabling as resolution of the resolvable current deviated substantially from specified values of the equipment and was unacceptably poor in the limit of low current. The current resolution specified for the manipulators is 1 pA and < 1pA for the Keithley 237. Typically voltage sweeps are performed in a two-point probe configuration (i.e. a

voltage is applied, a current is measured, a new voltage is applied, a new current is measured, etc.). This results in a capacitive current effect that in practicality can limit the resolution of the experiment and the smallest measureable current onset value. The faster the sweep-rate of the voltage, the larger the current artifact will be. In practice we are able to resolve currents near the pA limit. Attaining this level of resolution however was particularly challenging in obtaining the results presented below on GaAs NWs; the high resolution and large voltage range necessary to observe the low-current regimes accurately resulted in requisite sweep times which were long enough to bring the temporal stability of the equipment into consideration. The absolute position in time of two to three apparatuses may impact the attainable duration and subsequently resolution of a measurement depending on the method of probing; this is particularly true when probing entities as small as NWs. By nature of design both the stage and the manipulators have inherent drift. Should both probes be used to contact a NW on an insulating substrate on the holder, drift of all three apparatuses may affect the measurement. In our published works we have measured vertically oriented NWs which grow from a conductive substrate. Therefore only the drift of the stage and one manipulator are of concern. The stage is positioned by joystick control of stepper motors using the Sprite system manufactured by Deben UK Limited. X and Y axis stage translation, and subsequently stage drift, is controlled by adjusting two potentiometers located at the back of the joystick unit. Numerous times, tuning of the potentiometers was necessary to successfully perform NW probing experiments; acceptable stage stability for even high resolution FE-SEM image acquisition is necessary but not

sufficient for NW probe studies. The MM3A-EMs are specified by Kleindiek to drift a maximum of 1 nm per minute.

The manipulators are driven by remote control of its piezos. Several speeds are available and motion ranges from macroscopic (10 mm/s) to beyond the resolution of a FE-SEM. On the finest setting, the resolution of movement is 2.5 Å. The manipulators are mounted to the ceiling of the SEM chamber and tip position would best be described in spherical coordinates. It is at first somewhat disconcerting that the tips must be driven in three dimensional space while viewing a two dimensional image on the SEM's monitor. Manipulating the focus on approach and utilizing shadowing effects are necessary in order to not damage the nanostructures or the probe tip. Manipulating the focus is necessary to avoid excessively long approach times and also because the fine scale settings of the manipulator have a notably limited range of motion, so it is not possible to focus on the substrate and bring the manipulator near from arbitrarily far away at the slowest speed. A good method was found where focus is set approximately halfway between the substrate and tip such that nothing is in focus. The tip is then lowered into focus and this is repeated until the tip is close enough to approach an in-focus substrate on the slow settings without reaching its end of travel. To land the tip on a nanostructure, one should utilize the "shadow" that is cast by the probe tip. As the tip nears a nanostructure, it prevents some secondary electrons emitted from the structure from reaching the detector; thusly, there is a darkening in the image. The shadow is maximized until the underlying structure is blocked by the tip and they are in contact. This should be performed with the highest resolution setting.

2.2 TIP ETCHING

For probe tips, a W wire is electrochemically etched in-house to nanoscopic dimension. The method is similar to protocols that have been developed for preparation of scanning tunneling microscopy (STM) tips; however the constraints differ dramatically. Whereas STM tips can be bulky and even misshapen so long as they have a single atom at the tip, tips in our case need not only be sharp but must be smooth and possess a sharp enough cone angle over a long enough distance to facilitate contact to only one NW at a time. It was found that even regularly shaped sharp tips produced by electrochemical etching in a bath of a solution are often not ideal for probing individual NWs. Such protocols typically involve using the W wire as the working electrode (anode) and a stable metal as the counter electrode (cathode). Typically no reference electrode is used. The electrodes are placed in a basic solution – 2M solutions of NaOH or KOH are typical. At suitable potential, the W wire is effectively oxidized and the oxidation product(s) dissolve as they are soluble in the basic solution. We typically use voltages > 3.5 V as this facilitates reasonable etch rates and is not prone to anisotropic etching of the tip seen at lower voltages. Lower voltages can yield sharp tips, though the tips are rough, resembling stalactites, and the process is unpredictable. The bath etching is performed to initially thin the W wire over suitable length. A secondary etch is then performed in a droplet of the electrolyte suspended in a small ring electrode [see Figure 4 a)] in the style of Guise et al.¹³ We modify the reported protocol however. Guise et al. lower the potential to .5 V and concentration of the KOH to 100 mM in the second etch step. We retain the > 3.5 V potential and 2M KOH concentration and observe sharp smooth tips. The etch is performed with a standard voltage source and monitored using

an ammeter for feedback. The etch is terminated as the current approaches but does not reach zero. Allowing the tip to etch until the current ceases results in blunt tips. Also, it is noted that the initial etch must suitably thin the W wire over a large aspect ratio (i.e. a length greater than the diameter of the droplet). Failure to do so precludes the use of current as an effective feedback mechanism for forming sharp tips as the signal is dominated by current corresponding to the bulk rather than the tip. Allowing the current to approach zero in a low aspect ratio wire also results in blunt tips. Figure 4 b) shows one of the sharpest W tips produced with our protocol. The nominal radius was ~ 20 nm, thinner than most NWs. In the image the edge of the NW behind the probe is easily visualized, showing the tip is partially electron transparent. Tips of such small radius were not used for transport measurements here to ensure efficient charge injection. Such thin tips may enable localized injection studies in the future however. Localized injection may be particularly relevant in assessing core-shell NWs for example which may be expected to contain two-dimensional electron gases at certain locations across the diameter.

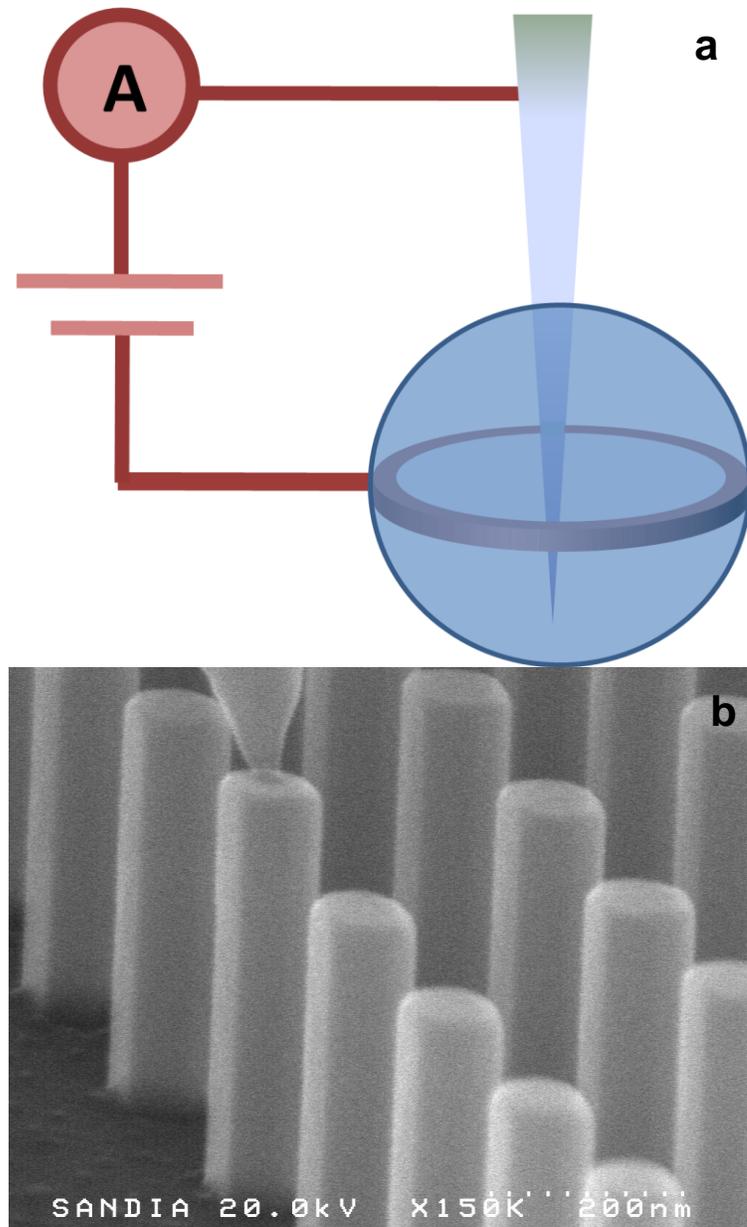


Figure 4: a) Schematic diagram of the electrochemical etching setup. b) Electron micrograph depicting one of the sharpest probes produced during this work contacting a GaAs NW.

2.3 ADVANCING CAPABILITIES

2.3.1 THE ELECTRON BEAM AS A PROBE

In addition to using the SEM as a tool for imaging or measurement, it is well known that the electron beam can be used as a probe for additional characterization.

Energy dispersive x-ray spectroscopy, Auger spectroscopy and cathodoluminescence are common examples of using the beam as a probe to obtain additional information.¹⁴ In the latter technique the beam is used for the creation of electron-hole pairs and the signal collected originates from their recombination. We shall use the beam to create electron-hole pairs, however, this will be performed in the context of a semiconductor device which has a built-in or applied potential and the signal collected will be electrical current. In this way the electron beam can be used in a manner analogous to a laser in photoconductivity-based studies.

Now we show measurements on bulk Si samples which helped elucidate the improved efficiency in Cu contaminated radial p-n junction solar cells over planar structures.¹⁵ The technique used is that of electron beam induced current (EBIC) measurements. For a device containing a built-in potential, the beam can be scanned across the sample creating electron-hole pairs. Pairs at, or diffusing to, the depleted region can be split and a short circuit current collected. This collected current takes the form

$$I = I_0 e^{-x/L_D}, \quad (4)$$

Where I_0 is a constant, x is the distance from the junction, and L_D is the diffusion length of the minority charge carrier. A fit to the data enables one to readily extract the diffusion length from such a measurement. Figure 5 shows EBIC measurements and curve fits superimposed onto secondary electron micrographs. The straight line indicates where the electron beam was scanned across the sample. The W probe tip provides a Schottky contact to the p-type Si samples and Ohmic contact is made through the

backside of the wafer using In. The Ohmic nature of this interface was affirmed by probing across two such back contacts.

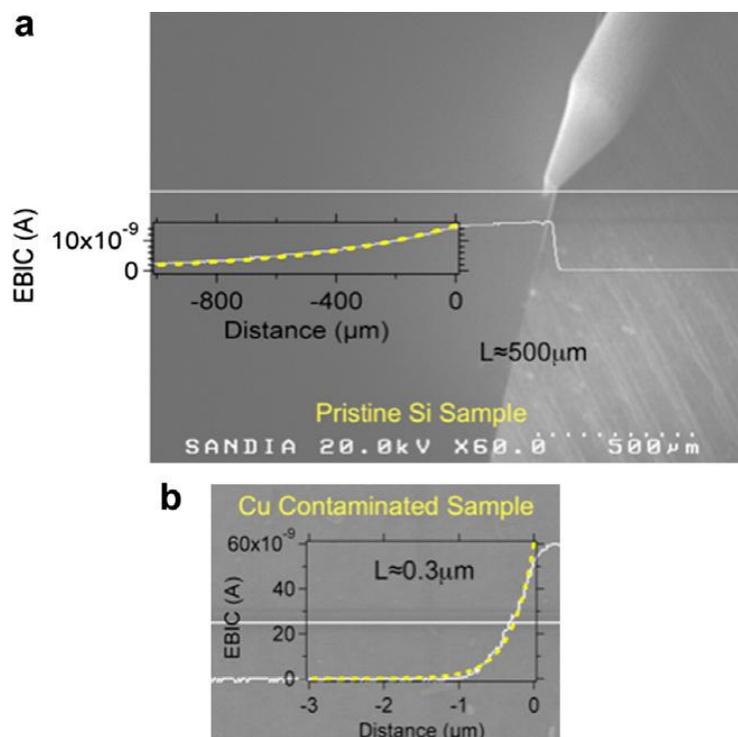


FIGURE 5: EBIC experiments to quantitatively discern the difference between minority carrier diffusion length in a) clean and b) Cu contaminated Si. A dramatic reduction in diffusion length in relatively impure materials supports the notion that properly designed radial p-n junction solar cells lead to improved efficiency over their planar counterparts.

Figure 5 a) gives the result of probing a “clean” Si sample. The fit of the data indicates that the electron diffusion length in the material is $\approx 500 \mu\text{m}$. As one might expect, contamination from additional impurities could hinder diffusion of the species and this is confirmed in Figure 5 b). Once Cu contamination has been introduced in the sample, the electron diffusion length is measured to decrease by three orders of magnitude, to $\approx 300 \text{ nm}$. This short diffusion length shows why radial core/shell p-n junctions of certain micro and nanoscopic dimensions showed improvement over planar solar cells and why additional scaling did not result in a monotonic efficiency trend. In Chapter 4 we show

that the beam serves as a powerful probe for directly analyzing semiconductor NW systems as well.

2.3.2 REAL-TIME MOVIE CAPTURE OF EXPERIMENT

Certain experiments carried out in the SEM were observed to be of a temporally critical nature such that the experiment could not be halted, an image collected, the experiment resumed, and so on. Complete continuity of some experiments is sometimes simply necessary. This makes it difficult to most accurately report and convey such experiments to collaborators and the scientific community. This in addition to the policy of many publishers to now host multimedia files which supplement a publication made it worthwhile to augment the SEM's capabilities to include real-time movie capture. Real-time viewing of the experiment was available only on the panel monitors and this is delivered as an analog signal; thusly, it cannot be immediately collected by a computer. A commercial analog to digital converter was connected to an auxiliary video output of the instrument and interfaced to a computer for time-resolved monitoring of experiments. The time resolution cannot exceed the resolution of the scanning rate or that of the converter, however, sufficiently slowly evolving experiments are readily captured. Such a capability proved useful in monitoring the thermal failure of InAs NWs by Joule heating for the work presented in the following chapter. Figure 6 shows a sequence of still frames taken from such a movie. The chronology is indicated by the arrow in the figure. The full movie is hosted at <http://ieeexplore.ieee.org> as supplemental material for reference [16].

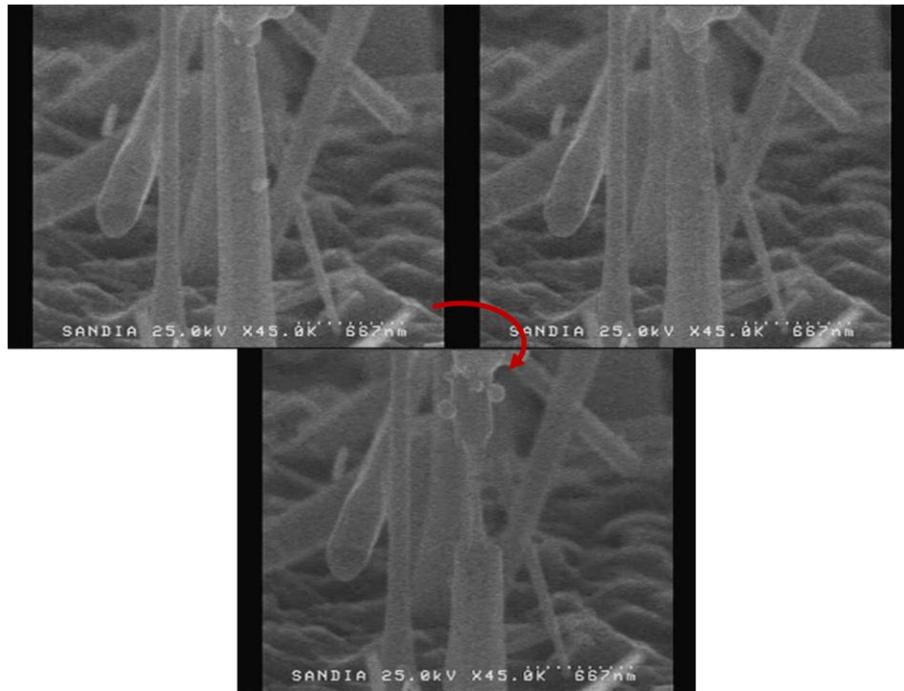


FIGURE 6: Still frames from a movie recorded during the induced failure of an InAs NW by Joule heating.

3 Individual Indium Arsenide Nanowire Characterization

3.1 Introduction

Semiconductor nanowires (NWs) continue to fascinate researchers, promising control over dimensions, crystallinity and composition during the nanostructure synthesis, as well as interesting basic transport properties and potential applications in electronic, optoelectronic, and thermoelectric devices. As discussed in the introduction, in order for these nanostructures to have technological impact, their basic electrical characteristics have to be measured accurately and reproducibly; however, bulk techniques such as Hall measurements cannot be easily¹⁷ implemented with NWs due to the small dimensions.

Characteristic nanowire parameters such as carrier type, concentration and mobility are thus frequently determined from the transfer characteristics of NW-FETs.¹ The results, however, can be strongly affected by the nanowire and the dielectric/nanowire surface and interface states.^{6,4} For example, Dayeh et al. found that the transconductance in top-gated InAs NWFETs is dependent on the sweep-rate of the gate voltage and that the hysteresis in the transfer characteristic is only removed by creating a charge-neutral interface via a slow sweep-rate.⁵ This naturally leads to a dependence of the extracted carrier concentration and mobility on the experimental conditions, with the extracted mobility varying by up to an order of magnitude. Thus, alternative characterization techniques free of perturbing interfaces would be valuable to measure the intrinsic properties of NWs.

Here,¹⁶ we discuss the electrical characterization of VLS (vapor-liquid-solid) grown InAs NWs using such a technique. We contact individual, free-standing NWs directly on their growth substrate using the electronic nanoprobe retrofitted inside of a FE-SEM as shown in Figure 7 a). The W probe serves as one contact and the heavily doped growth substrate serves as the other. Using this technique, we show that the electrical transport in these InAs NWs is space-charge-limited (SCL), a bulk transport regime that arises when the charge injection at the contacts is efficient. Using recently developed theory specific to SCL transport in NWs,¹⁸ we show how one can extract the mobility and effective carrier concentration from I-V measurements indicative of SCL current. By controllably inducing failure by Joule heating, we show that electrical transport is dominated by the bulk of the NW instead of the contacts, a further indication of SCL transport. The two-point probe method we employ¹⁰ is performed *in vacuo* on free-

standing wires thus diminishing the electrical and thermal influence of molecular adsorbates and the substrate on which NW devices typically lie.

3.2 SYNTHESIS

Non-intentionally-doped InAs NWs were grown on a degenerately Si-doped GaAs(111)B substrate. The substrate was coated with a 1 nm thick Au layer by ex-situ electron beam evaporation, and subsequently inserted into the chemical vapor deposition (CVD) reactor. In the growth chamber, the template was annealed for 10 min in arsine (AsH_3) ambient at 650°C and then cooled to 400°C for growth. The NWs were grown by low-pressure (60 Torr) metal-organic CVD using AsH_3 and trimethyl indium (TMIn) with the Au serving as the collector for the VLS mechanism. The growth occurred for 10 min using a TMIn partial pressure of 2.42 mTorr and an AsH_3 partial pressure of 0.336 Torr giving a V-III ratio of 140. The resulting NWs have diameters between 30 and 300 nm and lengths often exceeding 10 μm . Planar growth rates under these conditions were below 0.04 $\mu\text{m}/\text{min}$. Transmission electron microscope (TEM) images [Figure 7 b)] and selective area electron diffraction (SAED) [Figure 7 c)] indicate that the wires are primarily wurtzite (WZ), are covered by ~ 2 nm native oxide, and contain a number of stacking faults (SFs) and thin zinc-blende (ZB) regions. The WZ structure with SFs and ZB regions is commonly observed in III-V NWs grown on 111(B) substrates. Growth conditions and the VLS mechanism make it energetically favorable for the WZ phase to occur.¹⁹

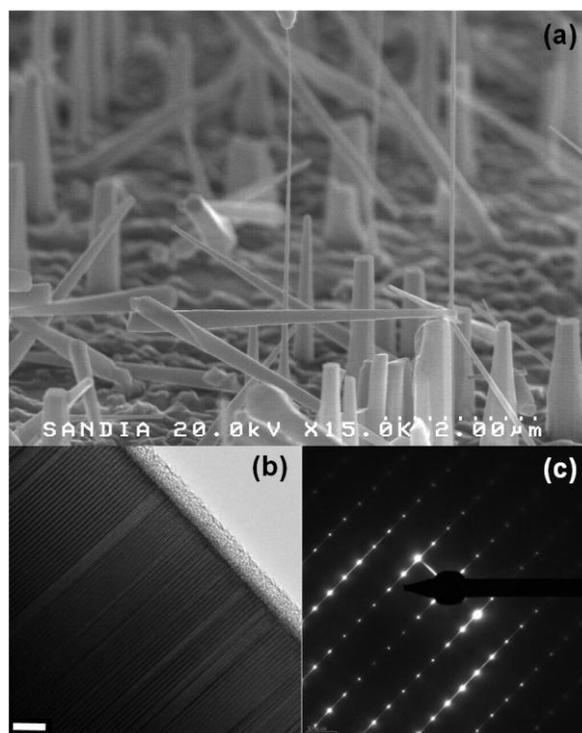


FIGURE 7: a) FE-SEM micrograph depicting a typical I-V measurement. In the center of the image, a W nanoprobe contacts a free-standing NW at its tip. The degenerately-doped substrate serves as the second electrode. b) TEM image indicating WZ (dark) and ZB (light) regions (scale bar is 5 nm). c) Electron diffraction pattern of a typical WZ region.

3.3 SPACE-CHARGE-LIMITED TRANSPORT

Figure 8 a) displays representative I-V characteristics for three NWs of different dimensions. The curves are non-linear, with symmetric behavior between positive and negative voltage polarities. Such I-V curves are often reported in the characterization of NWs using lithographically-defined contacts, and are usually attributed to the presence of symmetric back-to-back Schottky or tunnel barriers at the contacts. However, in the present measurements the contacts are very dissimilar, and yet the curves are symmetric. Moreover, plots of I/V vs V show that in addition to the small bias Ohmic regime, there is a strong quadratic $I \propto V^2$ dependence on voltage, as shown in Figure 8 b), and we

attribute this behavior to space-charge limited (SCL) transport as was recently modeled and measured for GaN NWs.¹⁸ SCL transport can be dramatically enhanced in NWs due to poor electrostatic screening. That is, the current density J is given by

$$J = \zeta \left(\frac{R}{L} \right) \frac{\epsilon \mu}{L^3} V^2 \quad (5)$$

where $\zeta(R/L)$ is a scaling factor which depends on the aspect ratio of the NW. In the limit $R/L \ll 1$ appropriate for the NWs included in this study,

$$\zeta \left(\frac{R}{L} \right) = \zeta_0 \left(\frac{R}{L} \right)^{-2} \quad (6)$$

where ζ_0 is a numerical constant of order unity.²⁰ For high aspect-ratio wires, the scaling factor induces a strong deviation from the bulk current density for which $\zeta = 9/8$.

Solving for the mobility of a high aspect-ratio NW in the SCL transport regime μ_{SCL} , gives

$$\mu_{SCL} = \frac{IL}{V^2 \pi \epsilon} \quad (7)$$

where ϵ is the permittivity of InAs.

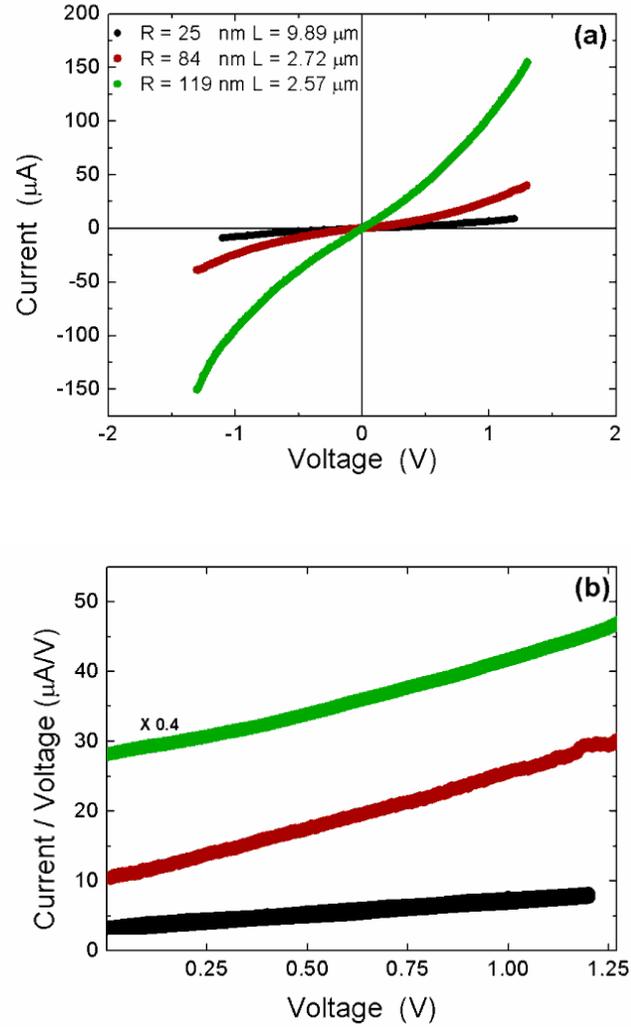


FIGURE 8: a) Current as a function of voltage for three representative NWs of different dimensions showing symmetric, non-linear, non-exponential behavior. b) Plots of current/voltage as a function of voltage for the wires shown in a).

The mobility can thus be extracted directly from the SCL regime of a 2 point probe I-V measurement, in addition to the linear Ohmic regime at small bias. The cross-over voltage, V_c , where the Ohmic, $J = n_{eff} e \mu L^{-1} V$, and SCL current, Eq. (1), are equal allows extraction of the effective carrier concentration:

$$n_{eff} = \frac{V_c \epsilon}{e R^2}. \quad (8)$$

Plotting I/V as a function of V , as shown in Figure 8 b), yields a straight line for SCL behavior and allows one to extract the Ohmic (y-intercept) and the SCL (slope) current contributions. The length and radius of the wires were determined from high resolution FE-SEM micrographs. Figure 9 a) displays n_{eff} as a function of NW radius indicating that the effective carrier concentration increases with decreasing diameter. The trend is well fit by a power law behavior which shows that $n_{eff} \propto R^{-2}$. In general, the effective carrier concentration is expected to increase with decreasing radius because the InAs surface is inverted with a high density of surface charge.²¹⁻²³ The thickness of the surface layer has been reported to be around

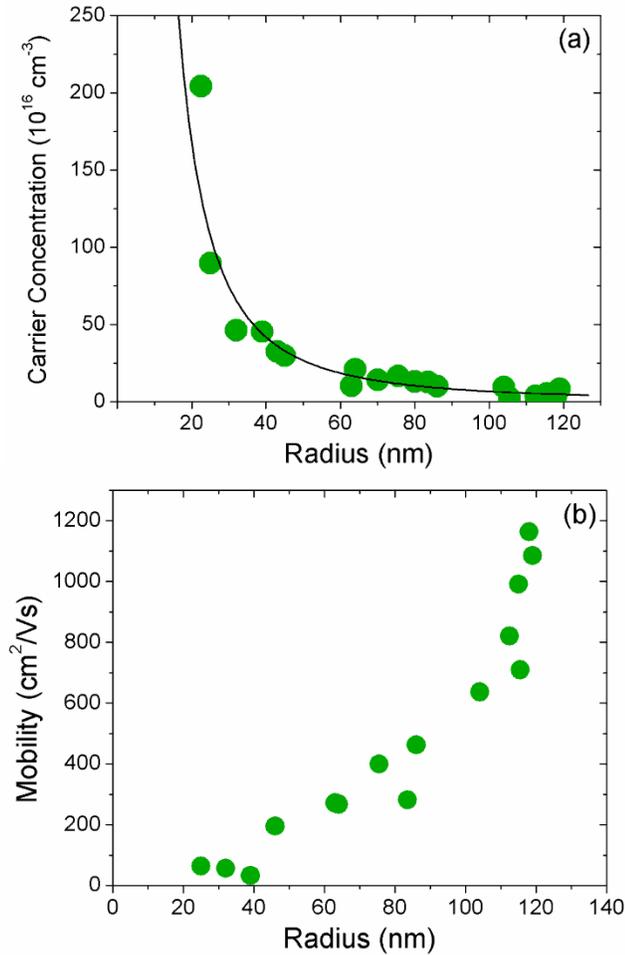


FIGURE 9 a) Effective carrier concentration and b) mobility plotted as a function of radius. Carrier concentration depends inversely on NW cross-sectional area and mobility is proportional to the radius in thin wires.

$t \approx 10 \text{ nm}$,²⁴ leading to a volume density on the order of 10^{18} cm^{-3} . As the nanowire radius decreases, this surface layer becomes more important, leading to an increase of the effective carrier concentration. From a surface to volume argument, this leads to a $n_{\text{eff}} \propto R^{-1}$ dependence; however, it is known that band-bending distances depend on nanowire radius²⁵ so we also expect t to increase with decreasing nanowire radius. These two factors together may explain the rapid increase of the effective carrier concentration with decreasing radius that we observe experimentally. The mobility as a function of

radius is given in Figure 9 b), and shows an increase with increasing nanowire diameter. This trend in mobility as a function of radius is consistent with that observed by Ford et al.²⁶ in small diameter wires. In general, the values we find for mobility and carrier concentration are in agreement with the findings of other groups investigating transport in InAs NWs²⁷⁻²⁹ including one study dealing specifically with WZ/ZB NWs similar to our own.³⁰ The main source of scatter in the extracted values is most likely due to the different stacking fault density and arrangement from wire to wire.

3.4 THERMAL AND CONTACT ANALYSIS VIA JOULE HEATING

Since the non-linear, symmetric I-V curves of Figure 8 a) are often ascribed to contacts, we sought an additional test to show that the I-V curves were predominantly determined by the transport in the NW itself. Thus, we intentionally Joule-heated NWs to their maximum temperature (i.e. thermal breakdown) in order to determine the location of failure. For a contact-dominated situation, this point would be close to the contacts since this is where the greatest voltage drop would occur. In contrast, for transport dominated by the NW itself, this point should be close to the midpoint between the two contacts. Figure 10 a) shows a SEM image of an InAs NW after breakdown, clearly indicating failure in the middle of the NW. This result confirms the presence of low resistance contacts³¹ and that the transport characteristics are determined by the NW. We carried out similar in-situ failure experiments on a number of NWs of different dimensions, recording the current and voltage at breakdown. (A movie of one of the Joule failure experiments is available as supplementary downloadable material at <http://ieeexplore.ieee.org>.) The temperature profile in the NWs was estimated using a 1-dimensional heat flow model.³² The model assumes that the temperature distribution in

the NW depends only on the axial coordinate, a condition that is appropriate in our case given that the wires are freestanding in vacuum, with little heat flow to the environment. Under this condition, the temperature distribution is the same as that in a bulk material. For two ends held at temperature T_0 , the temperature profile is given by

$$T(z) = T_0 + \frac{q}{2\kappa} z(L-z) \quad (9)$$

where z is the axial coordinate, q is the heat generation rate, L is the length of the wire, and κ is the thermal conductivity. Within this model, the maximum temperature is reached at the point $z = L/2$, i.e. at the midpoint between the two contacts, as observed in our experiments. By equating the heat generation rate with the electrical power delivered to the wire, the maximum temperature is

$$T_{\max} = \frac{IVL}{8\kappa\pi R^2}. \quad (10)$$

We used this equation to extract the thermal conductivity of NWs of different radii and length by measuring the current and voltage at which the NWs breakdown, and equating T_{\max} to 793 K, a temperature known to result in the desorption of the native oxide.³³⁻³⁴ Assuming that the NW failure is initiated at 793 K,³⁵ the thermal conductivity is plotted for NWs as a function of their radius in Figure 10 b). The average thermal conductivity extracted from the failure measurements is 8.35 W/mK, about 1/3rd the value of high quality bulk InAs. This result is in accord with the large density of stacking faults present in these NWs, as it is well-known that structural defects, including stacking faults, cause increased phonon scattering.³⁶

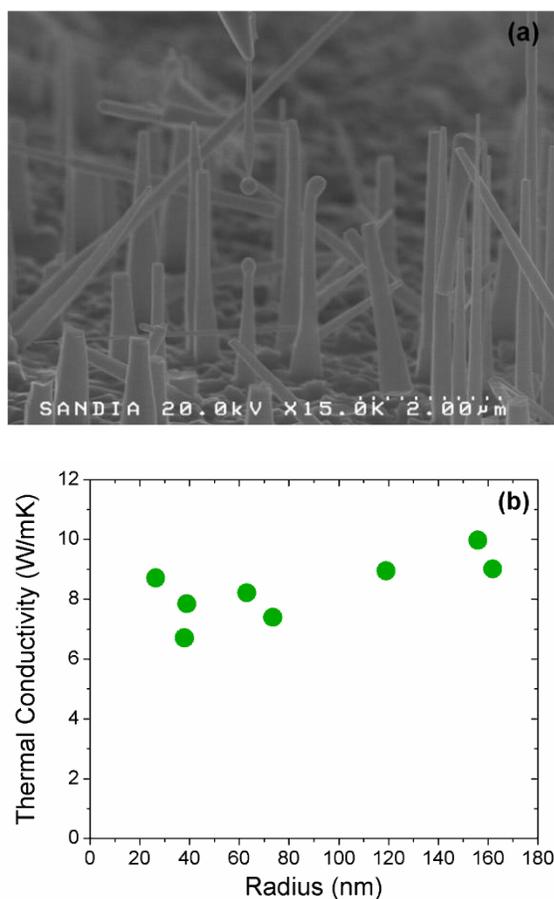


FIGURE 10 Panel a) shows a SEM image of an InAs NW after breakdown by Joule heating. b) Thermal conductivity as a function of NW radius extracted from the breakdown experiments.

3.5 SUMMARY

We have presented a two-point probe method for electrical characterization of NWs which does not rely on the FET geometry. When applied to InAs NWs, the measurements suggest that space-charge-limited current is the dominant transport mechanism. For our InAs NWs an inverse relationship was found between carrier concentration and NW cross-sectional area while carrier mobility was found to increase with NW radius. Thermal breakdown measurements suggest a suppression of the thermal conductivity with respect to bulk which may be a result of numerous stacking faults along

the length of the wires. These results indicate that dimensionality effects govern the electrical behavior of InAs NWs even at radii as large as 100 nm.

4 Individual Gallium Arsenide Nanowire Characterization

4.1 INTRODUCTION

As stated in the main introduction there are many materials and techniques with which to grow NWs. A major task then is identifying the particular charge transport phenomena that dominate in a given nanowire system. This is important not only to take advantage of the transport physics for device engineering, but also to correlate electronic transport with basic materials issues. In chapter 3 we saw that InAs NWs have charge accumulation rather than depletion at the surface rendering them easy to contact Ohmically; however this “doping” was not enough to fully screen the injected charge suggesting that substitutional doping would be required to realize fully Ohmic devices.

Additionally, measurement and theory have recently revealed many different transport regimes and effects. Examples of this include Ohmic transport for Si NWs,³⁷⁻³⁹ space-charge-limited current in GaN,¹⁸ InAs,¹⁶ CdS⁴⁰ and trap-containing GaAs NWs,⁴¹ recombination current in Au-catalyst/Ge NW Schottky diodes,⁴² ballistic and diffusive transport in InAs NWs⁴³ and size-dependent mobility^{16, 26} and carrier concentration¹⁶ in InAs NWs. Here we show that yet other transport regimes, Poole-Frenkel and phonon-assisted tunneling, arise in GaAs NWs by utilizing *in situ* nanoprobings of individual

nanowires directly on the growth substrate.⁴⁴ These regimes arise due to the presence of traps along the length of the NWs, as confirmed by a novel characterization technique.

4.2 SYNTHESIS

The vertically aligned NWs used in this study were grown by catalyst-free metal-organic chemical vapor deposition (MOCVD) on a degenerately doped (n^{++}) GaAs (111)B wafer coated with a SiO₂ template. E-beam lithography was used to create arrays of holes in the SiO₂, which determined NW diameter. The wires were grown at 700°C for 10 minutes with a V-III ratio of 10, using *tert*-butylarsine and trimethylgallium precursors in hydrogen carrier gas at a total reactor pressure of 60 Torr. The nanowires were doped n-type with Si; a bulk sample grown under these conditions contained a Si concentration of $7 \cdot 10^{18}/\text{cm}^3$, and exhibited linear current-voltage characteristics with a resistivity of $\sim 10^3$ A/V-cm.

4.3 CARRIER TRANSPORT

Figure 11 a) depicts a typical measurement and Figure 11 b) shows a representative I-V characteristic for NWs in this study. Attention is called to the high turn-on voltage of several tens of volts and its symmetry between polarities. This behavior is indicative of electronic transport limited by processes along the length of the NW, as opposed to contact effects, since the latter are asymmetric. Indeed one expects an Ohmic contact at the substrate/NW interface given dopant type and concentration and a Schottky contact at the NW/W probe interface given that defects commonly pin metal Fermi levels near mid-bandgap in GaAs.⁴⁵ Thus, if the transport was injection-limited, a strong asymmetry in the I-V characteristic between polarities would be observed with a turn on voltage at

forward bias given by $E_g/2e \approx 0.72V$, where E_g is the bandgap of GaAs. The fact that the data does not follow this picture implies that the transport is dominated by the bulk of the nanowire. (We show below that the *injection-limited* nature of the system, once revealed, is consistent with this picture.)

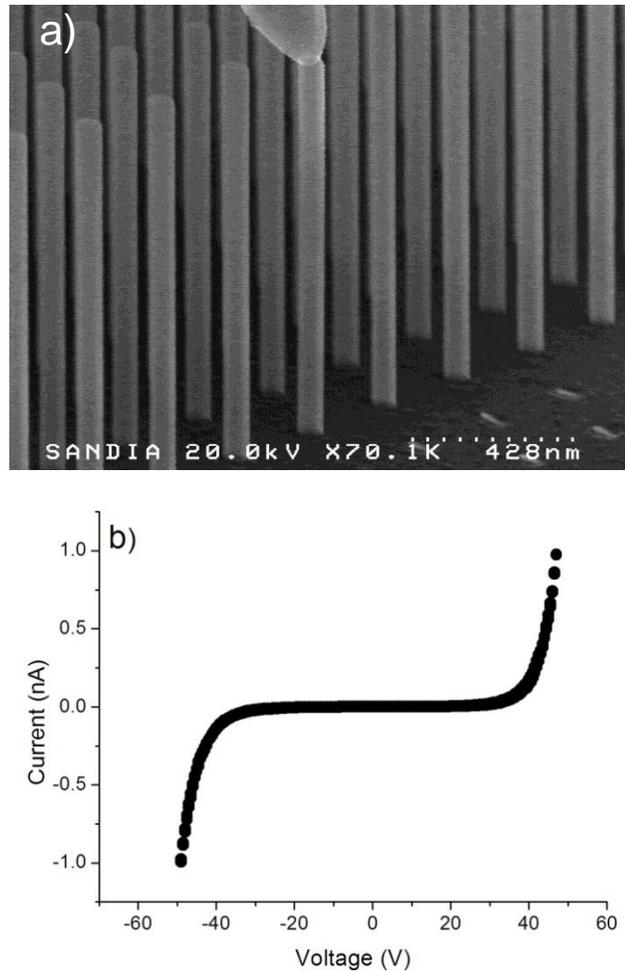


FIGURE 11 a) FE-SEM micrograph depicting a typical *in situ* electrical measurement. b) A representative I-V curve. The e-beam is directed away from the NW during measurement unless otherwise specified.

The large electric fields required to observe relatively small currents are quantitatively consistent with concepts of trap-dominated transport. Indeed Frenkel showed that in a semiconductor or insulator, carrier traps, which are charged when empty and neutral

when filled, can mediate carrier transport and give rise to a pre-breakdown phenomenon in which the increase in conductivity is exponentially proportional to the square root of the electric field.⁴⁶ This relationship arises as the applied field lowers the barrier of the trap Coulombic potential, thus enhancing thermionic emission over the trap barrier. This model has been reworked in order to account for experimental results;⁴⁷⁻⁴⁸ however, we find that our GaAs NWs are well described by the classical, one-dimensional model in which:⁴⁷

$$\sigma \propto \exp\left(\frac{e^3 E}{\pi \varepsilon (kT)^2}\right)^{1/2}, \quad (11)$$

where σ is the conductivity, E is the electric field, ε is the dielectric constant, k is the Boltzmann constant, and T is the temperature. Figure 12 a) shows data for the NWs plotted at forward and reverse bias under this formalism along with linear fits. (The coefficient of determination in each instance was $\geq 99.3\%$. Fits to other power laws gave nonphysical values of ε .)

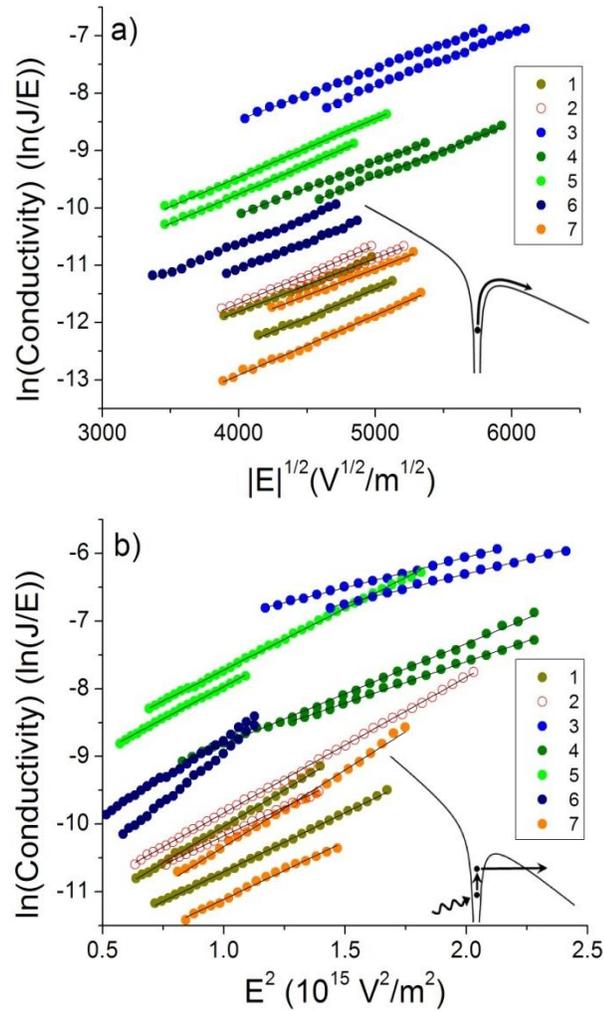


FIGURE 12 a) Intermediate-field and b) high-field data plotted respectively in the formalisms of Poole-Frenkel effect and phonon-assisted tunneling. The insets schematically depict carrier escape from the trap in each regime. The voltage range over which a transport mechanism was observed in a given NW can be obtained using the NW lengths in Table 1.

The linearization of the data indicates that the conductivity is indeed exponentially dependent on $E^{1/2}$ in this intermediate field regime. Schottky emission would also be linearized in such a plot, so care must be taken in ascribing the appropriate mechanism in the absence of other indicators such as that discussed above. Discrimination between the two effects is provided by analyzing the slope of the lines (lower by a factor of 2 for Schottky emission) which typically enables one to extract a sensible value for the

dielectric constant under the correct formulation.⁴⁸ Using the Poole-Frenkel formulation we find the nanowires to have dielectric constants near that of bulk GaAs which further affirms bulk-limited transport and the linear fits in Figure 12. The dielectric constant values extracted for all wires in this study at forward and reverse bias are given in Table 1 as are the NW dimensions.

Table 1: NW Characterization Values

Wire	R (nm)	L (μm)	ϵ_{r+}	ϵ_{r-}	τ_+ (fsec)	τ_- (fsec)
1	33	0.99	10.7	9.08	11.7	11.1
2	40	1.032	8.83	10.6	11.6	10.9
3	42	0.672	11.6	10.2	8.77	8.68
4	38	0.712	10.5	10.5	10.4	9.71
5	41	1.05	8.65	8.48	11.1	11.3
6	42	1.013	10.1	10.3	13	12
7	43	0.865	10.5	8.32	12	10.9

With application of increasingly higher electric field, a competitive transport mechanism emerges as a result of field-induced thinning of the trap energy barrier. Rather than being fully emitted over the barrier, it becomes more probable for a carrier to absorb a lesser amount of energy from phonons and subsequently tunnel through the trap

barrier. This mechanism, aptly named phonon-assisted tunneling results in a conductivity increase described by:⁴⁹

$$\sigma \propto \exp\left(\frac{(eE)^2 \tau^3}{3m^* \hbar}\right), \quad (12)$$

where τ is the tunneling time and m^* the effective carrier mass. The hallmark of this transport mechanism is that conductivity increases exponentially with the square of the applied electric field. Increasing the applied field beyond values where Poole-Frenkel transport is applicable, in all cases resulted in plots that become superlinear in the Poole-Frenkel formulation. We plot this high field region of the datasets in the formalism of phonon-assisted tunneling as represented in Figure 12 b). Again, data from forward and reverse bias regions are shown. The data are well linearized, indicating that at relatively high fields carriers traverse the NW via phonon-assisted tunneling events. The slope of the line enables determination of the tunneling time and these values are listed for each wire in forward and reverse bias in table 1. (We used the GaAs bulk effective carrier mass of $0.067m_0$.) The tunneling time predicted from theory,

$$\tau = \frac{\hbar}{2kT} \pm \tau', \quad (13)$$

is increased or decreased from a value determined entirely by fundamental constants and reciprocal temperature by τ' depending on the nature of the traps in the material (i.e. whether the traps facilitate weak or strong electron-phonon coupling, respectively).⁵⁰ In all NWs we observe similar tunneling times which are near and less than $\hbar/2kT = 13$ femtoseconds, consistent with strong electron-phonon coupling and indicating the traps are autolocalized centers.⁵¹ An affirmation and consequence of this are discussed below.

(Determining the exact nature of the traps is beyond the scope of this paper, requiring detailed analysis using, e.g. Deep-Level Transient Spectroscopy. Two possible candidates are the EL2 level and DX centers, both of which have been determined to be self-trapping in GaAs.⁵²⁻⁵⁵)

4.4 CHARACTERIZATION OF CONTACTS

Finally to confirm that traps dominate the transport and to reveal the nature of the contacts we employ a novel characterization technique – electroconductivity measurements - in conjunction with the well known electron beam induced current (EBIC)⁵⁶ technique. In EBIC a focused electron beam is rastered over the semiconductor and the created electron-hole pairs which diffuse to a built-in potential (e.g. p-n junction or Schottky contact) are separated and used to generate a spatial current profile or an EBIC image in which the contrast directly corresponds to the collected current. Figure 13 a) shows a representative EBIC profile collected as the beam is rastered along the length of a NW. Net current is only collected in the vicinity of the built-in potential formed by the W contact. The trough (as opposed to a peak) in the profile indicates that a hole current was collected at the W tip (and an electron current at the substrate). The lack of net current collection when the beam is near the substrate/NW interface indicates Ohmic contact. Therefore the EBIC profile affirms the asymmetry of the contacts and the injection-limited nature of the system when traps are activated.

Complementarily, rather than rastering the beam with the device at fixed (zero or reverse) bias we focus it to a point on the NW and perform a I-V sweep. This technique allows us to probe the response of the system when free carriers are made available and quantitatively determine the Schottky barrier height (i.e. the applied voltage for which the

net current is nullified). Figure 13 b) shows a I-V curve recorded during such an electroconductivity experiment. The I-V curve is strongly asymmetric, with a turn-on voltage at forward bias less than 1V, consistent with the contact being pinned at mid-bandgap. The measured beam current at the sample (10 pA at +70 V bias of the collector) cannot account for this substantial change in behavior during e-beam exposure; the increased current is the result of the creation of multiple carriers per injected e-beam electron.⁵⁶

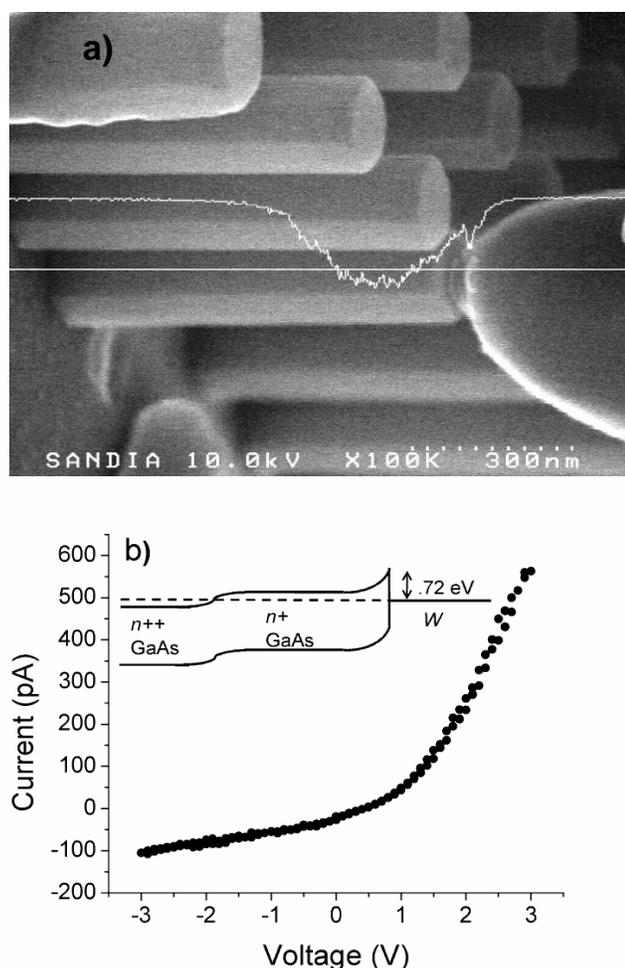


FIGURE 13 a) An EBIC profile (at zero applied bias) superimposed on the secondary electron image. The straight line shows the trajectory of the e-beam scan along the length of the NW and the corresponding current profile indicates net current is collected only near the NW/tip interface. The acceleration energy and beam current were 10 keV and 10 pA respectively. b) A typical I-V curve obtained from an electroconductivity experiment. The electron beam was focused laterally in the center of the NW, 100 nm away from the W probe tip. The acceleration energy was 15 keV and the beam current, 10 pA. The creation of carriers reveals a low turn-on voltage and strong asymmetry. The expected band diagram at equilibrium is given in the inset.

I-V curves taken after electroconductivity experiments, with the e-beam off, revert back to the trap-dominated transport behavior after several hours, which indicates the NWs were not damaged. While the electroconductivity diminished over time, it was still clearly identifiable even ~ 1 hour after e-beam exposure. This effect is not unique to e-beam excitation of carriers but is rather a consequence of the autolocalized centers we

revealed above through analysis of the phonon-assisted tunneling transport. Persistent current has often been observed in the context of photoconductivity experiments and results from metastable states in which re-trapping is hindered by an energy barrier.⁵⁷

4.5 SUMMARY

In summary, we have shown that the semi-insulating electrical characteristic of catalyst-free MOCVD grown GaAs NWs is the result of trap-mediated carrier transport within the material. At intermediate electric fields Poole-Frenkel transport dominates crossing over to phonon-assisted tunneling at larger fields. By analyzing the phonon-assisted tunneling regime, we extracted the tunneling time, which enabled us to determine that the traps are autolocalized centers. Through electron-beam excitation techniques we confirmed the injection-limited nature of the system when traps are activated, thus revealing the nature of the contacts. The presence of traps in MOCVD-grown GaAs nanowires in conjunction with those previously observed in solution-grown material,⁴¹ indicates that defects play a key role in this material system. Why would defects be more important in nanowires compared to thin films? One possibility is that surface states, which are known to be present at GaAs surfaces,⁵⁸ deplete the carriers in the nanowire thus enabling even modest trap densities to affect the transport.

5 Optoelectronic Characterization Platform

5.1 INTRODUCTION

In addition to electrical characterization methods such as those shown above, optical techniques have proven indispensable in the characterization of semiconducting materials. However techniques which were developed for bulk materials are not always directly applicable for nanostructures as they often lack spatial resolution. Below we show how the confluence of highly focused laser light and a scanning stage with nanoscopic resolution enables optoelectronic characterization – specifically, localized PC mapping – of NWs and NTs

5.2 AMBIENT PROBATION WITH FIXED LASER LINES/SCANNING STAGE.

5.2.1 INITIAL ELECTRICAL CHARACTERIZATION

The initial electrical characterization at this probe station is performed using a National Instruments model 6229 data acquisition (DAQ) board preceded by a current preamplifier (DL Instruments model 1211). The data collection is facilitated remotely by the so-called meaSureit.vi LabVIEW program available as shareware. Fixed gate, swept source-drain voltage and swept gate, fixed source-drain voltage measurements are routinely performed to assess device transport and transconductance, respectively to assess devices prior to optical investigation.

5.2.2 PROBATION SPECIFICS

SPCM of nanostructured devices is a currently evolving field despite the introduction of the concept in the 1970s. It was described by Lang and Henry of Bell

Laboratories as long ago as 1977 in order to study bulk devices.⁵⁹ Literature review suggests the technique has remained fairly dormant however until its renaissance within the last decade which is bringing resolution capabilities suitable for interrogating nanoscopic materials and/or regions, and resolving potential profiles. The initial papers, including the intimately related scanning photovoltage microscopy, employed adjustable mirrors to steer the laser beam in the experiment and few details regarding the resolution were provided. Current implementations involve scanning a translational stage, rather than the incident beam by mirror. This has the potential to confer greater uniformity in the experiment as the beam path remains constant as opposed to addressing the surface at progressively oblique angles as in a mirror guided beam experiment. Modern actuators, particularly those which are piezoelectric, offer nanoscopic step resolution.

The experiments described here were performed on a modified Olympus MX40 microscope (originally modified at the column to accept laser light). The microscope is manufactured to accommodate long working-distance objective lenses as are preferred or required for probing devices. One of the most crucial modifications was the replacement of the manual X-Y stage with a translational stage comprised of two independent Newport 850F actuators mounted orthogonally to one another. The original mechanical Z axis for adjusting focus is retained and contains a lock. Addition of a custom stage support was found to be essential in maintaining focus for high resolution experiments. The electronically addressable actuators are DC motors with a resolution of 50 nm/step. These actuators offer a good compromise between resolution and travel distance enabling the probe station to be fully functional for finding devices formed from stochastic processes as well as a suitable resolution SPCM station. The maximum travel distance is

50 mm in each direction. The drive mechanism is based on a leadscrew which has a pitch that corresponds to 50 nm of travel per encoder spacing. The encoder is comprised of a light source, a linear grid of holes, and a photodetector.

The driver for the actuators is a MM3000 motion controller also manufactured by Newport. The MM3000 offers sophisticated control over the actuators and is most easily addressed via computer. LabVIEW programs are used to control scanning and adjust settings via the IEEE488 interface. The controller uses a proportional, integral, differential (PID) gain factor closed loop control, the settings of which are reasonably well selected by the manufacturer for the task of SPCM. There is no feedback mechanism for resolving the absolute position of the stage however despite knowing the absolute position according to encoder counts. This is perhaps the most insidious and challenging aspect in regards to obtaining a scan in which one is certain of the registry on the nanoscale. In fact, through the course of this dissertation it was realized that the Y axis actuator was not in spec despite backlash compensation, discussed below. A SPCM map of a CNT Schottky diode could not be overlaid with either visible light nor AFM images of the device with appropriate registry when brought to scale; maps of vertically aligned core-shell p-n GaAs NW arrays were found to seemingly contain artifacts. Replacement of the Y axis actuator aided in resolving this issue and realizing precise scanning of samples. Ultimately, it was necessary to tune the PID loop for one axis to obtain nanoscale resolution, which will also be discussed below.

A critical aspect of realizing a SPCM setup which utilizes DC motors is backlash compensation which must be systematically applied. In the limit of nanoscale resolution, DC motors display extreme hysteresis which can be as large as or even larger than the

desired scan range. That is, a change in scan direction inevitably results in error in returning to the initial position if one does not provide compensatory encoder counts in the driving program. Provided the actuator has been scanning for an appropriate distance in a given direction, commanding the actuator to step N times from this zero position in the same direction and then negative N times back towards zero leaves the stage not at the zero position but at a position positive of zero. The motor displays a “memory” of which direction it has been travelling. Correction in the subordinate, or slow, scan direction can be applied once at the commencement of a scan; however, the primary, or fast, scan direction requires correction at the beginning and end of each line scanned. It will now be shown that only over compensating the backlash for a sufficiently long scan range provides a blanket solution for achieving a nanoscale DC motor-driven SPCM platform.

Three essential instances of DC motor scans can be imagined in relation to incurred backlash: under compensation, perfect compensation, and over compensation. Figure 14 schematically depicts the starting (green) and ending (red) points in each scenario given a line is scanned in X, incremented in Y and then returned in X, with the noted backlash compensation, in order to affect the second line scan.

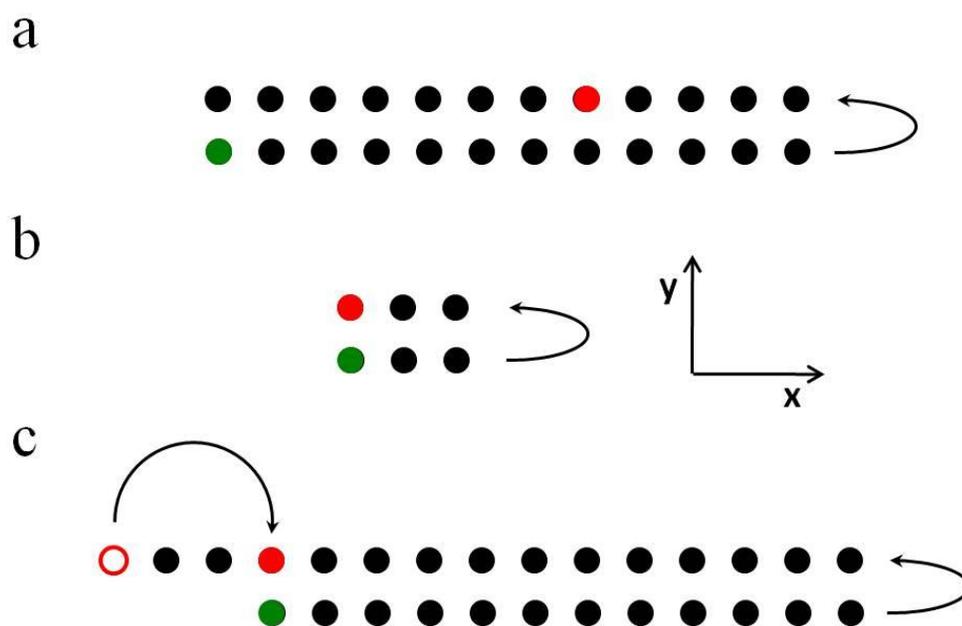


FIGURE 14 Schematic diagram depicting instances of a) insufficient backlash compensation b) compensation suitable for a single instance of return and c) over compensation suitable for robust operation.

In order to confer tangibility, let us use dimensions found heuristically to coincide with the Newport actuators employed. That is, let each incremental point in the grid, in both X and Y, correspond to a step of 1 micron, as the backlash is two orders of magnitude larger than the stepping resolution. Figure 14 a) corresponds to a positive line scan in X after accumulating a “memory” of travelling positively in X and attempting to return to the starting X coordinate with insufficient backlash correction. Typical backlash compensation is approximately 7 microns. This value was experimentally determined by performing calibration scans on arrays of vertically aligned NWs with 500 nm TCO (transparent conducting oxide) capped diameter and 600 nm pitch using a .9 NA, 100X objective and more rigorously by comparing results of SPCM on the arrays. Assuming we command the actuator to perform the under compensation of stepping backward the same number of encoder counts as it did forward, we shall find the starting

point for the second line scan a full seven microns positive of the actual zero position and the mapping will be entirely erroneous.

For nanoscale features and arrays it may be desirable to scan regions of only a micron or less. For a DC motor system, this must be avoided in the primary scan direction but is acceptable in the subordinate direction - provided the backlash is compensated prior to starting the scan. For the primary scan direction, it is necessary that the motor move the appropriate amount of steps to accumulate the full amount of backlash. In the course of this work, it was noted that a 3 micron x 3 micron scan of a NW array should include enough NWs to prove the functioning of the solar cell they comprised while limiting the duration of the scan to an acceptable time frame. Figure 14 b) depicts a perfectly backlash compensated scenario. For a 3 micron scan, the motor does not accumulate the full amount of backlash. In theory, one may expect it possible to simply measure the backlash incurred over this scan size and correct it at the value which will be less than 7 microns. This however results in a program, or at best an input parameter, that is useful only for this particular measurement. Any change in the primary axis scan range will result in an improperly compensated system. In general, this should be avoided whenever possible as calibrating the backlash is quite time consuming. It was also found that true nanoscale resolution in this underscanned case was more difficult to obtain, possibly as a result of uncertainty or variation in the backlash accumulated.

Figure 14 c) depicts the ideal scenario in which an X scan was performed, Y was incremented, and the X axis was commanded to move back the number of positive X steps plus an overcompensation of 3 microns. This intermediate stopping location after return is represented by the hollow red circle. This overcompensation is essentially

arbitrary but should be limited to within reason in order to limit the duration of scans. After applying the positive overcompensation for the memory effect built up by the negative X scan, we are left precisely at the intended starting X coordinate.

The PID control loop is essentially oblivious to backlash since backlash does not affect encoder counts. Once backlash is corrected for however, we should be concerned with the error in position of the actuator which *is* addressable with the PID loop. The difference in actual and intended position is technically termed the following error. The proportional (P), integral (I), and differential (D) gain factors of the control loop contribute to the feedback signal according to:

$$K_p \cdot e + K_i \int e dt + K_d \frac{de}{dt}, \quad (14)$$

respectively, where e , is the following error and t , is time. The PID filter also contains parameters for maximum allowable following error and the integration limit. The maximum allowable following error is a hard limit which disrupts power to the actuator if its value is exceeded at any point of scanning. When tuning, this setting can be informative, but if set too low precludes any further diagnosis of the loop. The P portion of the loop is a weighted correction based directly on the instantaneous error in position that occurs. It reduces following error until set too high at which point it causes the stage to oscillate. The I portion of the loop is a correction factor which is based on the accumulated error. The manual suggests that K_i and the integration limit should be set to nearly the same value. This may constitute a good rule of thumb but offers no insight as to how the loop will be impacted and it makes sense to monitor changes in its value against a calibration standard. The D portion of the loop corrects for change in the error.

Using SPCM maps and the apparent movement of an attenuated laser beam against a NW array, it was possible to tune the PID loop to obtain ~50 nm resolution over few micron by few micron areas. It was also found that error in the minimum incremental motion could cause distortion of the maps from scan to scan. However performing numerous scans and contrasting them to one another as well as the device pitch (known from other microscopies) enabled sorting correct maps from those that contained anomalies. Maps displaying the desired resolution will be given below. It is noted that a stage actuator with smaller minimum incremental motion would enable scans at a still finer scale. Piezoelectric actuators could confer higher resolution stepping of the stage; however, one should consider the desired step size and the desired scan size, as a tradeoff is inevitable to some extent. Additionally, excessively small step sizes prolong the duration of this serial microscopy potentially to the point of introducing unexpected instabilities. Common issues to this end are vertical stage drift/defocusing of the laser and ambient vibration which may introduce serious restraints on how small a step size is actually useful at a given probestation.

Given that the resolution of an SPCM measurement depends strongly on the laser as a probe, optical aspects of the probe station are now discussed in more detail. A suite of objective lenses are employed to perform the various tasks - from a very low magnification, low NA objective for simple probing of contact pads to a high quality objective which was found to be indispensable for SPCM of nanostructures. For laser experiments, unique setups may be encountered depending simply on what material or range of materials are to be investigated by any given group. The lab used in these studies contains two lasers semi-permanently routed to the scanning probe station: a

green helium neon gas laser, $\lambda = 544$ nm, manufactured by Uniphase and an infrared diode laser of $\lambda = 1552$ nm manufactured by Laser Micro Systems, Inc. Given the group's strong interest in IR optoelectronics of CNTs, the green laser's intensity necessarily is diminished in the routing. This is directly a consequence of the demands brought about by delivering the IR beam to the objective with reasonable intensity given large spot size and focusing limitations of IR light. The effects of delivering multiple beams to a single system are lessened when working with say multiple visible wavelength lasers. The lab also contains a red HeNe laser with $\lambda = 638.2$ nm and a HeCd ultraviolet laser, $\lambda = 325$ nm, both of which are manufactured by Melles-Griot. The red and UV lasers can be plumbed into the system as necessary.

The optical table which holds the lasers is shown in the photograph, Figure 15. The image shows how to route multiple beams to achieve delivery of both. One of two beam splitters is shown which results in partial loss of the green laser's intensity. The splitter is needed to reflect the green but pass the the IR laser which impinges from behind it for alignment. The splitter is positioned at 45 degrees from normal to the green laser path. The second loss of green laser intensity and partial loss of IR intensity as well is within the housing of the microscope itself. This beam splitter is needed to pass the helium arc lamp white light source for normal viewing, reflect both laser lines into the objective, and also pass the green light scattered from the sample and red light scattered from the IR detector card into the eyepiece and CCD camera. Alignment is achieved with multiple highly reflecting mirrors. Given that the CCD camera is not sensitive to IR irradiation, the green laser is located on an IR detector card in relation to the IR laser spot. The relation is marked on a monitor fed by the CCD camera. And in this way, the

green laser can be used as a guide beam for positioning the IR laser on samples on which it is invisible, i.e. practically every specimen which is not the IR view card.

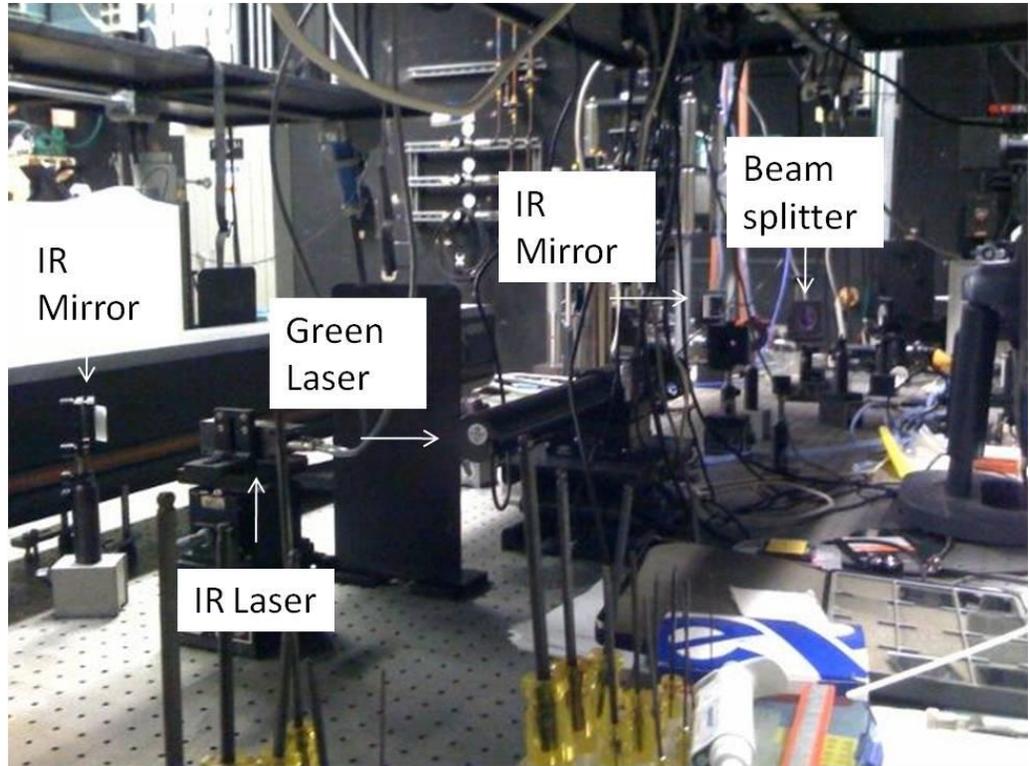


FIGURE 15 Photograph of the optical table and beam routing behind the probestation.

Lasers are valuable for many types of characterization owing not only to their monochromaticity but also to their coherence. This second trait enables the laser beam to be focused to small dimensions which are not accessible by conventional incoherent light sources. Achieving a small spot size enables the use of lasers as high intensity spatial probes for semiconductor devices. The laser spot size is determined by the wavelength of emitted light and the NA of the objective lens used to focus it. The NA is given by

$$NA = n \sin \theta, \quad (15)$$

where n is the refractive index of the medium through which the light travels, always unity for our experiments, and θ is the half angle of focused light from a filled lens. The radius w , of the minimum obtainable spot size is then given by

$$w \approx \frac{\lambda}{\pi NA}, \quad (16)$$

where λ is the wavelength of light. This radius corresponds to where the laser intensity has dropped to $1/e^2$ of the maximum intensity. The beam profile is Gaussian.

5.2.3 SPCM OF VERTICALLY ALIGNED GAAS CORE/SHELL NW SOLAR CELLS

As briefly mentioned above in the context of the scanning stage, high resolution SPCM was carried out on solar cells comprised of an array of core/shell NW p-n junctions fabricated by collaborators at UCLA. The NWs are prepared similarly to those studied in Chapter 4. The p-type core of the NWs in this case is 200 nm in diameter and the n-type shell 60 nm, yielding a total diameter of 320 nm. An insulating buffer layer is deposited and an etch back performed over which a transparent indium tin oxide (ITO) top electrode is deposited to complete the device. These NWs have been chemically passivated at their surface.

SPCM was performed using diffraction-limited optics and a green HeNe laser ($\lambda=544$ nm) to confirm each individual NW functioned as a solar cell. Zero-bias photoconductivity is measured as the sample is scanned on a translational stage with 50 nm/step resolution in X and Y axes. The spot size of the beam is ~ 310 nm as determined from full-width at $1/e^2$. The laser intensity for the measurements is attenuated to $103 \mu\text{W}/\mu\text{m}^2$ to utilize the more sensitive settings of the preamplifier given the critical pitch of the NWs and the levels of photocurrent generated by the NW arrays. Figure 16 a)

shows the SPCM map obtained for the best ITO device, with Figure 16 b) a line scan through the image. The map clearly shows alternating regions of higher and lower photocurrent forming a diamond array, with a spacing of 850 nm laterally and 600 nm diagonally, between maxima. Note that because of the laser spot size and the close spacing between ITO capped NWs (~100 nm), scattering and diffraction result in a non-zero photocurrent even when the laser beam is centered exactly between four NWs. The technique is able to resolve features smaller than the spot size⁶⁰ as the beam profile as well as location is of importance in generating the signal used in the microscopy. The current work is possibly the highest resolution display of the technique in so far as resolving dense features of known proximity. The SPCM mapping validates the fact that the collective J-V characteristics of the array under light are indeed the superposition of all the photocurrent contributions coming from each individual NW. Furthermore, from the laser intensity and maximum generated photocurrent, an EQE of 2.8% is calculated. This number is in reasonable agreement with the one obtained from the full illumination of the devices by our collaborators.

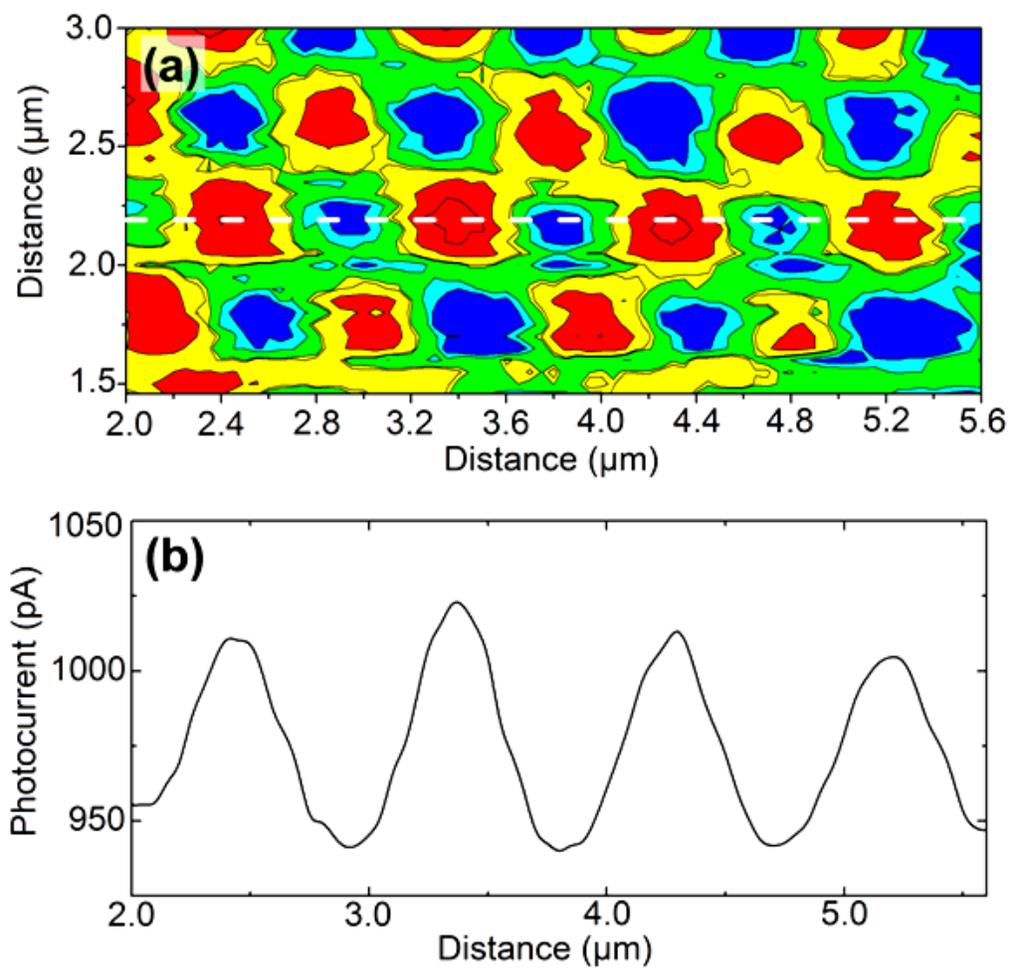


Figure 16 a) SPCM image of the best device processed with ITO as top transparent electrode. Red indicates largest photocurrent and blue the lowest. b) Corresponding photocurrent line profile across the dashed line in panel a).

6 CNT Device Fabrication

6.1 INTRODUCTION

As mentioned in the introduction, the state of the art in CNT research, aside from quantum transport studies for one example, has largely moved to device applications and testing. We are interested in carbon nanotube optoelectronic devices that can be broken into two areas from the perspective of this dissertation: electrostatic p-n junctions and Schottky diodes. These devices serve as excellent testbeds to develop novel optoelectronic characterization techniques.

In order to realize nanotube devices, it is necessary to develop approaches to assemble the nanotubes on substrates with the desired properties. We have developed several protocols for producing devices with different tube densities and positioning across a chip according to the application. A general and often used technique is that of drop casting tubes from solution. This entails using a spinner of the variety used for photoresist deposition to bring a prepared substrate up to a certain RPM and simply pipetting the desired volume of solution. The simple process has many parameters by which the tube density can be affected. We use an RPM of 2000 and vary concentration and volume so as to produce the desired density of CNTs on the wafer. This process affords densities ranging from single tube devices to many tube devices. Alignment of the tubes is found to be only local in so far as considering a particular direction and corresponds to the radial spreading of the solution. Generally, a normal layout for a mask will not find the tubes to be aligned to it. Possibly the simplest deposition procedure would be to suspend the NTs in non-polar solvent and drop-cast the solution onto an

untreated SiO₂ wafer. After spinning, the tubes are found to adhere well to the substrate as a result of van der Waal's forces and do not rinse off with standard cleanroom rinsing procedures. In practice it was found that this simple procedure results in devices which include poor quality tubes and that a large amount of carbon contamination is present.

Figure 17 provides AFM amplitude and height images of two legitimately functioning field effect transistors which contain tubes that are kinked, bundled, notably vary in diameter, and accompanying carbon contamination (large light spots).

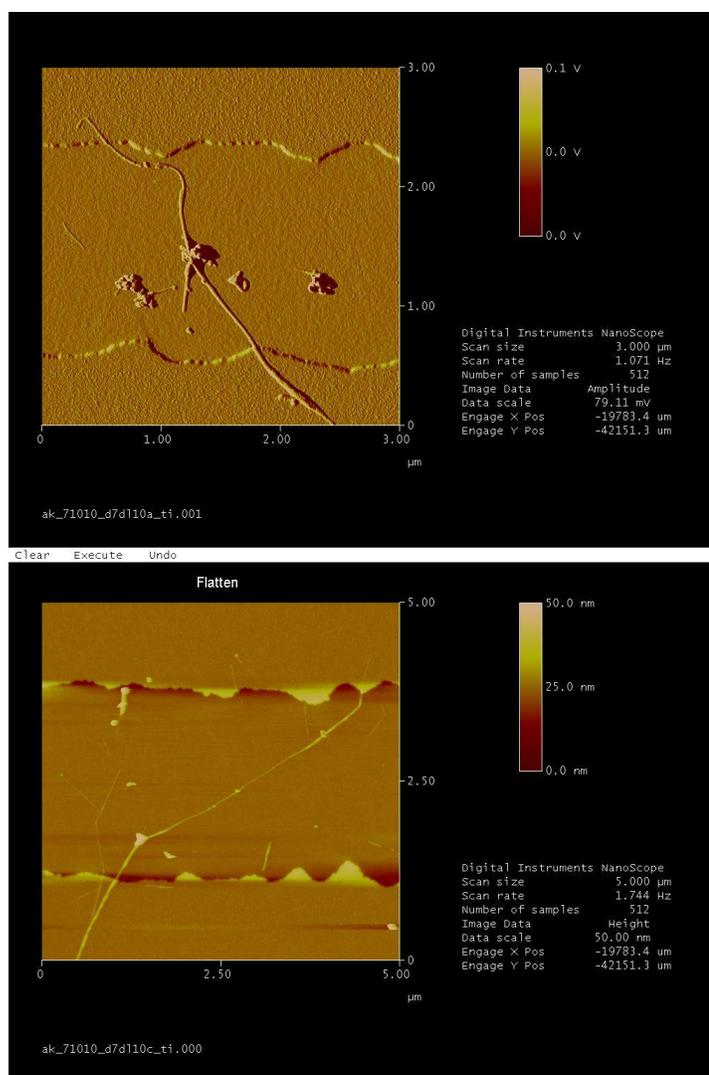


Figure 17 AFM images of CNT transistors employing tubes deposited from non-aqueous solutions. Despite legitimate operation the inferiority of these tubes suggested a more refined process was necessary for solution preparation.

All of these characteristics are undesirable for scientific and technological application and these devices received no additional testing after imaging even though they displayed reasonable FET characteristics. This, in combination with the promise of aqueous based refining techniques has led us to favor surfactant-coated NTs suspended in water.

6.2 AQUEOUS CNT SOLUTIONS

Hersam et al. have shown the potential to sort single wall CNTs by electronic type using density gradient ultracentrifugation (DGU).⁶¹ This is currently the most promising route to realizing controlled applications for tubes, i.e. devices (semiconducting NTs) and interconnects/electrodes (metallic NTs). Even enrichment of certain chiralities has been reported. Tubes enriched in electronic type are now commercially available from NanoIntegris. Solutions containing greater than 99% semiconducting tubes can even be purchased. The specified dimensions for the tubes are 1.2-1.7 nm in diameter and 300 nm – 5 μ m in length. However, we have found the majority of tubes in these solutions are under 1 micron in length and this is reasonably well supported by length histograms offered by the supplier. Tubes less than one micron in length hinder research and development efforts in the field as high performance devices, those in which all NTs in a device fully span the electrodes (i.e. percolation pathways do not dominate the transport) cannot readily be fabricated using late model photolithographic aligners such as those available at most universities and research institutions. Given that e-beam lithography is not a parallel process and has the potential to damage SWCNTs, improvements are needed. We are addressing this issue from both ends by producing clean solutions of long tubes and developing photolithography-based methods which are shown to beat the standard resolution limits.

Typically, catalytic CVD tubes purchased from Cheaptubes.com are subjected to ultrasonication in water in the presence of a particular surfactant. The surfactant is present in concentration exceeding its critical micelle concentration in order to encapsulate the tubes. Often used surfactants are sodium taurodeoxycholate (STDC),

sodium dodecyl benzene sulfonate (SDBS) and sodium taurocholate (STC). This forms an aqueous suspension which is processed in a centrifuge. After the first centrifugation, the supernatant is removed as the precipitate is rich in carbonaceous impurity. A second centrifuge is performed on the supernatant with a density stop layer to further purify the solution. For a third centrifuge, a density gradient is established using Optiprep. Following this last centrifuge, notable bands (see Figure 18) appear in the vial and can be pipetted off in order to investigate the properties of the tubes in these layers. The tubes are found to be

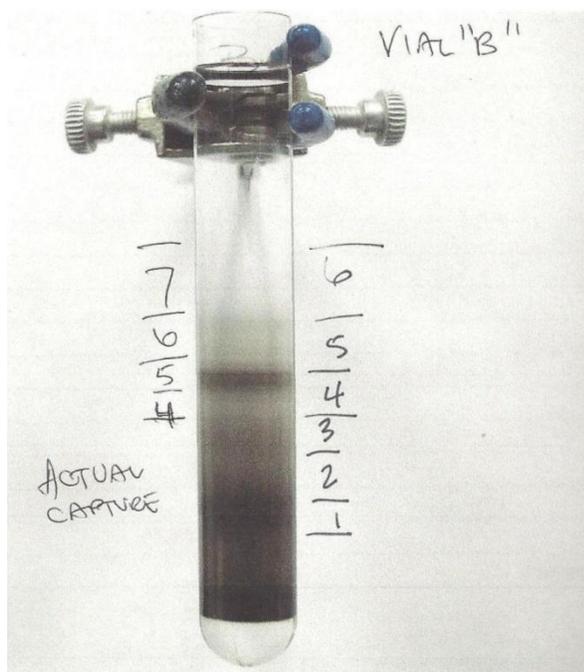


FIGURE 18 Result from a typical DGU run performed by Karen Lee Krafcik.

“clean” and additionally well separated rather than bundled; the anionic surfactants provide electrostatic repulsion which aids in preventing agglomeration which is more common in unfunctionalized tubes. In order to enable the tubes to adhere to the surface,

functionalization of the substrate is necessary. A piranha clean is performed on oxide capped Si wafers and then (3-aminopropyl)triethoxysilane (APTES) is allowed to self-assemble in order to render the surface suitable for tube deposition. The APTES functionalization of the surface promotes adhesion of the tubes via the positively charged amine moiety as the tubes are functionalized with a negatively charged surfactant.

6.3 ALIGNED CNT DEPOSITION

As mentioned, drop-casting solution processable NTs yields tube orientation which is rather unaligned for our intents and purposes. Therefore a new technique was developed which yields reasonably well aligned NTs over the substrate, uses minimal NT solution, and accommodates 4" wafers. Technologically it is important that a technique consume as little NT solution as possible as the solutions which are sorted and purified are particularly valuable. Other alignment techniques⁶² have neglected this issue. A schematic depicting the technique is given as Figure 19.

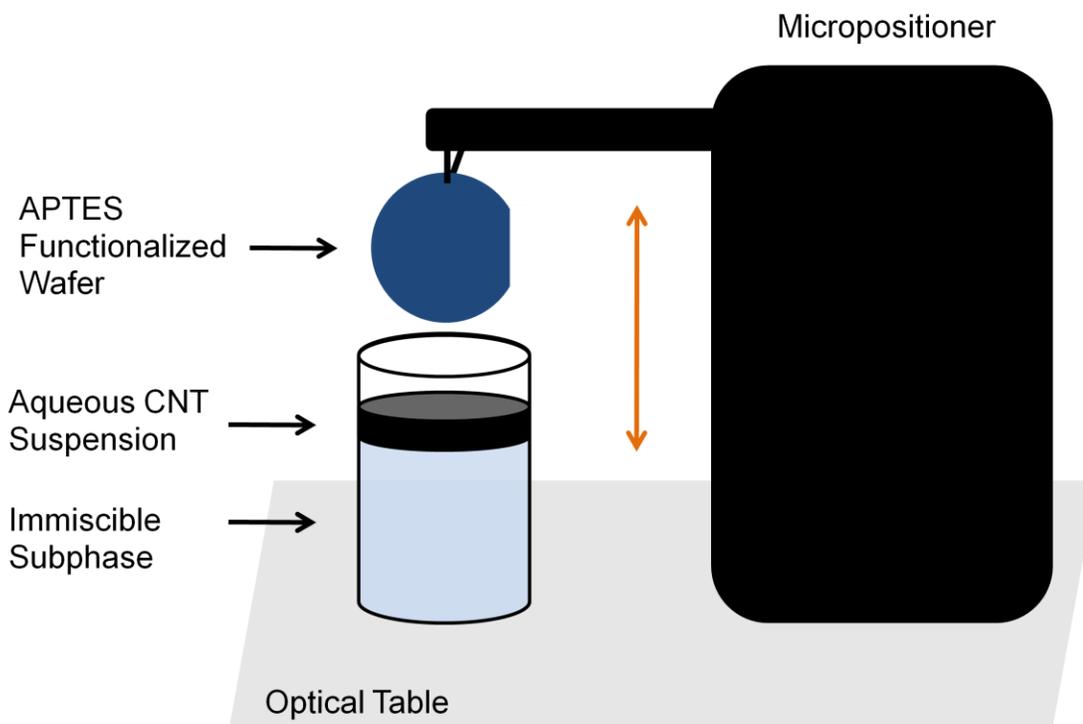


FIGURE 19 Schematic of our NT deposition process. The process enables oriented deposition of tubes for increased device yield. The rate of dipping helps control the tube density.

A degenerately doped Si wafer with a 90 nm thermal oxide capping layer is treated as described above. The wafer is dipped through the aqueous NT suspension which rests on an immiscible organic liquid subphase. The subphase typically employed was dichloroethane or dichloromethane which simply served as a relatively inexpensive filler material. Other non-polar solvents with a density greater than that of the CNT solution could also be employed. A micropositioner is driven in 1 μm increments at rates typically between 100 and 1000 $\mu\text{m}/\text{sec}$. After extraction of the wafer at the same rate, the wafer is rinsed with DI water and dried with N_2 . Standard photolithographic techniques are used to define contact regions. The top panel of Figure 20 depicts the

AFM height image of a NT-FET prepared from a wafer exposed to the dip-coating procedure. It can be seen that the majority of the tubes are aligned perpendicularly to the edge of the electrodes. The bottom panel in Figure 20 is the amplitude image of tubes deposited from a cleaner solution. The direction of deposition is indicated by the arrow in the figure.

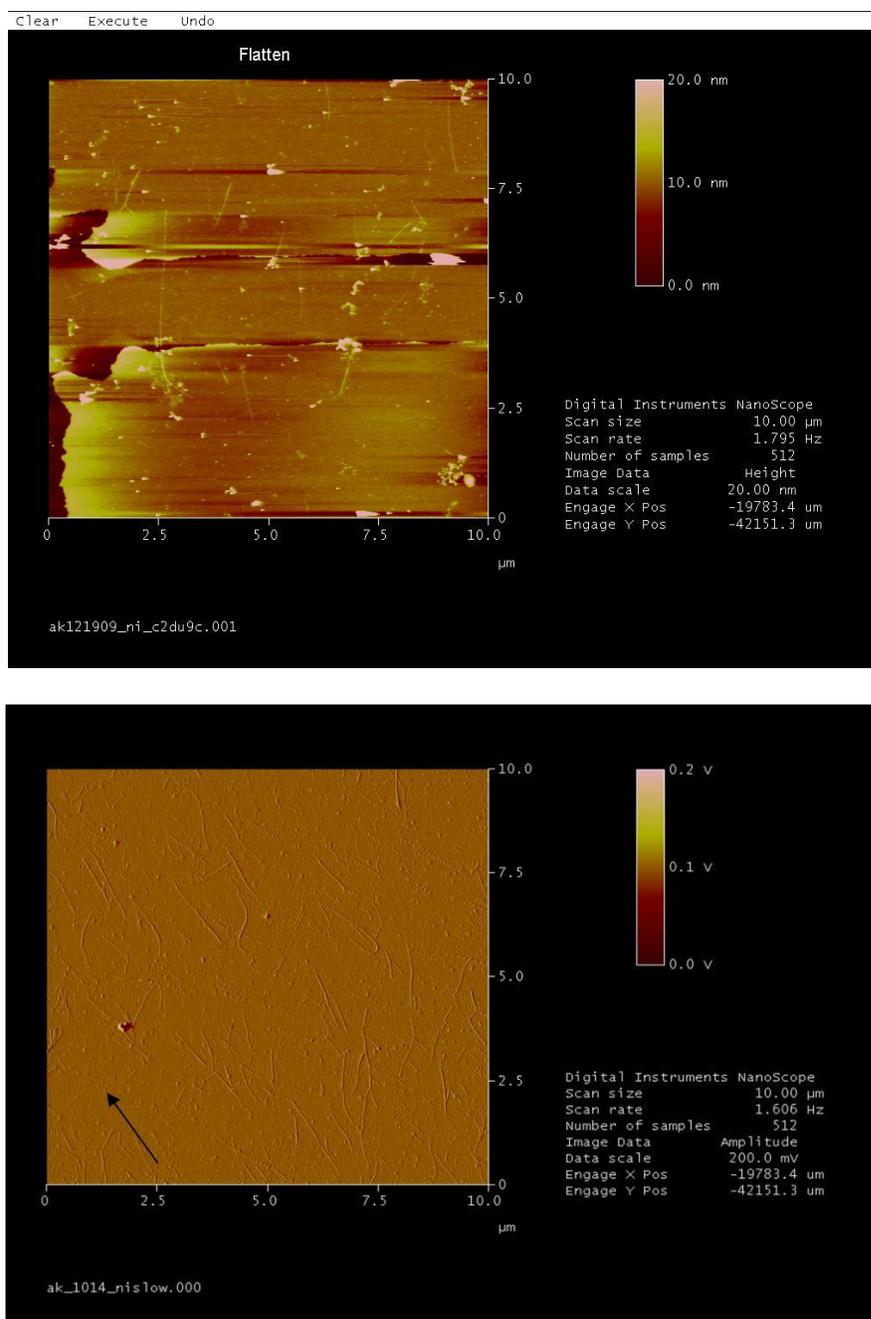


FIGURE 20 Top) AFM height image showing a single tube FET prepared with the deposition method discussed above. Bottom) CNTs deposited from a clean solution. The direction of dipping is indicated by the arrow.

6.4 PHOTOLITHOGRAPHY

After tube deposition has been completed by spin-casting or the dip-coating procedure, a variety of lithography protocols were employed to realize the various devices desired. The main categories for devices were field-effect transistors, split-gate p-n junctions, and Schottky diodes. All devices fabricated employed lift-off after metallization. Initial fabrication of devices was focused on FETs. All other device fabrication protocols grew out of modifications from these two FET procedures. For the first FETs, a negative tone, epoxy-like photoresist was used: NR9-1000PY manufactured by Futurrex. The primary advantage of this PR is its ease of use. It does not require an adhesion promoter and was found to require no special pre-treatment whatsoever. It also develops with its own undercut such that lift-off after metallization readily occurs. Two disadvantages encountered when using this PR alone were non-negligible line edge roughness and the adhesion actually being too good. The first issue is simply aesthetic in most instances; however, the strong adhesion could contaminate the tubes along their length and serve as scattering centers and/or compromise the electrical contact.

A standard lithography procedure for fabricating FETs using NR9 is as follows:

Pipette NR9 onto substrate and spin at 4000 RPM

Pre-exposure bake (time and temperature varied according to feature size)

UV exposure of 450 mJ/cm^2

Post-exposure bake 100°C for 1 minute

Develop in RD6 for 20 seconds

Rinse thoroughly in DI water

Dry with N_2

With this procedure features the size of the resolution limit of a negative tone resist were achieved, i.e. channel lengths of 1 μm , were created. Achieving this feature size resulted in particularly poor line edge roughness and greater contamination however. After metallization with either Pd or Pd with a thin Ti ($< 10 \text{ \AA}$) adhesion layer, liftoff was performed in acetone. The thickness of the Pd layer was typically 20 or 30 nm.

FETs were also fabricated with a standard positive tone PR process based on Shipley S1805. This PR does not display appreciable undercut and so is insufficient for lift-off by itself. Therefore a lift-off resist, LOR series by Microchem, was used to undercut the S1805. The advantage of S1805 is that it forms sharp edges more easily than does the NR9 and being a positive tone PR, it is easier to form small features. Also, the LOR series resists presumably leave clean surfaces after development, and if so may yield better performing devices.

A standard process used for this was:

Bake NT wafer at 200°C for at least 5 minutes to dehydrate

Spin LOR 1A at 4000 RPM for 40 seconds

Bake 180°C for 1 minute

Spin S1805 at 4000 RPM for 40 seconds

Bake at 90°C in convection oven for 30 minutes

UV exposure of 17.1 mJ/cm^2

Develop in MIF-319 for 1 minute

Rinse with DI water

Dry with N_2

The mask used for this process was a dark-field inversion of the mask used for the NR9 process. Similar metallization as that discussed above was performed. Lift-off of the LOR is carried out in Remover PG which is based on the solvent *N*-Methyl-2-pyrrolidone (NMP). It contains a small amount of surfactant to prevent resist from re-adhering to the substrate. Typically, critical features were better formed with this process however non-negligible residual LOR may be left as the product ages or expires. LOR can be effectively removed from non-metallized regions of devices by placing the substrate in NMP under reflux.

The most complicated devices fabricated were the split-gate electrostatic p-n junctions. A heavily doped Si layer capped with thermal oxide was used as the starting substrate. The split-gate pattern was transferred to the wafer using the above procedure for NR9. Forty nanometers of Al was deposited to form these electrodes, and this was followed by deposition of 100 nm of SiO₂ by plasma enhanced CVD. After SiO₂ deposition, the piranha clean, APTES self-assembly, and tube deposition were performed. The above NR9 procedure was used then to fabricate source and drain electrodes after alignment to the split-gate electrode layer was performed. Typically it was beneficial to intentionally overexpose the NR9 to create channel lengths slightly larger than those of the normal FETs. This helps ensure appropriate underlap of the split-gates into the channel and that they are not completely screened by the source-drain electrodes. This impacts device yield but is necessary given the resolution limits of the technology. To complete the devices for probing, one more lithography step was performed. Windows to

the split-gate contact pads were opened by lithography again after alignment. Argon was used as the gas to etch the SiO₂ down to the Al in an Oxford reactive ion etch chamber.

Schottky diodes were fabricated by two methods. The first method relied on alignment lithography. FET electrodes were formed using the NR9 protocol above. Then they were again coated with NR9. The FET structures were aligned to the FET mask and then intentionally offset slightly so as to place the source electrode region into the channel of the pre-existing FET structure while moving the drain electrode region away from the channel. After development a portion of the channel is opened exposing one contact while the other contact is shielded by PR. Subsequent metallization with a material that forms a Schottky contact completes the device. In practice this method gave reproducible results and enables asymmetric devices of shorter channel length to be produced. It was found however that this process is extremely tedious, time consuming and can fail due to the poor resolution of the aligner's microscope. It is likely a high NA objective and/or an electronic translation stage would vastly improve this process. However a less risky alternative to modifying the user facility aligner was ultimately pursued.

The most robust and effective protocol developed for fabricating CNT devices during this study enables asymmetric *or* symmetric contact metal deposition, does not require an alignment lithography step, involves a single metallization vacuum pump down, and can produce channels of arbitrary length, including nanoscopic dimensions far shorter than can directly be realized by the UV flood-exposure alignment tool used for the process. It may be applicable for NW devices as well, but it would require that the NWs adhere as well as NTs to the substrate and are not lifted off during the chemical

processing. This is typically not an issue as there is normally PR pinning the NT/NW to the substrate and only the ends of the NT/NW are exposed for metallization.

The process draws on concepts from micro-electrical-mechanical systems (MEMS) and single electron transistor fabrication – free standing microbeams and tilt-angle shadow evaporation, respectively. Shadow evaporation was used by Javey et al. to produce quasi-ballistic NT-FETs. They first formed FETs and then opened windows exposing the channels. Tilting the substrate in the evaporation chamber enabled the use of the existing electrodes as shadow masks. The new channel length, l is given by:

$$l = t \times \sin \theta, \quad (17)$$

Where t is the thickness of the electrodes deposited in the initial fabrication and θ is the angle of tilt. FETs with channel lengths as short as 10-50 nm were made using $t = 30$ -50 nm. This method was attempted in the author's work. Devices were found to typically be shorted out in the second metallization. Only upon depositing electrodes > 100 nm in thickness were non-shorter junctions produced. This also has the disadvantage of limiting the efficacy of AFM in imaging the devices. For short channels and tall electrodes, the AFM tip cannot image the tube(s) within the channel region and cannot necessarily confirm the number of tubes contacted. A further disadvantage of such short channels is that very thin oxide layers must be used in order to prevent short channel effects. In the case of SiO_2 on Si gate stacks the oxide thickness is thin enough to make gate leaks a concern. For slightly longer channel lengths, thicker SiO_2 layers may be used. The developed process also allows electrodes of arbitrary thickness to be deposited so imaging is not a concern.

It was realized that a lift-off layer could be incorporated in the lithography process to provide a fairly substantial undercut beneath the PR and that this, with tilt-angle evaporation, could provide a route to forming features smaller than can be directly formed with the PR alone. It was apparent that development of the LOR for such a purpose was critical and that line edge roughness would be poor as the LOR would be in contact with the metal and electrode tearing would occur during lift-off. Instead it is better to undercut a mechanically robust PR entirely and leave a free standing bridge as a mask. The bridge is essentially an *in situ* proximal shadow mask with dimensions smaller than are typically encountered in *ex situ* shadow masks. Further the bridges are a well defined height above the substrate. Figure 21 schematically shows the process in cross section. The substrate is loaded onto a turntable in the electron beam evaporation chamber at an angle θ from normal. The pressure in the chamber is maximally a few microTorr. At these pressures, evaporated metal from the crucible travels in a line of sight path. Given this information we can determine L , the length under the bridge of width W , the metal is deposited with simple geometrical consideration:

$$\tan \theta = L/H, \quad (18)$$

So

$$L = H \tan \theta. \quad (19)$$

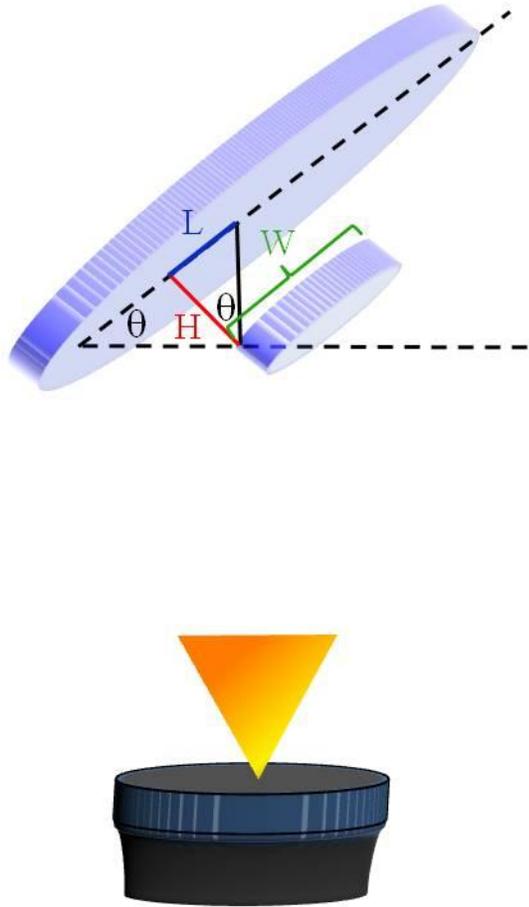


FIGURE 21 Schematic depiction of the tilt-angle evaporation process used to define short device channels and/or asymmetric electrodes.

After depositing the desired thickness of metal, the turntable is rotated 180° by electronic control. This prevents the need to come up to air and then pump down for the second metallization. The process is then repeated with the same or a second metal depending on the device intended. Given the symmetry between first and second metallizations,

$$L_1 = L_2 = L, \quad (20)$$

and L_{TOT} , the final channel length is given by:

$$L_{TOT} = W - 2L. \quad (21)$$

H is known approximately from the LOR datasheet and the spin speed used. It needs to be determined experimentally for best results when attempting very small feature sizes. This can be measured by taking a cross-sectional SEM image and can simultaneously provide the measurement for undercut. A small section of wafer was cleaved from the main sample for this determination. In principle this only need be performed once for a given set of process parameters. The piece was loaded into a sputter coater for 20 seconds in order to deposit $\sim 20 \text{ \AA}$ of AuPd to prevent charging of the PR and LOR. Figure 22 is a SEM micrograph that was used to determine H and the amount of undercut.

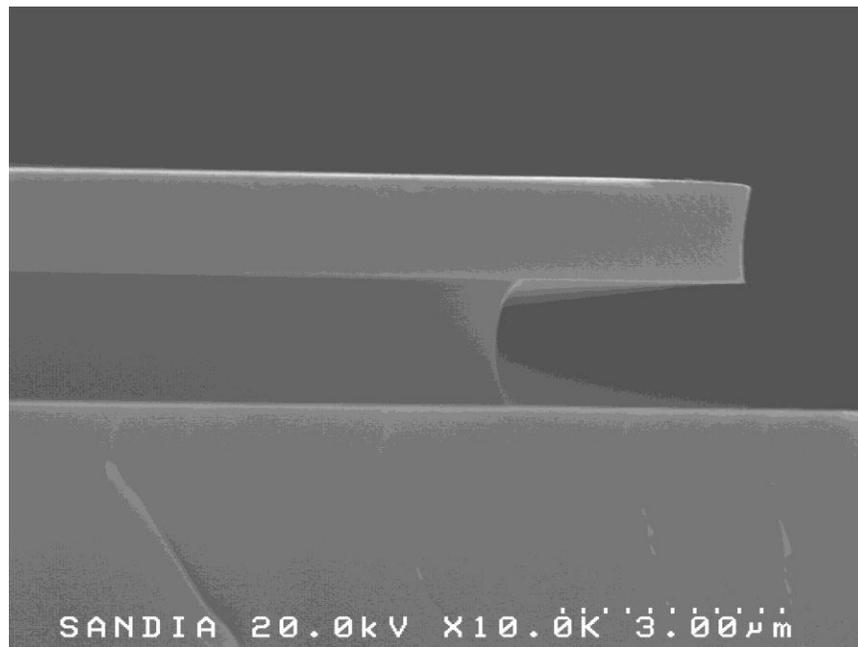


FIGURE 22 Cross-sectional SEM image of the resist bilayer used to produce shadow mask bridges. Note the substantial undercutting of PR enabled by the lift-off resist.

The image shows NR9 on LOR on SiO₂ (90 nm) on heavily doped Si. The image is taken from the cross-section of the contact pad rather than the bridge as cleaving the

substrate at the bridge may cause mechanical disruption of the structure and the undercut will be undefined in the limit that the bridge is freestanding as desired and expected.

Microchem offers LOR in two varieties, A and B, and each variety in a multitude of numbers which correspond to thickness after spinning. The B series offers high undercut rates compared to the A series. LOR20B was chosen to provide reasonable elevation of the PR above the substrate and because it enabled vastly selective development over the NR9 in the NR9 developer, RD6. Three main considerations enter into the formation of the freestanding bridges:

- 1) The bridges should be high enough from the substrate to prevent adhesion to the substrate upon drying after development.
- 2) The bridges should be high enough from the substrate to enable the desired under-
evaporation but low enough to offer appropriate angular resolution.
- 3) The material comprising the bridges should be mechanically robust to buckling.

Initially LOR5B spun three times, baked after each coat was used to validate appropriate conditions. From SEM cross-sectional images, no obvious signs of inhomogeneity through the three layers were observed, suggesting that for developing lithography processes where layer thickness is critical, it may be beneficial and cost effective to use multiple layers of more thinly spun resist. Given this was successful, LOR20B was used to enable similar conditions with a single LOR spin which saves time and money after the protocol has been developed. The difference in viscosity between LOR20B and LOR5B is dramatically larger than between LOR5B and the LOR1 products. As such, LOR20B was found to be the most difficult lift-off resist to work with. Care should be taken while

pipetting and depositing the LOR20B. It should be drawn from the bottle slowly and the pipetting ceased while still submerged in the resist to prevent air bubbles from being captured. Upon deposition, the resist should be delivered slowly and not forced from the pipette as this also introduces bubbles into the layer of resist on the wafer. The resist spins very nicely at 5000 RPM in regards to coverage and uniformity. The only other potential issue is the formation of strands from the edge of the wafer. The polymer strands do not form with the less viscous formulas of LOR possibly because the excess resist is spun well away before the solvent dries. Careful handling is enough to prevent the strands from adversely affecting the lithography. Alternatively the strands can simply be plucked by hand or tweezers, or removed using a swab soaked with NMP.

NR9-1000PY, a negative tone epoxy-like PR was chosen to fulfill the obligation of a strong bridge material. The resist undergoes a cross-linking process under UV exposure which strengthens the resist in relation to the as-spun material. The PR is developed in a basic aqueous solution and the exposed features remain robust for a long process window. Positive tone PRs are designed to degrade under UV exposure and unexposed regions are at best as strong as they were when spun on. S1805 in its developer appeared less selective than NR9 in relation to LOR products perhaps due to increased developer pH; this has the effect of reducing the process window for defining the bridges. Also, after development, exposure to ambient lighting during wafer transfer will not degrade or weaken the negative tone structures. It was known ahead of time that S1805 would be compatible with the LOR products. The last remaining issue in the choice of NR9 for the bridge materials was complete compatibility with the Microchem products. Primary concerns were the compatibility of the solvent the PR is suspended in

and the developer solution. The LOR datasheet suggests compatibility with cyclohexanone (the NR9 solvent) and .24N metal-ion-free developers such as RD6. NR9 appears to scum when exposed to the lift-off solution for LOR20B, comprised namely of NMP; however this was not found to affect the substrate cleanliness likely because it was never in direct contact with the NR9.

The developmental lithography steps for the realization of the *in situ* microbeams were:

Prebake wafer to dehydrate it at 180°C for at least 5 minutes

Spin LOR5B at 3000 RPM for 40 seconds

Bake at 180°C for 30 seconds

Perform two preceding steps as desired, N-1 times (each spin adds ~500 nm of thickness)

Spin LOR5B at 3000 RPM

Bake at 180°C for 3 minutes

Spin NR9 at 3000 RPM for 40 seconds

Pre-exposure bake at 75°C for 30 seconds

Expose wafer to 495 mJ/cm² of UV radiation

Post bake at 100°C for one minute

Develop in RD6 developer for ~25-30 seconds to break through NR9 overlayer

Develop in 5-10 second increments (rinsing in DI water and dry with N₂ each time) and examine under microscope to reach desired undercut

This procedure should work well for deposition of LOR5B layer stacks near three depositions thick. Adding a substantial number of layers may benefit from the use of a convection oven rather than a hotplate in order not to over (under) bake the bottom (top) layers of the stack.

The finalized procedure for producing the microbeam shadow masks was:

Prebake wafer to dehydrate it at 180°C for at least 5 minutes

Spin LOR20B at 5000 RPM for 40 seconds

Bake at 180°C for one minute

Spin NR9 at 3000 RPM for 40 seconds

Pre-exposure bake at 75°C for 30 seconds

Expose wafer to 495 mJ/cm² of UV radiation

Post bake at 100°C for one minute

Develop in RD6 developer for ~25-30 seconds to break through NR9 overlayer

Develop in 5-10 second increments (rinse in DI water and dry with N₂ each time) and examine under microscope to reach desired undercut

Total development times are near 45 seconds for sufficient undercutting. The incremental steps are monitored under a visible light microscope with a 50X objective.

Near completion the bridges are checked using a 100X, .8 NA objective and differential interference contrast (DIC) to highlight the features. Even without DIC the undercutting is readily visible as fringing which spreads outward from the NR9 features which are largely transparent. To ensure sufficient undercut, the width of the fringes are compared to the width of the electrode, typically 20 μm wide, and the region directly beneath the bridge is monitored; it should be fully undercut and show no fringing or residual material beneath it. The bridges are ~ 20 microns long in the suspended region and are usually 3-4 microns wide. This width is approximately three times larger than can be resolved with the same mask and NR9 directly deposited on the wafer. This may be the result of the thicker NR9 layer used for the bridges and the mask being additionally raised the height of the LOR above the substrate which would cause a broadened exposure of the PR as diffracted light reflects from the substrate. Figure 23 a) and b) show the free standing PR bridge structure. Figure 23 c) is an AFM height image of electrodes produced after metallization and liftoff. The minimum electrode spacing is ~ 315 nm.

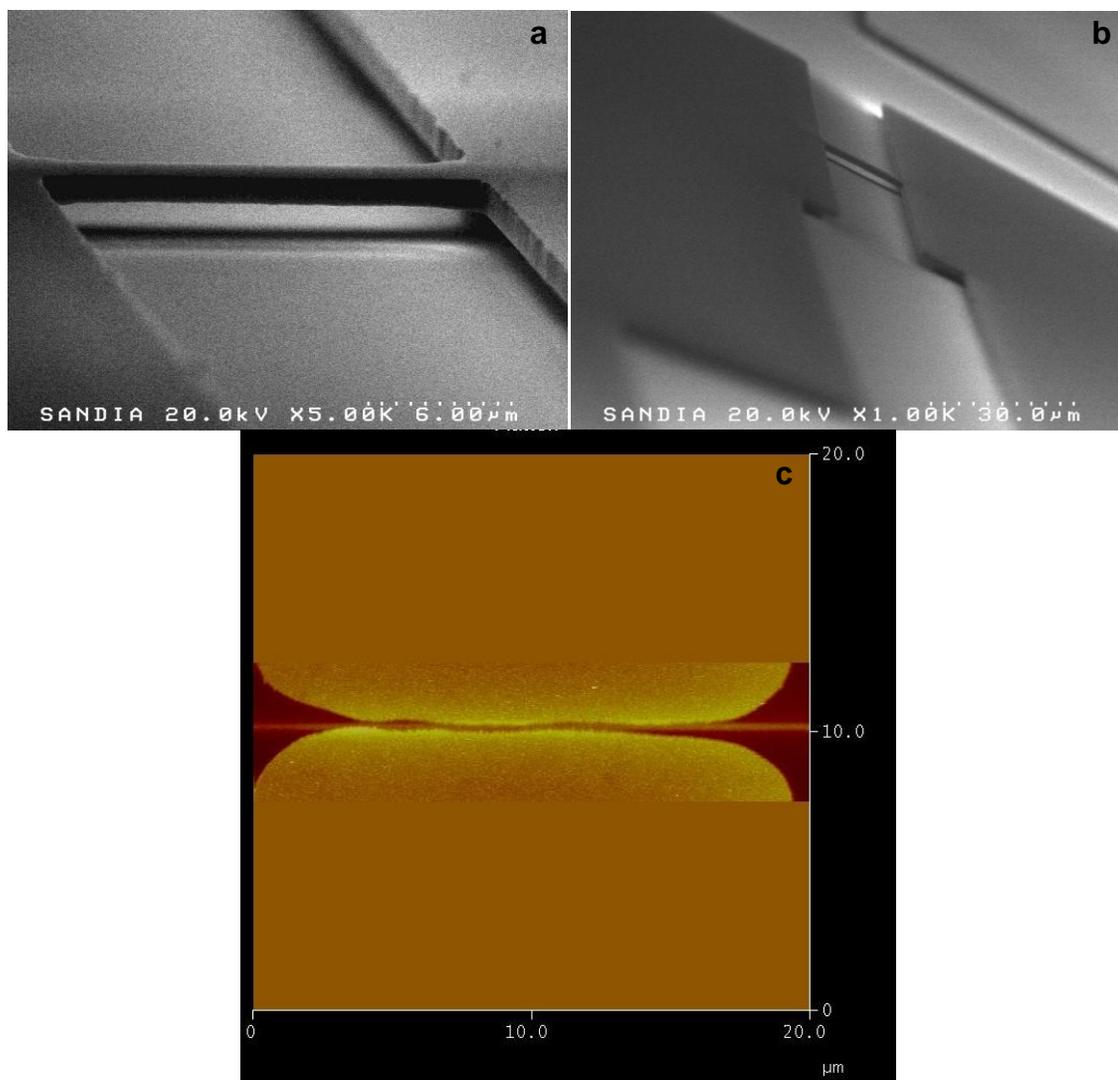


FIGURE 23 a) and b) SEM micrographs of a PR microbridge shadow mask. c) AFM image of electrode spacing showing that submicron feature sizes can be realized using microbridges and tilt-angle evaporation. Here the feature size is approximately 315 nm.

6.5 INCREASING DEVICE YIELD

In the case of multiple tube devices it is sometimes encountered that not all tubes spanning the channel are semiconducting. Unfortunately this prevents transistors from being gated fully off and substantially hampers the “on/off” ratio as is shown in Figure 24 a). The modulation of the current is only by a factor of 3. For diodes, metallic CNTs introduce unacceptable reverse bias leakage current. However, we have found that often

it is possible to render the devices completely semiconducting by controlled burning (oxidation) of the metallic tube or tubes. The method involves gating the semiconducting tubes off with sufficiently high positive gate voltage as determined by the initial transfer characteristic and then sweeping the source-drain bias until a large discontinuous drop in the current is observed. The source-drain bias is then quickly removed. This failure event is shown in Figure 24 c). Figure 24 b) depicts the same transistor's transfer characteristic after the metallic tube has been destroyed and now shows a large on/off ratio.

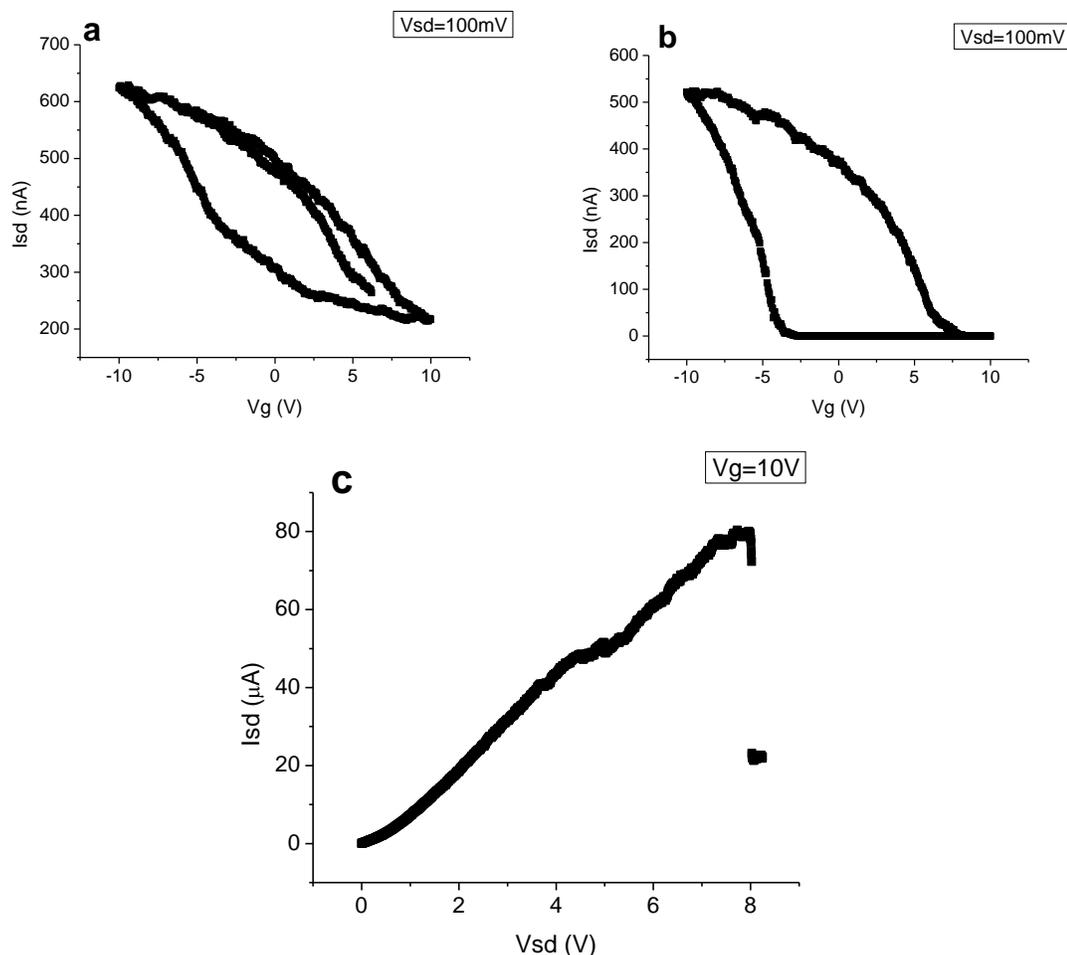


FIGURE 24: The controlled destruction of a metallic NT from a multitube FET. a) The transfer characteristic before burning shows poor modulation of current. b) After burning the NT-FET is comprised only of semiconducting tubes and displays a significantly improved on/off ratio. c) The I(V) curve obtained from the burning experiment. The discontinuous drop in current signifies that the metallic tube has been destroyed. This technique helps increase the yield of high performance transistors and gateable diodes.

7 CNT Device Characterization

7.1 FIRST GENERATION SCHOTTKY DIODES

As described above, Schottky diodes were originally fabricated by a two step alignment procedure. Pd was used to form an Ohmic contact while Ti provided the

Schottky barrier. This can be understood from the band diagram of the system. The workfunction of a CNT is 4.5 eV.⁶³ Tight binding calculations⁶⁴ suggest a bandgap of .6 eV for a CNT with a diameter of 1.5 nm, the median diameter of tubes we use. Now given that Pd has a workfunction of 5.1 eV⁶⁵ we expect alignment to the valence band of the CNT resulting in Ohmic contact. The Ti contact with a workfunction of 4.4 eV⁶⁵ places it in the bandgap of the CNT and results in a Schottky barrier of .2 eV. The AFM amplitude image is given in Figure 25 a). The inset depicts the band diagram. Figure 25 c) shows the device being operated as a transistor in forward bias and Figure 25 d) shows that the device does indeed rectify. Figure 25 b) is the photocurrent map generated by SPCM using an infrared laser and 10X objective. SPCM here validates an important concept that is not readily demonstrated by flood exposure techniques. By spatially mapping the device we show that a unipolar short-circuit current is obtained over the entire active region. This confirms an efficient contact scheme has been realized for a photodetector or solar cell application including for cases involving flood lighting of the device.

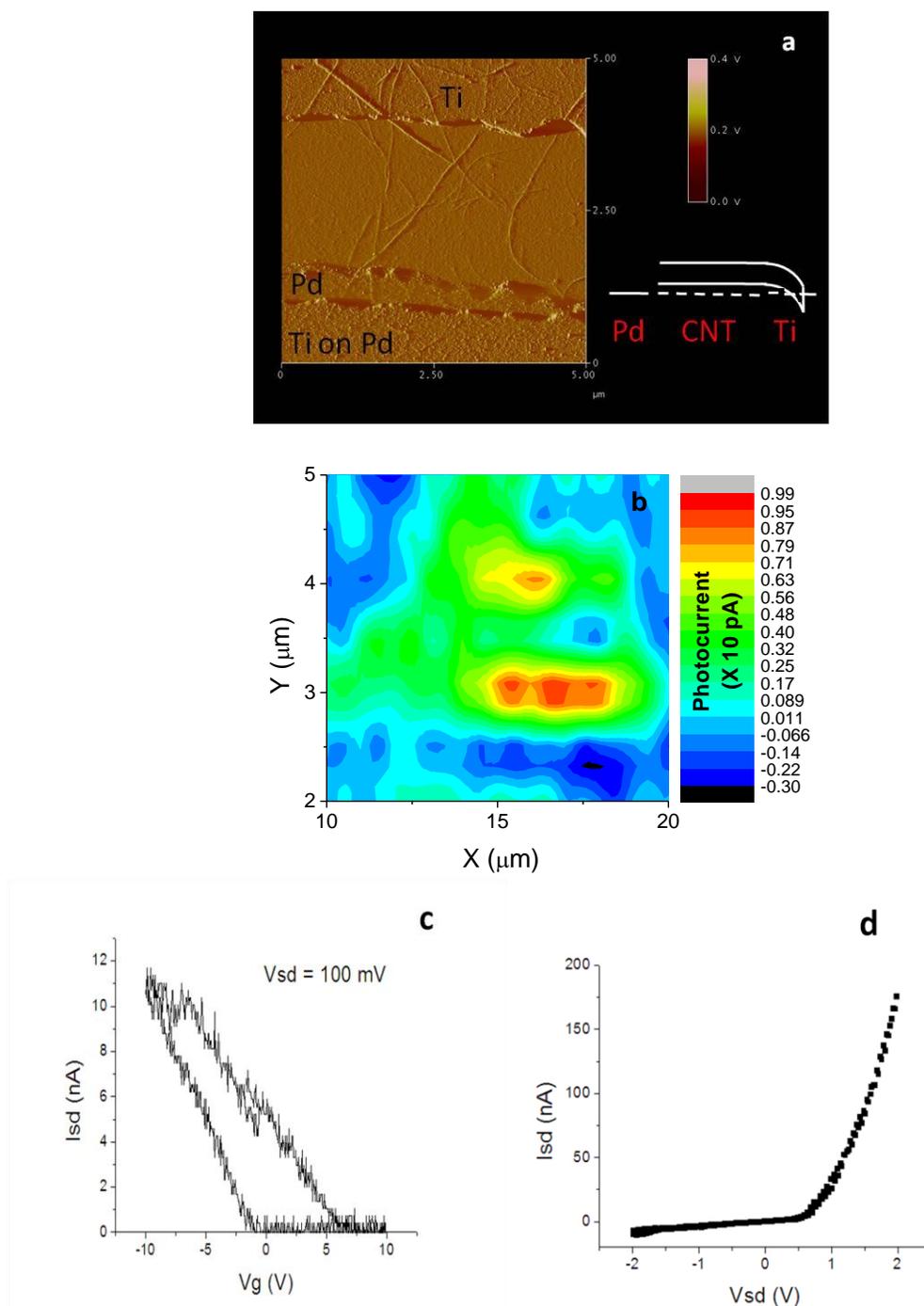


FIGURE 25: a) AFM amplitude image showing a NT Schottky diode. The inset shows the band diagram. b) The photo current map generated by SPCM indicates the ability of the device to detect an IR photocurrent. c) The transfer characteristic for the device in forward bias. d) The I(V) curve shows the desired rectifying behavior.

7.2 ELECTROSTATIC P-N JUNCTIONS

It was expected that improved collection efficiency could be obtained using an electrostatic p-n junction⁶⁶ device as depicted in Figure 26 a). The devices were fabricated using the detailed lithography process mentioned above. Figure 26 b) shows the device functions as a p-n junction diode. The split gates were held at -10 V and 10 V respectively for this measurement. The photocurrent map generated for this device using the IR laser and 10X objective is depicted in Figure 26 c) where the gate voltages used were again $|10|V$. As for the above Schottky diode, a unipolar short-circuit current is collected from the device however the current is an order of magnitude larger here.

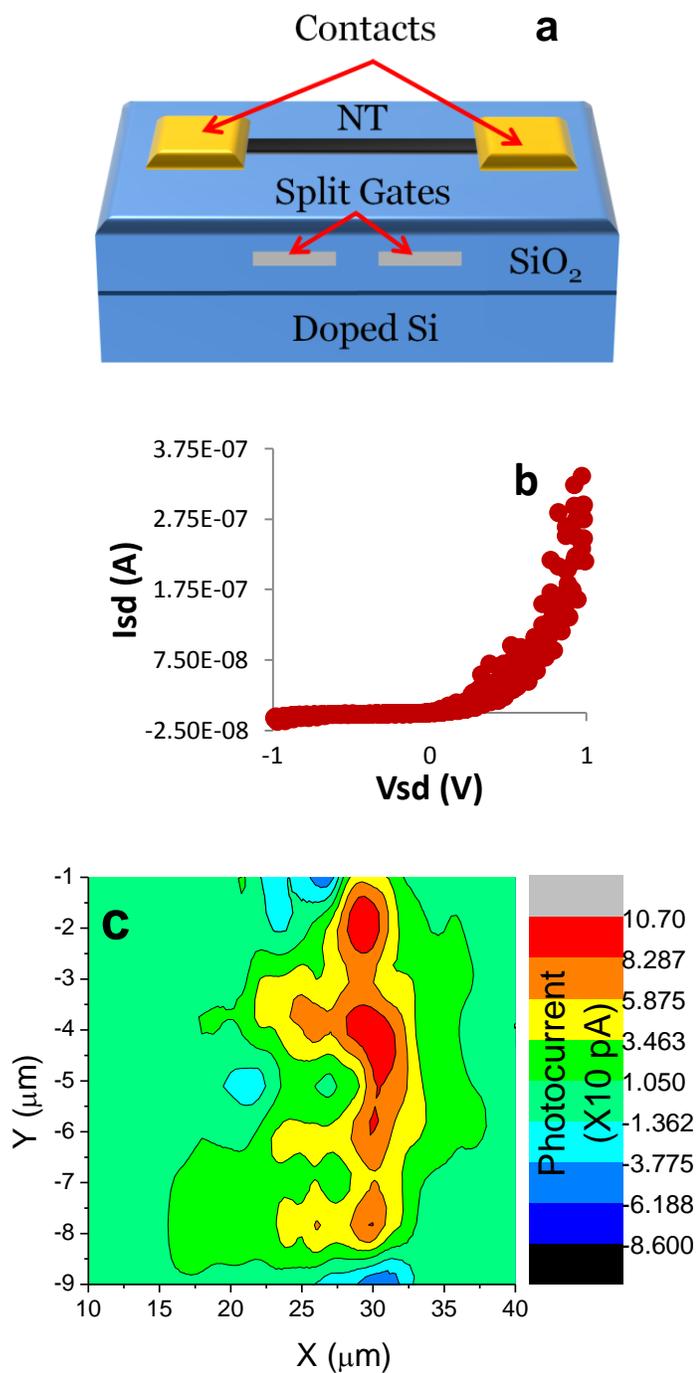


FIGURE 26 a) Schematic of an electrostatic p-n junction device. b) The I(V) curve of one of our devices shows rectification induced by applying $|10|$ V to the split gates. The photocurrent map showing improved collection efficiency over the Schottky diode device.

While, in principal, an electrostatically doped p-n junction could be expected to outperform a Schottky diode at zero source-drain bias, it is now believed that the improved current collection was possibly just due to better resonance of the laser with this device. It has become known that n-type electrostatic doping of CNTs is regularly suppressed by an oxygen/water redox couple present when devices are measured under ambient conditions and employ a SiO₂ dielectric.⁶⁷ Therefore, the device in Figure 26 was likely partially p-type, partially depleted rather than partially p-type, partially n-type.

7.3 SECOND GENERATION SCHOTTKY DIODES

The tedious fabrication procedure used to initially fabricate Schottky diodes from CNTs has been reworked and is yielding better results. Figure 27 a) is an AFM amplitude image of a CNT Schottky diode with one Ti and one Pd contact. The I(V) in panel b) indicates good rectification and little reverse bias leakage current. SPCM of the device was used as a tool to confirm efficient charge collection of the device and locate the position of the CNT at the laser scanning setup. The device was then subjected to photoconductivity experiments at the position of peak PC given in the map.

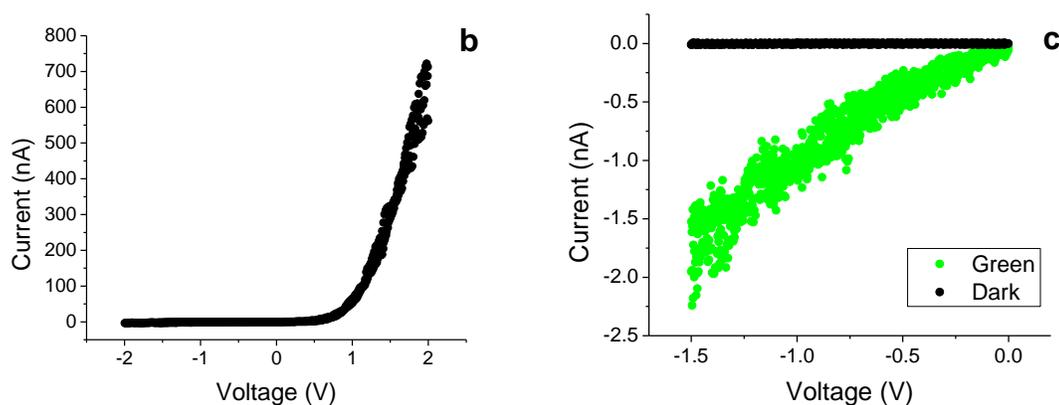
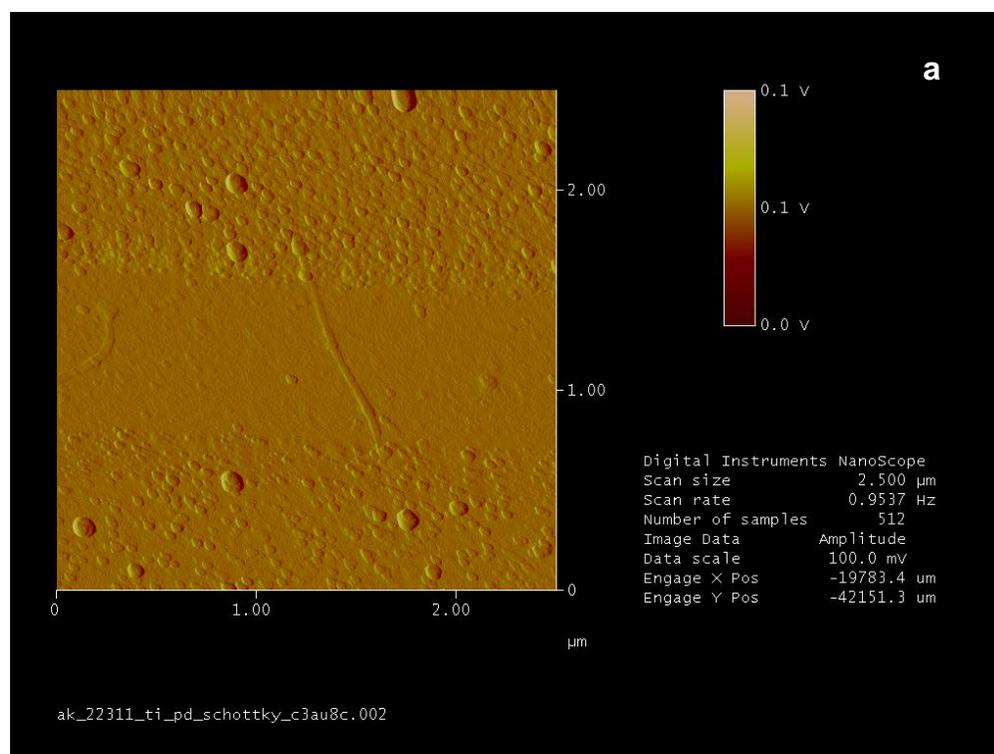


FIGURE 27 a) AFM image of a CNT Schottky diode with one Ti and one Pd contact. b) I(V) curve of the device depicted in panel a). c) The reverse bias photocurrent shows a marked enhancement with increasing reverse bias not seen in conventional photodiodes.

Figure 27 c) highlights a reproducible and unexpected behavior that shows these photodiodes deviate substantially from bulk versions in two major ways. Typically photodiodes have a photocurrent that is generated readily so long as the photon energy exceeds the band gap of the semiconductor and that saturates rapidly when the device is

reverse biased. The CNT devices however appear to show neither of these behaviors. Given the quasi-one-dimensional nature of nanotubes it can be expected that excitation with a non-tunable laser will not correspond to a resonant transition for most devices. Hence, above bandgap illumination is not sufficient for efficient collection of PC. A further concern is that many body effects lead to tightly bound excitons whose binding energies are stronger than thermal energy at room temperature - not true of most bulk optoelectronic materials. The fact that we observe strongly enhanced PC at reverse bias provides an opportunity to investigate these issues in a two terminal device which may be more scalable than electrostatically doped structures and is compatible with solution processed tubes and ambient environment. A concerning issue however arose in light of SPCM work performed at IBM.⁶⁸ Freitag et al. show that localized gating effects can occur in devices fabricated on SiO₂, even though the laser energy does not exceed the band gap of the dielectric, as trap states are populated. We have been able to show that these effects cannot be mimicked by global back gating; however this could be addressed more thoroughly in the future in a suspended device.

The final task in this dissertation was to assess the feasibility of producing such a suspended CNT Schottky diode. Suspended devices have been produced by other groups; however only wet etching the substrate away or stamping the tubes are compatible with solution processing techniques. Due to the success of the wet etching idea,⁶⁹⁻⁷⁰ this was pursued. Both cited papers employ symmetric contacts, however, which are unsuitable for efficient current collection under flood lighting as each electrode's collected current counteracts the other's. A process robust to HF etching had to be developed. The process additionally had to accommodate asymmetric electrode

deposition. Ultimately it was found that using the microbridge shadow mask to deposit a Cr (30 nm) Schottky contact and an Ohmic Cr(30 Å)/Pd(30 nm) contact was suitable. Annealing at 600K for 5 minutes conferred suitable adhesion to prevent “wicking” under the electrodes for an isotropic under etch. The anneal also aids in achieving Ohmic contact at the Cr/Pd electrode. A buffered oxide etch is used to etch out the supporting SiO₂ dielectric at 100 nm/minute, typically for 2.5 minutes. Figure 28 shows SEM micrographs and corresponding I(V) curves (immediately to the right) for two suspended diodes produced by this procedure.

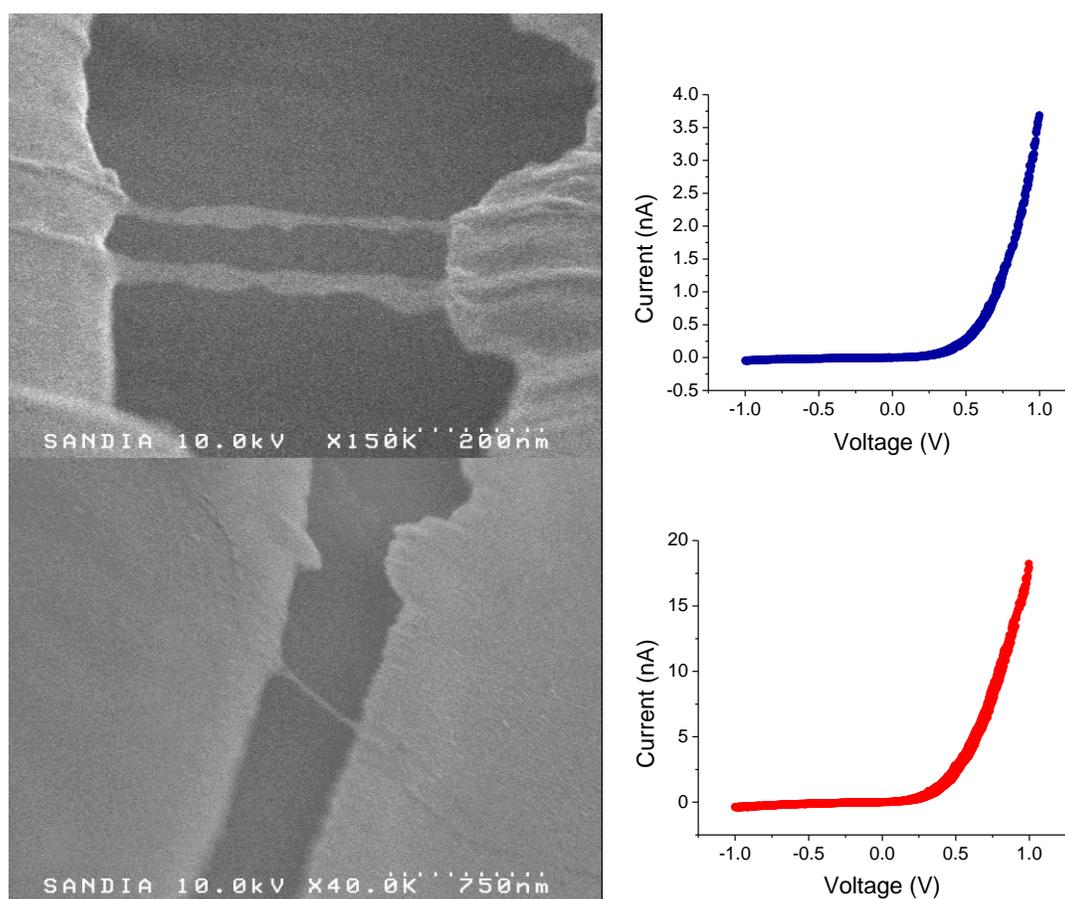


FIGURE 28 SEM images and I(V) curves for suspended CNT Schottky diodes.

It is noted that the diodes appear to be comprised of NT bundles rather than single tubes. They are taught however and clearly survive the under etch process without getting pinned to the newly lowered surface below. Given the desirable I(V) characteristics, optical response at reverse bias will be the subject of future work with the aim of understanding the strong PC enhancement observed in Figure 27 c) and potential applications. The nature of the effect could be investigated by varying intensity and changing wavelength (green to red) of the probe laser. Additionally, the devices could be illuminated with a tunable laser to probe differences between resonant and non-resonant excitation.

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9 List of Publications

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