

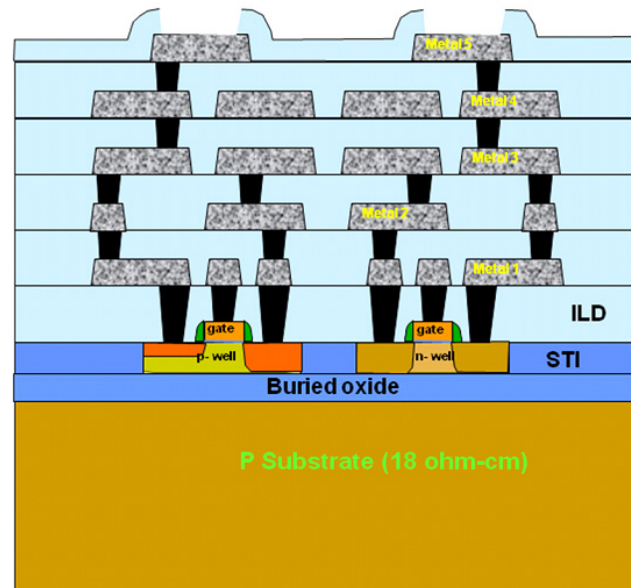
Radiation-Hardened Technology

In support of its primary mission as steward of the U.S. nuclear stockpile, Sandia has developed and delivered microelectronic products for over three decades. This expertise has also been applied to other national security needs. These include ensuring the nonproliferation of nuclear weapons and materials, reducing the threat from chemical and biological weapons, and providing advanced custom designs for other agencies involved in national defense. Sandia's Application-Specific Integrated Circuit (ASIC) development team provides custom microelectronic products and engineering services that fulfill the needs of a diverse set of customers.

Sandia's CMOS7 technology is a strategically radiation-hardened, 3.3-volt, 0.35-micrometer, SOI (Silicon-on-Insulator) CMOS process for custom, high reliability digital, analog and mixed-signal ASICs. CMOS7 is a 24 mask level process with 5 metal layers.

Options for analog and mixed-signal applications include Metal-Insulator-Metal (MIM) capacitors and N+ poly resistors.

Sandia uses 0.35-micrometer geometry to optimize performance for analog circuits resulting in better device matching, higher supply voltages, lower leakage, and broader signal dynamic range than smaller geometry devices. Properly designed and fabricated, larger devices are more likely to continue to perform in extended operating environments of temperature fluctuations, shock and radiation.



CMOS7 Radiation Performance

- **Sandia National Laboratories has developed and tested its CMOS7 technology to meet or exceed all applicable ITAR limits.**
- **CMOS7 was specifically designed to withstand strategic radiation environments.**

Performance specifications available upon request for qualified inquiries.

Sandia National Laboratories has historically focused on high-reliability custom solutions for high-consequence applications. Today Sandia is a DoD Category 1A Accredited Supplier of both "trusted design and foundry services" with an efficient and disciplined ISO 9001 certified process optimized for high-mix low-volume custom radiation-hardened, digital, analog and mixed-signal ASICs. With in-house capabilities in packaging, test, failure analysis and reliability, Sandia offers a total supply-chain solution for high-reliability custom microelectronics for expanding national security applications.



Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

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A Total Solution

ASIC Design Services

Sandia's ASIC development team develops and maintains digital, analog, and mixed-signal design expertise along with a deep understanding of technology offerings and design methodologies to provide custom microelectronic products and engineering services that fulfill the diverse needs of our customers. Sandia's design team implements a disciplined ISO certified process using the latest EDA design tools to realize designs in foundry technologies ranging from 350nm to 45nm.

CMOS7 Foundry Support

Process Design Kit (PDK)

Technology model files and support for custom design, layout, and validation.

Standard Cell and I/O Libraries

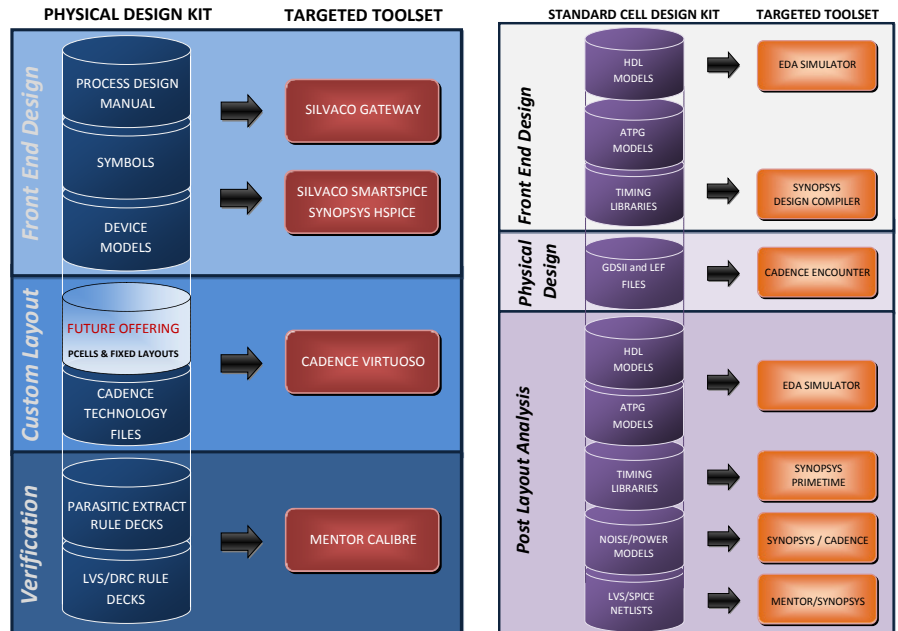
Full suite of standard cell and I/O cells with support for simulation, synthesis, and physical design.

Analog Intellectual Property (IP) Modules

Including A-to-D Converters, PLLs, and D-to-A Converters (contact for full listing)

SRAM and ROM Memory Macros

Pre-configured memory array macros (contact for full listing).

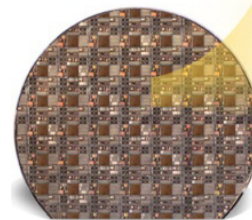
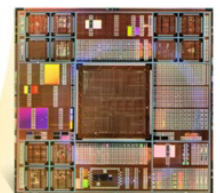
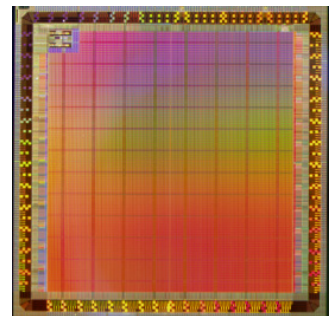


Structured ASIC

Sandia has developed a structured ASIC that enables rapid turn-around, lowers non-recurring engineering (NRE) and development costs, and reduces development risk by using pre-qualified base arrays. The structured ASIC is a metal-via configurable, regular fabric like structure using the ViASIC[®] Via-Mask Technology. Sandia's structured ASIC is partitioned for power sequencing and redundancy which also allows unused transistors to be turned off to minimize power consumption, static current, and photocurrent. The option to include on-package decoupling capacitors is also included. Currently, two product platforms have been developed: Eiger ViArray Digital Radiation-Hardened Structured ASIC and Whistler ViArray Mixed-Signal Radiation-Hardened Structured ASIC.

Multi-Project Wafer (MPW) Program

Sandia's MPW Program provides MPW services for CMOS7 radiation-hardened ASICs. MPW services integrate a number of different integrated circuit designs on a single reticle set. Sharing mask and wafer resources reduces the overall cost per design and makes it more cost effective to produce integrated circuits in low quantities.



For more information email snlasic@sandia.gov
www.sandia.gov/mstc

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