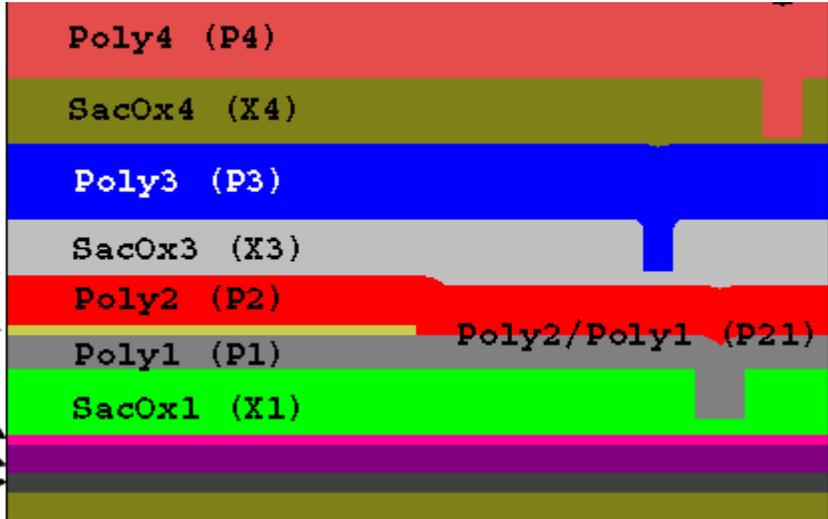
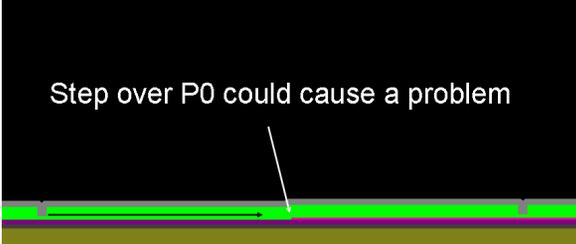
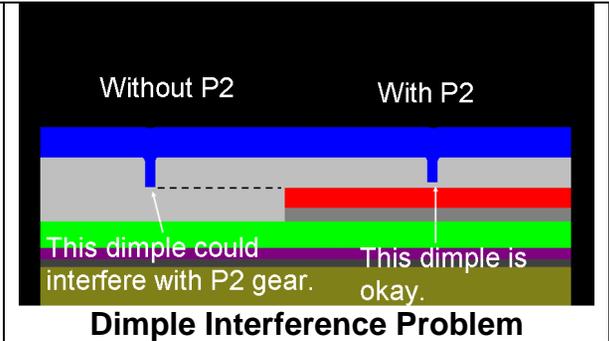
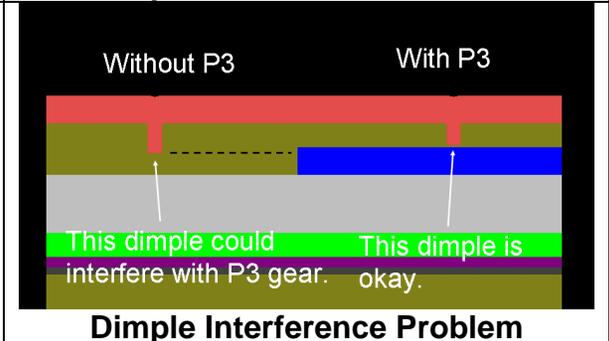
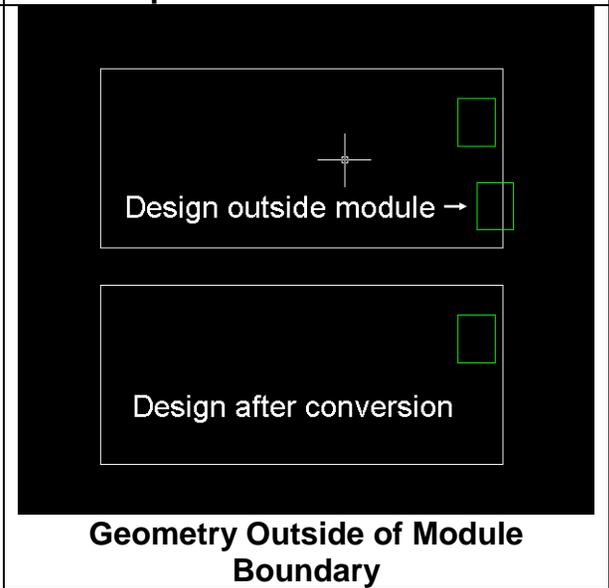
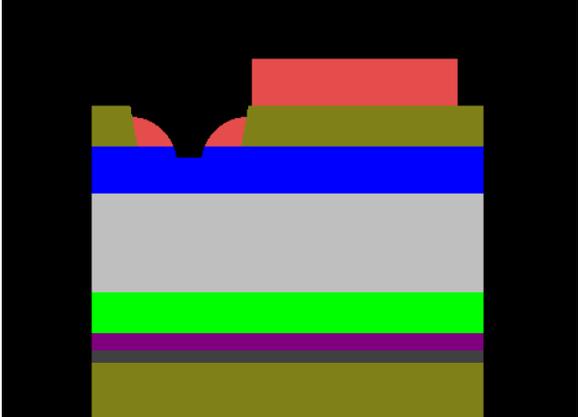
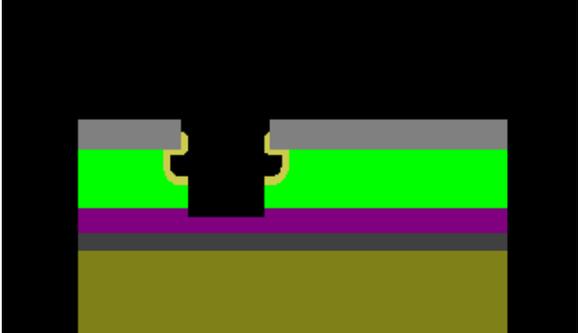


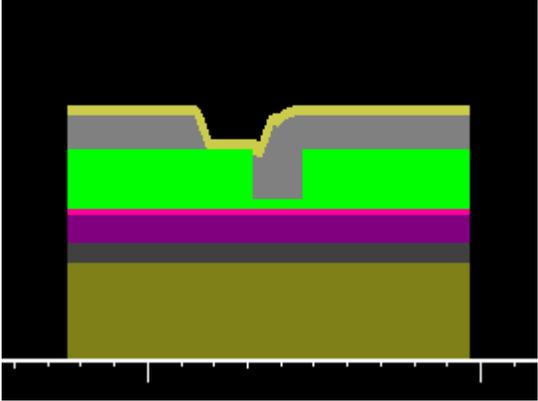
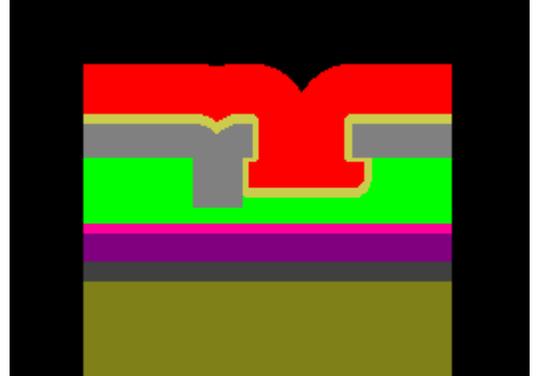
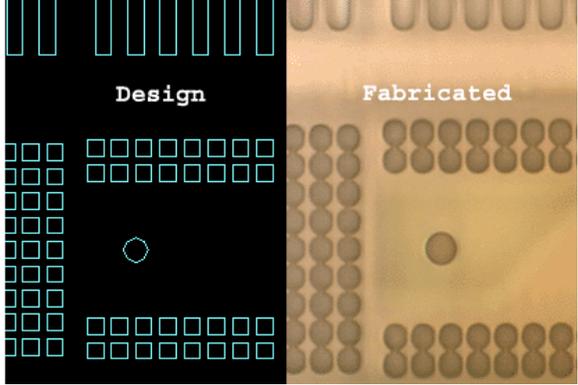
DRC Error Code Descriptions

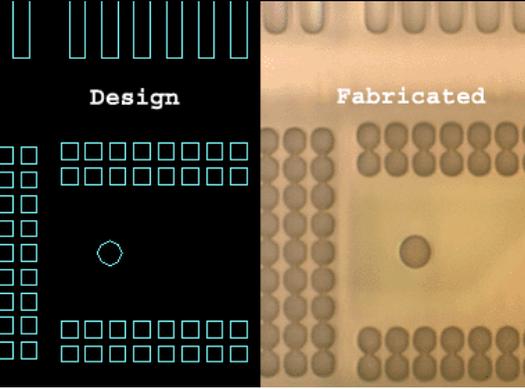
Error Code	Short Description	Text Description	Picture
<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;"> <p>SUMMIT V (TM) LEGEND</p> <div style="display: flex; flex-direction: column; gap: 5px;"> <div style="background-color: yellow; padding: 2px; border: 1px solid black;">SacOx2 (X2)</div> <div style="background-color: magenta; padding: 2px; border: 1px solid black;">Poly0 (P0)</div> <div style="background-color: purple; padding: 2px; border: 1px solid black;">Nitride</div> <div style="background-color: olive; padding: 2px; border: 1px solid black;">Poly0 (P0)</div> </div> </div> <div style="text-align: center;">  </div> </div>			
ADV_D1C_S_GT_75	dimple1_cut space greater than 75µm	Advisory indicates there may be problems with stiction if the Dimple1 spacing is greater than 75 µm.	 <p style="text-align: center;">Dimple Spacing Minimum</p>
ADV_D1C_WITHOUT_P0	dimple1_cut without mmpoly0	Advisory warns that there could be a step difference between dimples that have P0 and dimples that don't.	 <p style="text-align: center;">Possible Dimple Step Issues</p>

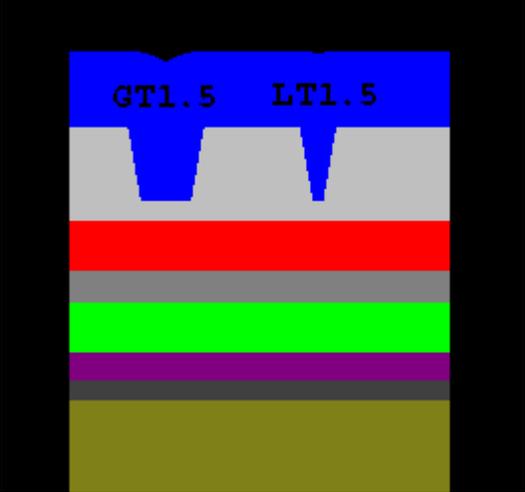
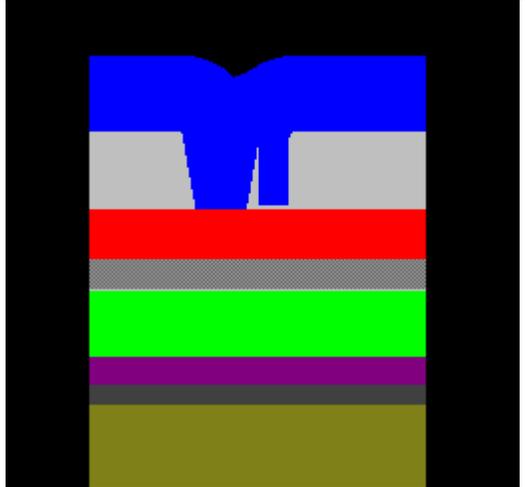
<p>ADV_D3C_WITHOUT_P2</p>	<p>dimple3_cut without mmpoly2</p>	<p>Warning that there could be interference issues in areas where Dimple3 has been created without P2. Curvature due to process related stresses could cause a Dimple3 structure to contact the edge of a Poly2 structure during movement.</p>	 <p>Dimple Interference Problem</p>
<p>ADV_D4C_WITHOUT_P3</p>	<p>dimple4_cut without mmpoly3</p>	<p>Warning that there could be interference issues in areas where Dimple4 has been created without P3. Curvature due to process related stresses could cause a Dimple4 structure to contact the edge of a Poly3 structure during movement.</p>	 <p>Dimple Interference Problem</p>
<p>ADV_GEOMETRY_OUTSIDE_MODULE</p>	<p>geometry outside of module boundary</p>	<p>All designs must fall within the module boundary. Geometry defined outside of the module boundary could be omitted from the final conversion.</p>	 <p>Geometry Outside of Module Boundary</p>

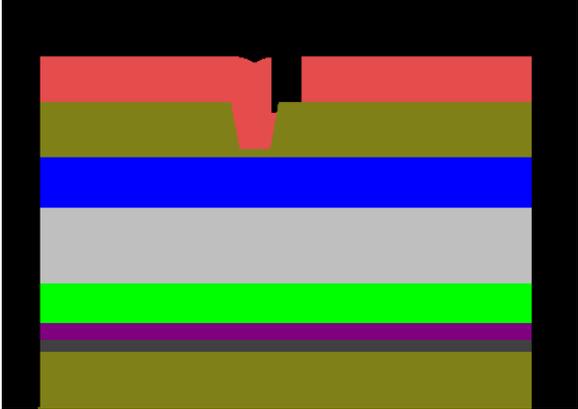
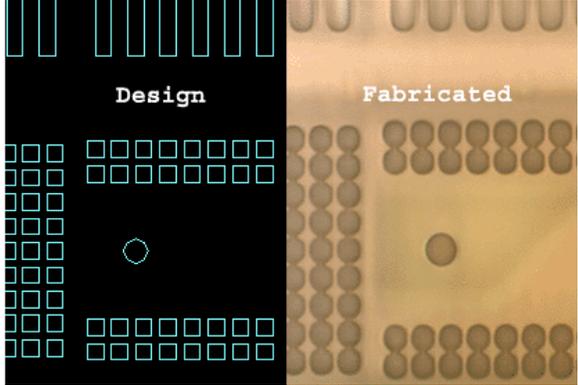
<p>ADV_P1_WITHOUT_P0</p>	<p>mmpoly1 without mmpoly0</p>	<p>Warning that there may be problems with Nitride layer accumulating charge and could cause unintended actuation, or discharge. If a Poly0 ground plane is used the potential needs to be managed. In the right-hand picture the beam is at the same potential as the ground plane.</p>	
<p>ADV_P2_X1C_E_LT_0PT5</p>	<p>mmpoly2 enclosure of sacox1_cut less than 0.5μm</p>	<p>This advisory is a warning because there could be Poly1 over the Sacox1_Cut. 0.5 μm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error.</p>	
<p>ADV_P2_X2_OLAP_LT_0PT5</p>	<p>mmpoly2 overlap of sacox2 less than 0.5</p>	<p>If there is insufficient overlap between Poly2 and Sacox2, a slight misalignment between layers can lead to etching trough the Poly1 layer. In cases like these it is recommended that there be a minimum of 0.5 um overlap.</p>	

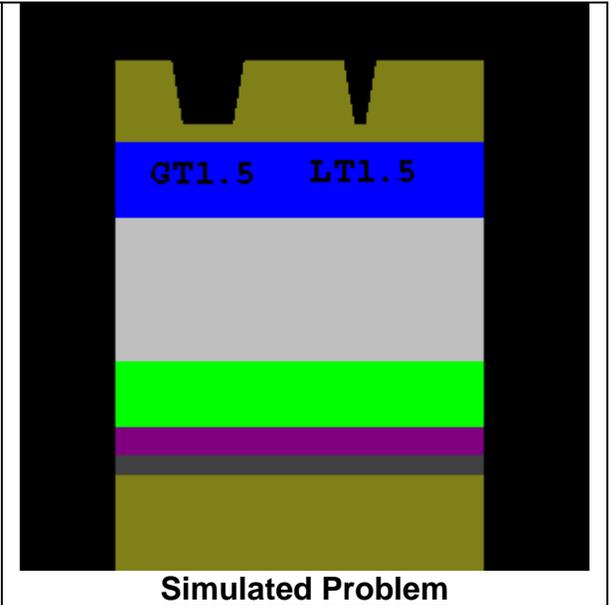
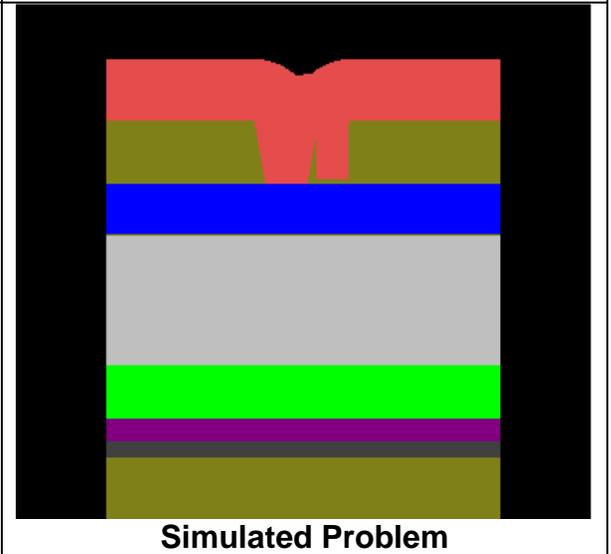
<p>ADV_P2C_SPC_GT_38</p>	<p>mmpoly2_cut space greater than 38µm</p>	<p>Warning of possible release problems if the spacing between etch release holes is greater than 38 µm.</p>	 <p>Potential Oxide Release Problem</p>
<p>ADV_P3C_SPC_GT_38</p>	<p>mmpoly3_cut space greater than 38µm</p>	<p>Warning of possible release problems if the spacing between etch release holes is greater than 38 µm.</p>	 <p>Potential Oxide Release Problem</p>
<p>ADV_P4_NOT_TOUCHING_X4C</p>	<p>mmpoly4 not touching sacox4_cut</p>	<p>Warning that there could be floating Poly4 structures if not properly anchored to Poly3.</p>	 <p>Simulated Problem</p>
<p>ADV_PJC_WITHOUT_P0</p>	<p>pin_joint_cut without poly0</p>	<p>Warning that there may be problems with etching of the nitride layer in certain circumstances. Also, nitride layer could accumulate charge and cause unintended actuation, or locking of device.</p>	 <p>Simulated Problem</p>

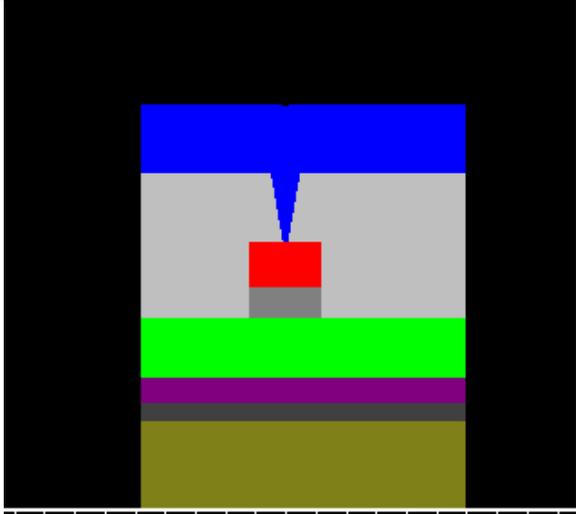
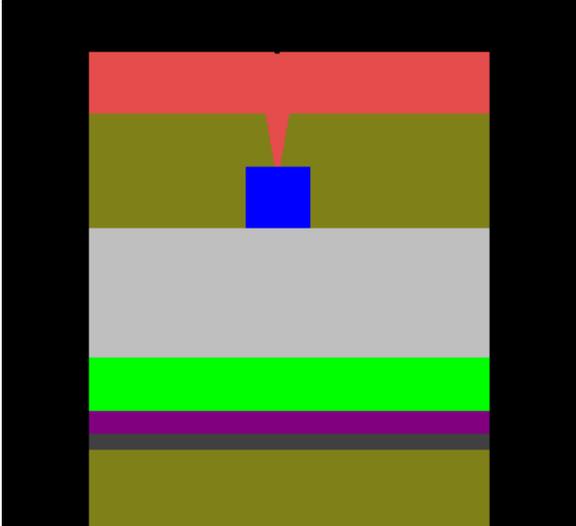
<p>ERR_D1C_P1C_S_LT_0PT5</p>	<p>dimple1_cut space to poly1_cut less than 0.5µm</p>	<p>0.5 µm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_D1C_P1C_S_LT_1</p>	<p>dimple1_cut space to pinjoint_cut less than 1µm</p>	<p>Pin joint undercut will impinge on the dimple structure creating an uneven pinjoint structure that could fail.</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_D1C_S_LT_1</p>	<p>dimple1_cut space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p> <p>Cuts next to each other can merge together, and lines can be considerably thinner than intended.</p>	 <p style="text-align: center;">Example of merged features Less Than 1.0 um rule (...LT_1)</p>

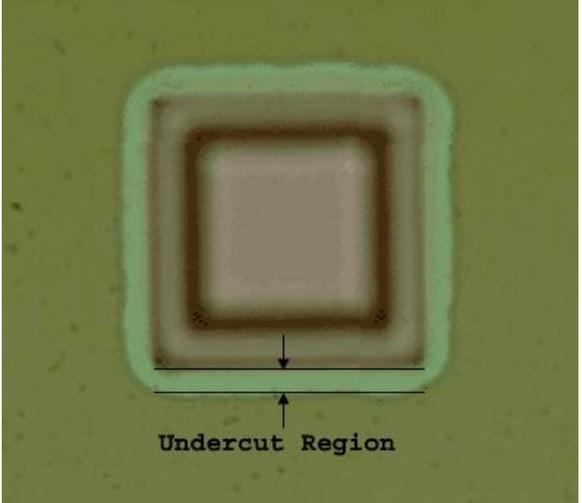
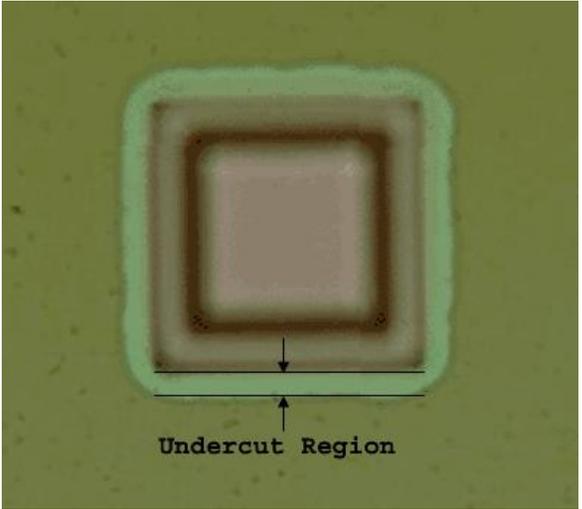
<p>ERR_D1C_W_LT_1</p>	<p>dimple1_cut width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p> <p>Dimples with less than 1 um width could result in inadequate photo resist clearing. Dimples could become sharp at the bottom or not etch to full depth.</p>	 <p>Simulated Problem</p>
<p>ERR_D1C_X1C_S_LT_1</p>	<p>dimple1_cut space to sacox1_cut less than 1µm</p>	<p>Dimple1 and SacOx1 Cut can merge together when designed to close to each other. Photo lithographic alignment tolerances and the sidewall slope can combine to create a single feature rather than what was intended.</p>	 <p>Simulated Problem</p>
<p>ERR_D3C_S_LT_1</p>	<p>dimple3_cut space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p> <p>Cuts next to each other can merge together, and lines can be considerably thinner than intended.</p>	 <p>Design Fabricated</p> <p>Example of merged features Less Than 1.0 um rule (...LT_1)</p>

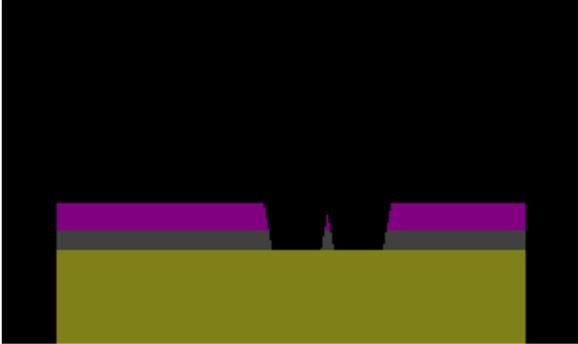
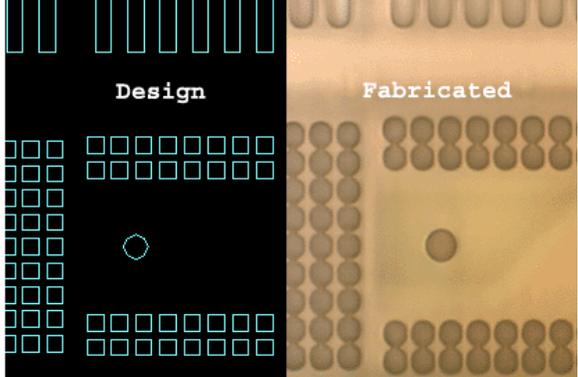
<p>ERR_D3C_W_LT_1PT5</p>	<p>dimple3_cut width less than 1.5μm</p>	<p>Dimple 3 backfill will close feature by 0.4 μm on either side. Process variations could create a closed off feature that may have a void (keyhole), unexpected sharp tip, or less than full depth etch.</p>	 <p>Simulated Problem</p>
<p>ERR_D3C_X3C_S_LT_1</p>	<p>dimple3_cut to sacox3_cut space less than 1μm</p>	<p>Dimple3 and SacOx3 Cut can merge together when features are to close to each other. Photo lithographic alignment tolerances and the sidewall slope can combine to create a single feature rather than what was intended.</p>	 <p>Simulated Problem</p>

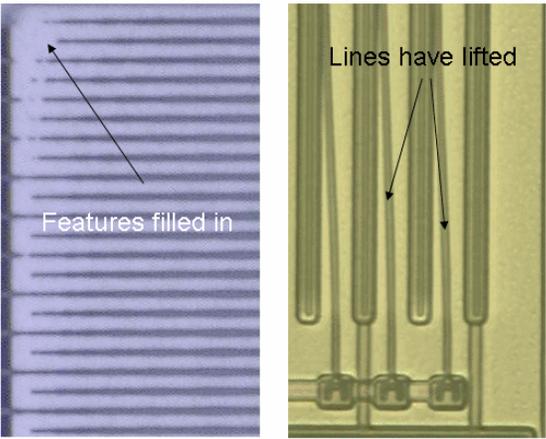
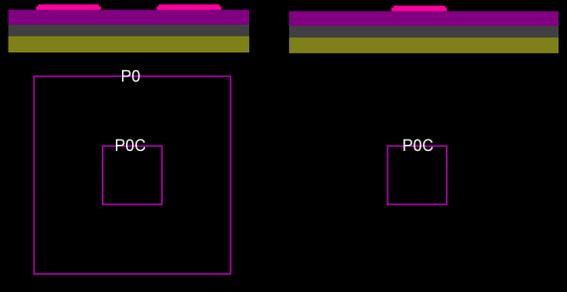
<p>ERR_D4C_P4C_S_LT_0PT5</p>	<p>dimple4_cut space to poly4_cut less than 0.5µm</p>	<p>0.5 µm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p>	 <p>Simulated Problem</p>
<p>ERR_D4C_S_LT_1</p>	<p>dimple4_cut space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p> <p>Cuts next to each other can merge together, and lines can be considerably thinner than intended.</p>	 <p>Example of merged features Less Than 1.0 um rule (...LT_1)</p>

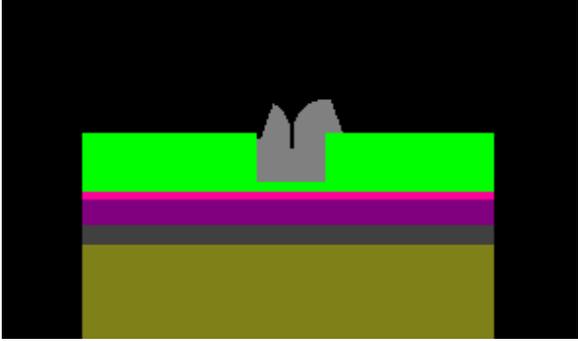
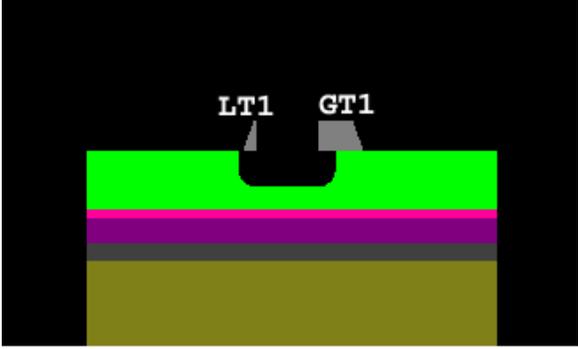
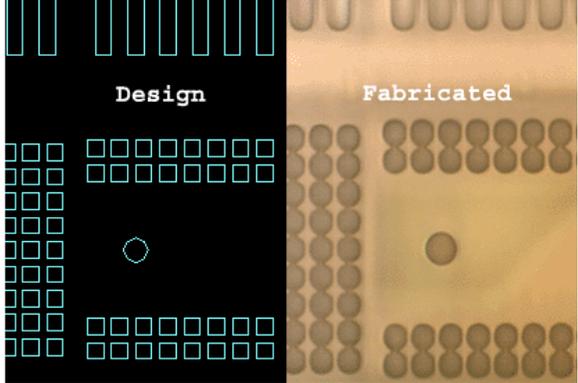
<p>ERR_D4C_W_LT_1PT5</p>	<p>dimple4_cut width less than 1.5μm</p>	<p>Dimple 4 backfill will close feature by 0.2 μm on either side. Process variations could create a closed off feature that may have a void (keyhole), unexpected sharp tip, or less than full depth etch.</p>	 <p>Simulated Problem</p>
<p>ERR_D4C_X4C_S_LT_1</p>	<p>dimple4_cut space to sacox4_cut less than 1μm</p>	<p>Dimple4 and SacOx4 Cut can merge together when features are too close to each other. Photo lithographic alignment tolerances and the sidewall slope can combine to create a single feature rather than what was intended.</p>	 <p>Simulated Problem</p>

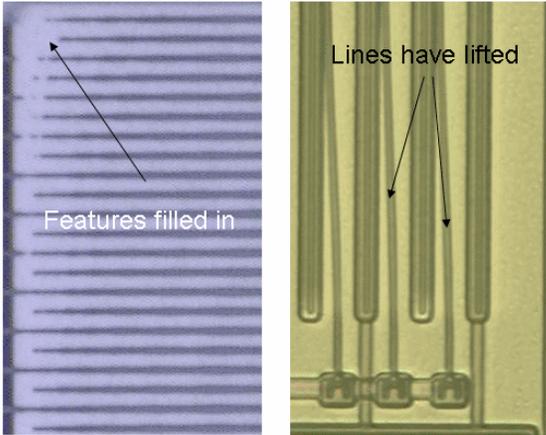
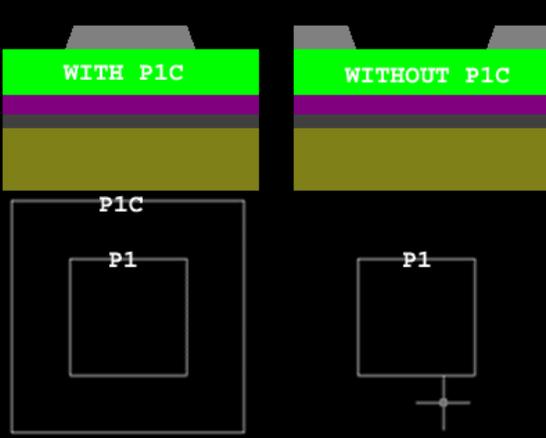
<p>ERR_INVALID_SACOX3_AN CHR</p>	<p>sacox3_cut anchor to poly2 area less than 3.14μm^2</p>	<p>Less than 3.14 μm^2 area anchor cuts could be insufficient in creating a strong connection. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. The anchor contact point could be small enough that it could break off and float away.</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_INVALID_SACOX4_AN CHR</p>	<p>sacox4_cut anchor to poly3 area less than 3.14μm^2</p>	<p>Less than 3.14 μm^2 area anchor cuts could be insufficient in creating a strong connection. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. The anchor contact point could be small enough that it could break off and float away.</p>	 <p style="text-align: center;">Simulated Problem</p>

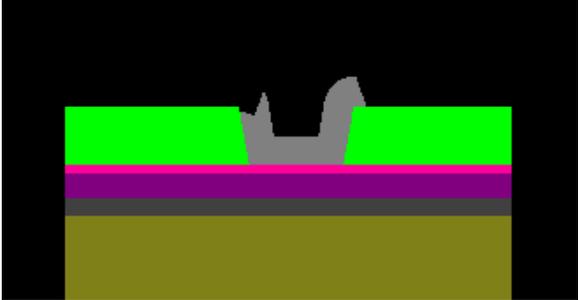
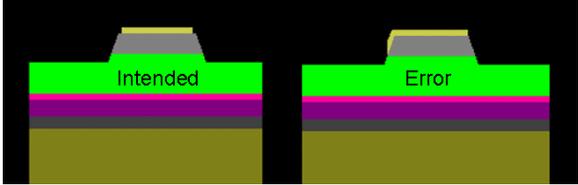
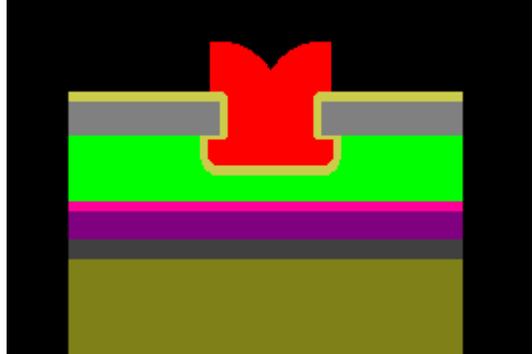
<p>ERR_NIC_EDGE_WO_P0</p>	<p>nitride_cut edge without poly0</p>	<p>This error produces an open path to the thermal Oxide isolation layer below the Nitride layer. If the error is violated the structures could float away or be severely degraded.</p>	 <p>Oxide Undercut During Release</p>
<p>ERR_NIC_EDGE_WO_P1</p>	<p>nitride_cut edge without poly1</p>	<p>This error could produce an open path to the thermal Oxide isolation layer below the Nitride layer. If the error is violated the structures could float away or be severely degraded.</p> <p>Studies have shown that without P1 covering the P0, an open path to the thermal oxide is possible.</p>	 <p>Oxide Undercut During Release</p>

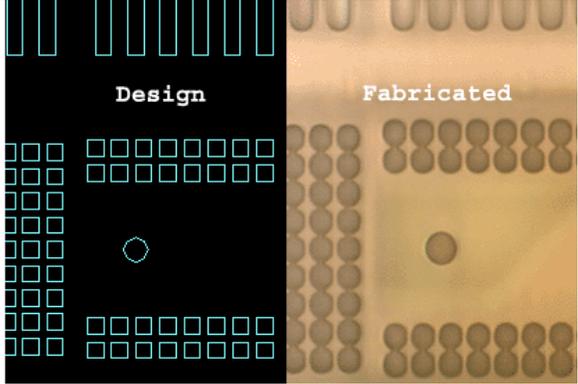
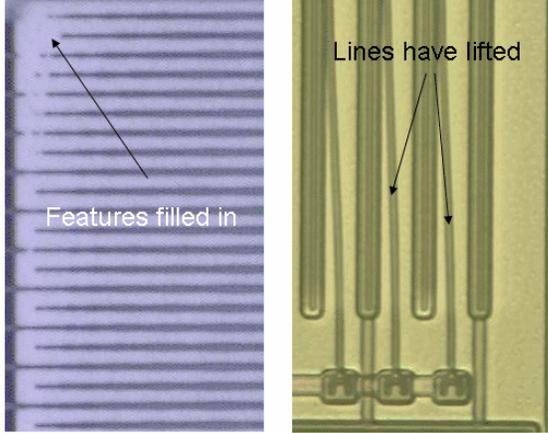
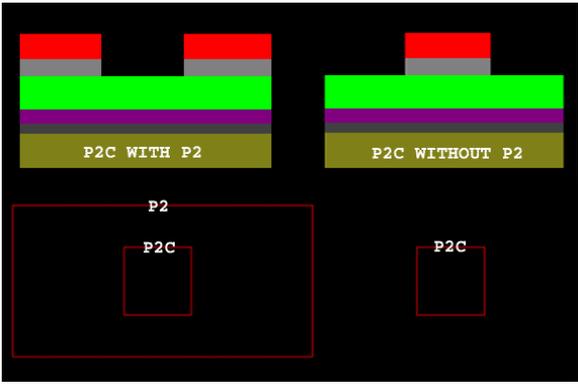
ERR_NIC_S_LT_1	nitride_cut space less than 1µm	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p> <p>Cut features can merge together when features are too close to each other.</p>	 <p style="text-align: center;">Simulated Problem</p>
ERR_NIC_W_LT_1	nitride_cut width less than 1µm	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p> <p>Cuts less than 1.0 micron may not completely clear during photolithography and cause an insufficient connection to substrate.</p>	 <p style="text-align: center;">Simulated Problem</p>
ERR_P0_S_LT_1	mmpoly0 space less than 1µm	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p style="text-align: center;">Example of merged features Less Than 1.0 um rule (...LT_1)</p>

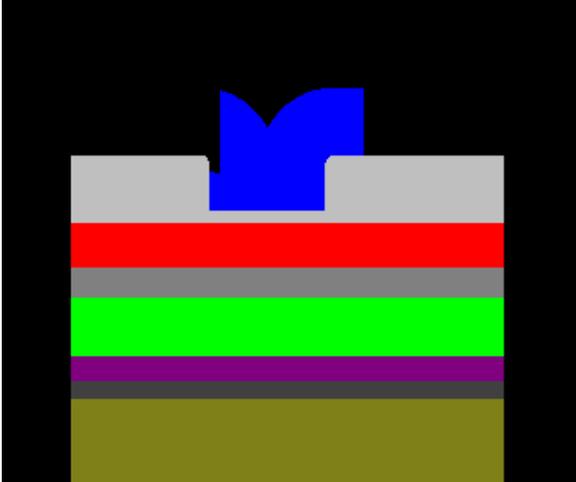
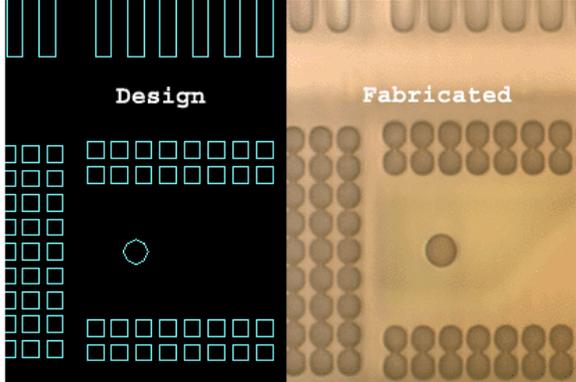
<p>ERR_P0_W_LT_1</p>	<p>mmpoly0 width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. Can result in lifting patterns, or no pattern.</p>	 <p>Lifting and Unresolved Features</p>
<p>ERR_P0_X1C_E_LT_0PT5</p>	<p>mmpoly0 enclosure of sacox1_cut less than 0.5µm</p>	<p>0.5 µm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p>	 <p>Simulated Problem</p>
<p>ERR_P0C_WITHOUT_P0</p>	<p>mmpoly0_cut without mmpoly0</p>	<p>Unintended geometry. Poly0_Cut will be interpreted as Poly0 by the mask conversion process if there is no Poly0 enclosing it.</p>	 <p>Simulated Problem</p>

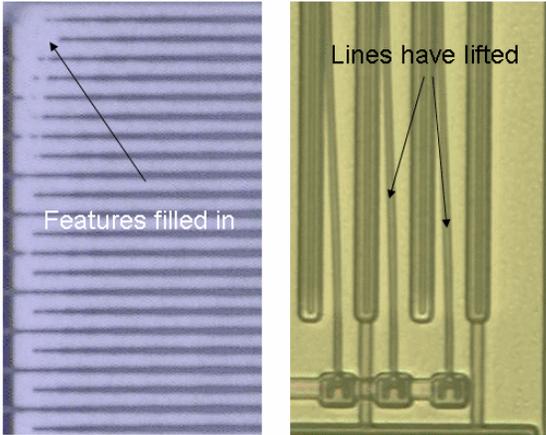
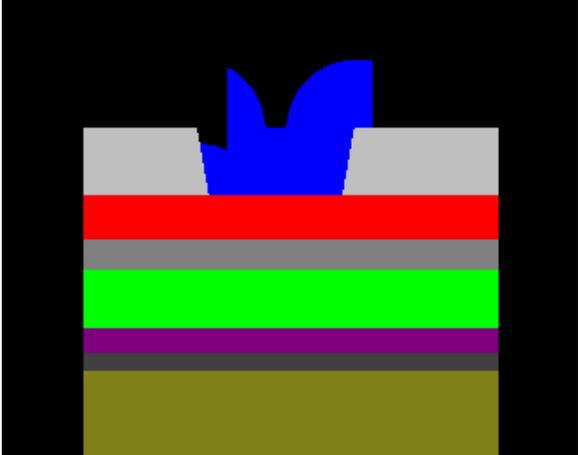
<p>ERR_P1_D1C_E_LT_0PT5</p>	<p>mmpoly1 enclosure of dimple1_cut less than 0.5μm</p>	<p>0.5 μm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_P1_PJC_E_LT_1</p>	<p>mmpoly1 enclosure of pin_joint_cut less than 1μm</p>	<p>The Poly1 sidewall etch profile has more of a sidewall angle and process bias than other Polysilicon layers, the 1.0 μm minimum enclosure rule is to insure that no unwanted geometry is created. The example shows how the error can create a floating P1 feature if Less Than 1 μm (LT1).</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_P1_S_LT_1</p>	<p>mmpoly1 space less than 1μm</p>	<p>1.0 μm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p style="text-align: center;">Example of merged features Less Than 1.0 μm rule (...LT_1)</p>

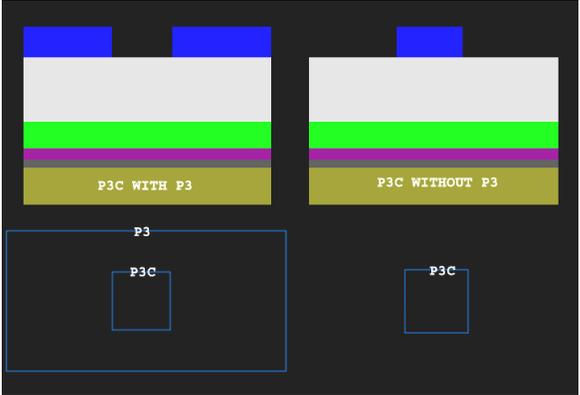
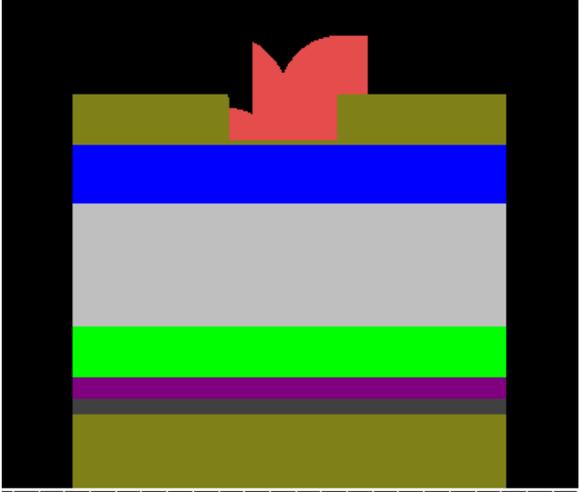
<p>ERR_P1_W_LT_1</p>	<p>mmpoly1 width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. Can result in lifting patterns, or no pattern.</p>	 <p>The left micrograph shows a blue-tinted image of horizontal lines with an arrow pointing to a region where the lines are blurred and filled together, labeled 'Features filled in'. The right micrograph shows a green-tinted image of vertical lines with an arrow pointing to a region where the lines are broken and curved upwards, labeled 'Lines have lifted'.</p> <p>Lifting and Unresolved Features</p>
<p>ERR_P1_WITHOUT_P1C</p>	<p>mmpoly1 without mmpoly1_cut</p>	<p>Poly1 will be left un-etched unless there is a Poly1_Cut level defined. The reason this differs from other layer '_Cut strategies is to facilitate the creation of Poly1/Poly2 laminate. Rather than having to define the P1P2 layer twice, the P1 layer is always left un-etched unless defined otherwise.</p>	 <p>The diagram shows two cross-sectional views of a layered structure. The top layer is green, the middle is purple, and the bottom is olive. Below these are two square regions labeled 'P1C' and 'P1'. In the 'WITH P1C' case, the P1C layer is present above the P1 layer. In the 'WITHOUT P1C' case, the P1C layer is absent, and the P1 layer is shown with a small crosshair at its base.</p> <p>Design Example</p>

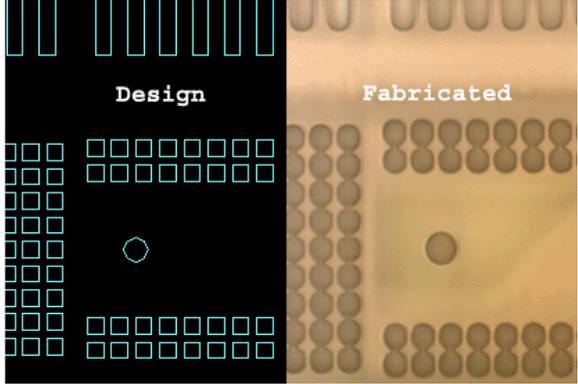
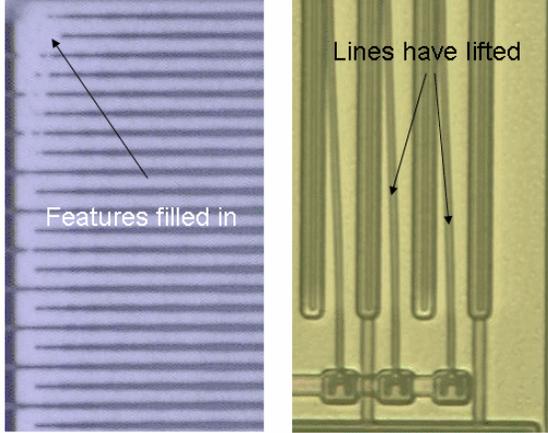
ERR_P1_X1C_E_LT_0PT5	mmpoly1 enclosure of sacox1_cut less than 0.5 μ m	0.5 μ m is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.	 <p style="text-align: center;">Simulated Problem</p>
ERR_P1C_X2_E_LT_0PT5	mmpoly1_cut enclosure of sacox2 less than 0.5 μ m	0.5 μ m is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.	 <p style="text-align: center;">Simulated Problem</p>
ERR_P2_PJC_E_LT_1	mmpoly2 enclosure of pin_joint_cut less than 1 μ m	This layer combination is used for creating Pin Joints and Hubs. Because of the Sacox2 spacer layer the flange above the Pin Joint/Hub must be a minimum of 1.0 μ m to insure the joint will not pull out from below the flange.	 <p style="text-align: center;">Simulated Problem</p>

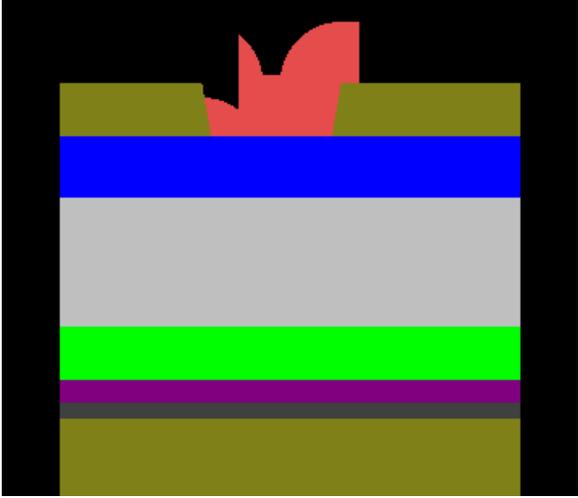
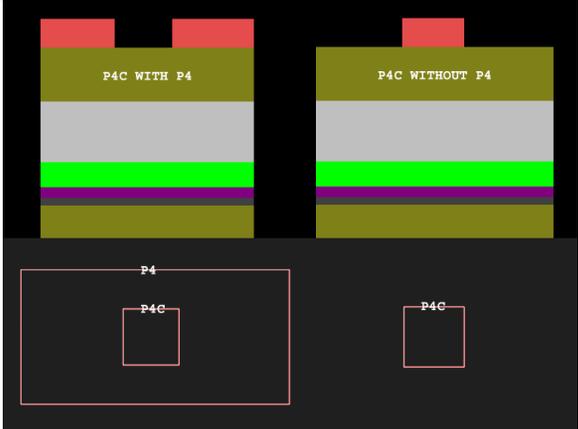
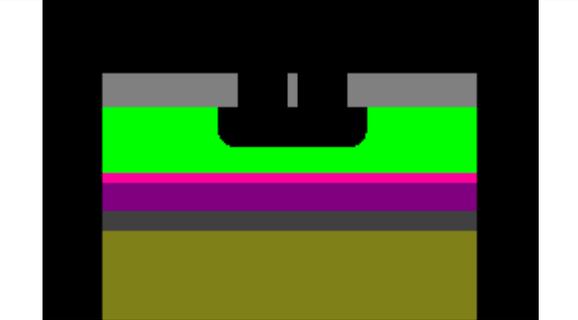
<p>ERR_P2_S_LT_1</p>	<p>mmpoly2 space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p>Example of merged features Less Than 1.0 um rule (...LT_1)</p>
<p>ERR_P2_W_LT_1</p>	<p>mmpoly2 width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. Can result in lifting patterns, or no pattern.</p>	 <p>Lifting and Unresolved Features</p>
<p>ERR_P2C_WITHOUT_P2</p>	<p>mmpoly2_cut without mmpoly2</p>	<p>Unintended geometry. Poly2_Cut will be interpreted as Poly2 by the mask conversion process if there is no Poly2 enclosing it.</p>	 <p>Design Example</p>

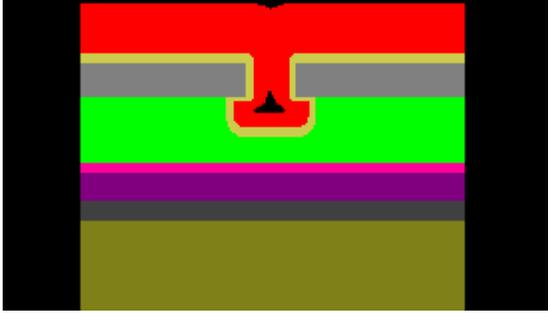
<p>ERR_P3_D3C_E_LT_0PT5</p>	<p>mmpoly3 enclosure of dimple3_cut less than 0.5μm</p>	<p>0.5 μm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_P3_S_LT_1</p>	<p>mmpoly3 space less than 1μm</p>	<p>1.0 μm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p style="text-align: center;">Example of merged features Less Than 1.0 um rule (...LT_1)</p>

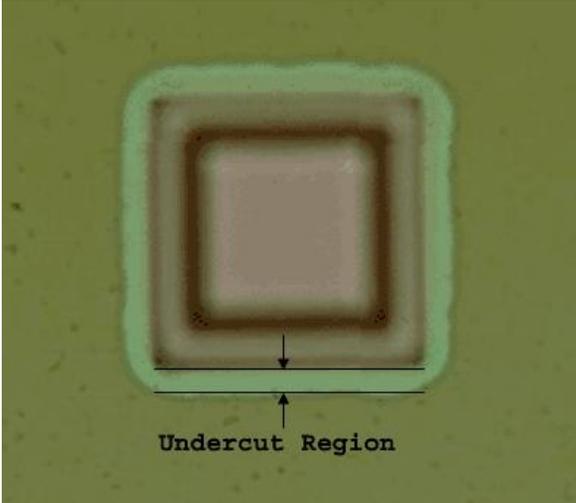
<p>ERR_P3_W_LT_1</p>	<p>mmpoly3 width less than 1μm</p>	<p>1.0 μm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. Can result in lifting patterns, or no pattern.</p>	 <p>Lifting and Unresolved Features</p>
<p>ERR_P3_X3C_E_LT_OPT5</p>	<p>mmpoly3 enclosure of sacox3_cut less than 0.5μm</p>	<p>0.5 μm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p> <p>D3 must be enclosed by P3 so as to fill the dimple feature completely.</p>	 <p>Simulated Problem</p>

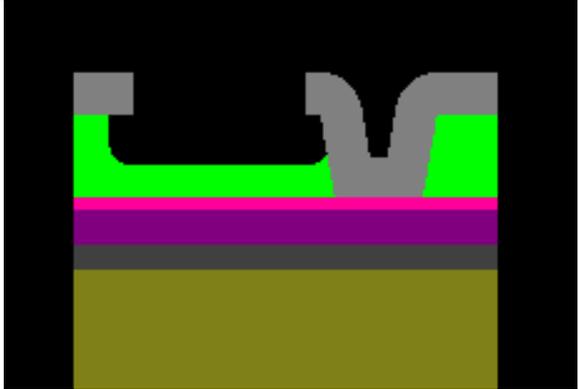
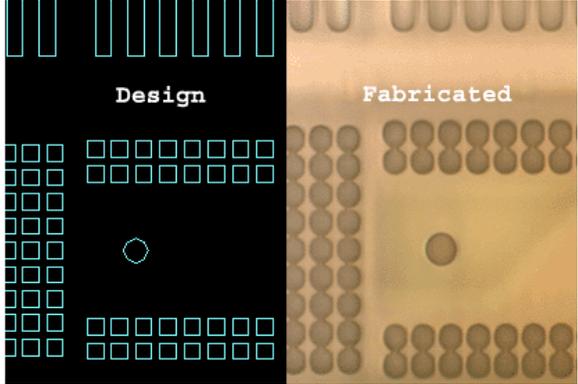
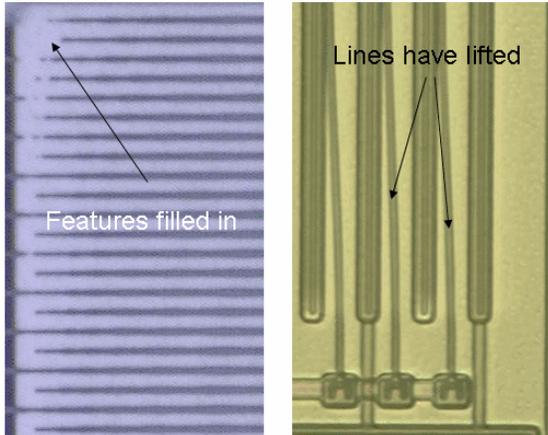
<p>ERR_P3C_WITHOUT_P3</p>	<p>mmpoly3_cut without mmpoly3</p>	<p>Unintended geometry. Poly3_Cut will be interpreted as Poly3 by the mask conversion process if there is no Poly3 enclosing it.</p>	 <p>Design Example</p>
<p>ERR_P4_D4C_E_LT_OPT5</p>	<p>mmpoly4 enclosure of dimple4_cut less than 0.5µm</p>	<p>0.5 µm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p>	 <p>Simulated Problem</p>

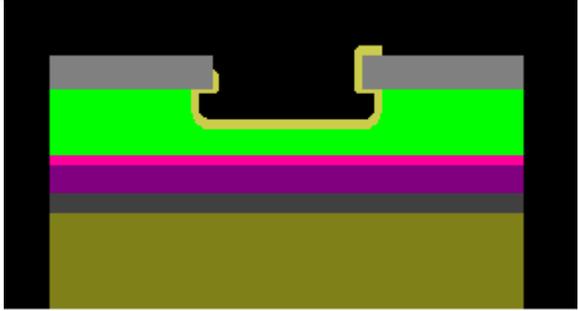
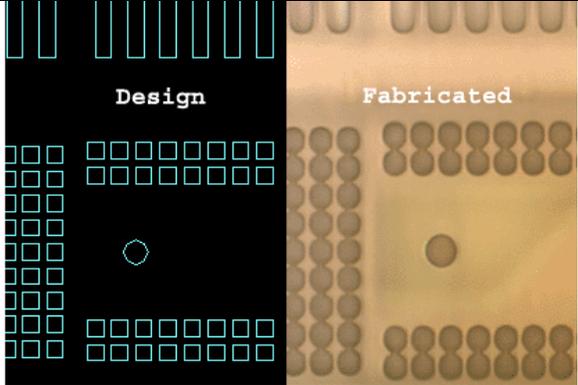
<p>ERR_P4_S_LT_1</p>	<p>mmpoly4 space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p>Example of merged features Less Than 1.0 um rule (...LT_1)</p>
<p>ERR_P4_W_LT_1</p>	<p>mmpoly4 width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. Can result in lifting patterns, or no pattern.</p>	 <p>Lifting and Unresolved Features</p>

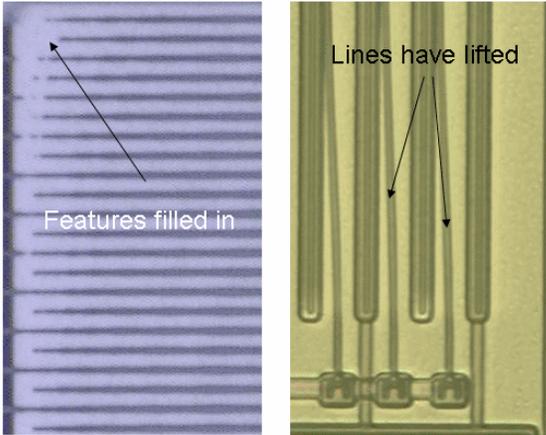
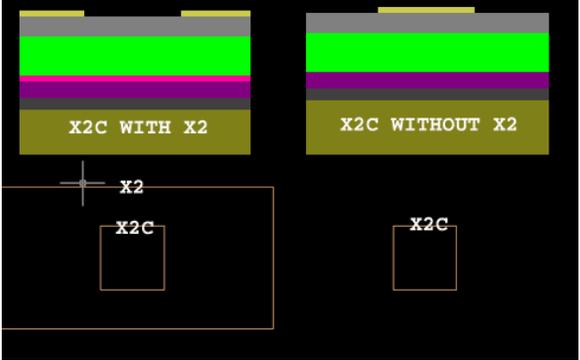
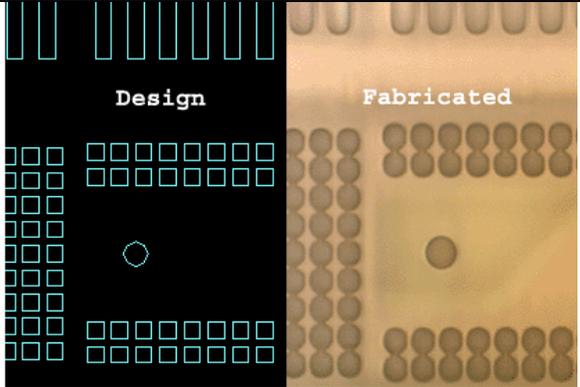
<p>ERR_P4_X4C_E_LT_0PT5</p>	<p>mmpoly4 enclosure of sacox4_cut less than 0.5μm</p>	<p>0.5 μm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p> <p>D4 must be enclosed by P4 so as to fill the dimple feature completely.</p>	 <p>Simulated Problem</p>
<p>ERR_P4C_WITHOUT_P4</p>	<p>mmpoly4_cut without mmpoly4</p>	<p>Unintended geometry. Poly4_Cut will be interpreted as Poly4 by the mask conversion process if there is no Poly4 enclosing it.</p>	 <p>Design Example</p>
<p>ERR_PJC_S_LT_1</p>	<p>pin_joint_cut space less than 1μm</p>	<p>When the pin_joint_cut spacing is less than 1 μm, there is the possibility of a floater being created, or some unintentional geometry. The Pinjoint undercut etch can meet below the P1 which will lock the pinjoint or hub .</p>	 <p>Simulated Problem</p>

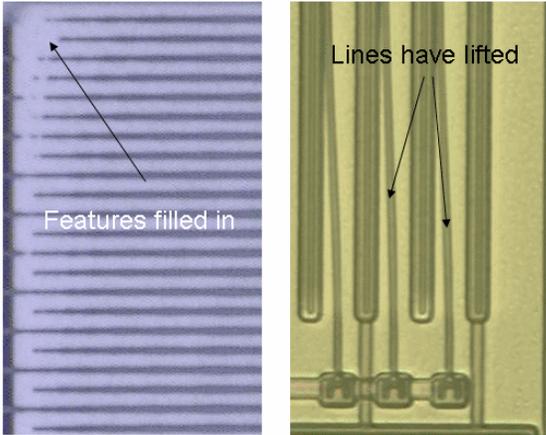
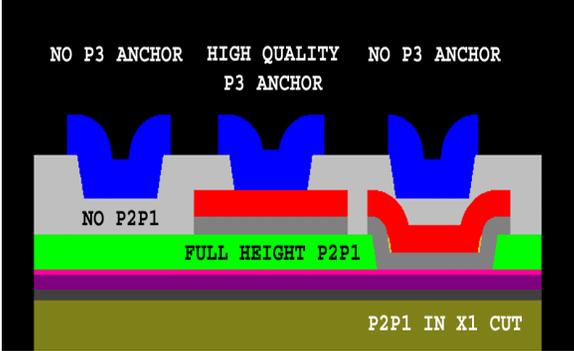
<p>ERR_PJC_W_LT_3</p>	<p>pin_joint_cut width less than 3μm</p>	<p>When the pin joint undercut is filled with poly2, if the space is not adequate, the sidewalls can touch each other prior to complete filling of the undercut region leading to a hollow pin or cause pin failure.</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_X1C_NIC_E_LT_OPT5</p>	<p>sacox1_cut enclosure of nitride_cut less than 0.5μm</p>	<p>0.5 μm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p>	 <p style="text-align: center;">Simulated Problem</p>

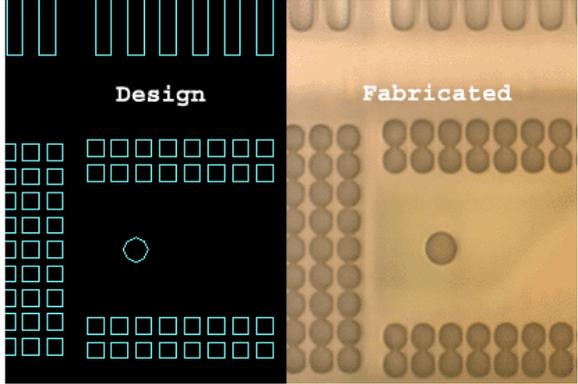
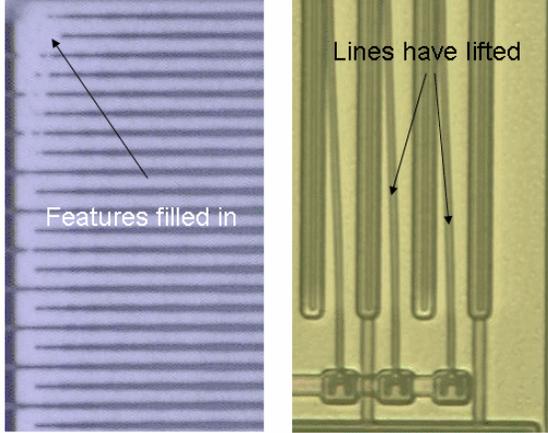
<p>ERR_X1C_NIC_UNDERLAP_LT_6PT5</p>	<p>sacox1_cut underlap of large nitride_cut less than 6.5µm</p>	<p>Empirical data has shown that there is a risk of P0 degradation due to cracking or pinhole formation at the P0 to Nitride cut interface that can lead to undercutting of the thermal oxide during release. The minimum of 6.5 µm of P1 in contact with the P0 layer was determined from experiment.</p>	 <p style="text-align: center;">Oxide Undercut During Release</p>
<p>ERR_X1C_P1C_S_LT_0PT5</p>	<p>sacox1_cut space to poly1_cut less than 0.5µm</p>	<p>0.5 µm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result.</p>	 <p style="text-align: center;">Simulated Problem</p>

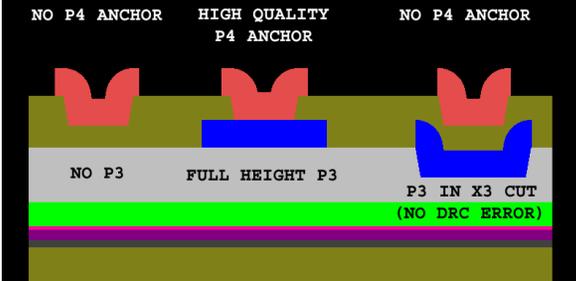
<p>ERR_X1C_PJC_S_LT_1</p>	<p>sacox1_cut space to pin_joint_cut less than 1µm</p>	<p>Unintended geometry could arise due to this error. The pin joint undercut will not be fully realized if the Sacox1_cut is too close to the pin_joint_cut.</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_X1C_S_LT_1</p>	<p>sacox1_cut space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p style="text-align: center;">Example of merged features Less Than 1.0 um rule (...LT_1)</p>
<p>ERR_X1C_W_LT_1</p>	<p>sacox1_cut width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. Can result in lifting patterns, or no pattern.</p>	 <p style="text-align: center;">Lifting and Unresolved Features</p>

<p>ERR_X2_PJC_E_LT_OPT5</p>	<p>sacox2 enclosure of pin_joint_cut less than 0.5µm</p>	<p>0.5 µm is the photo lithographic alignment tolerance stated in the design rules. Unintended geometry could arise due to this error. During photo lithography, registration can be slightly misaligned from layer to layer due to topography as well as stress in the wafer. Alignment can vary from the center to edge of the wafer as well. If a feature on an upper layer overlaps the edge of a feature on a lower level the etch process could create the unintended result. Hub or pin joint could be locked due to this error.</p>	 <p style="text-align: center;">Simulated Problem</p>
<p>ERR_X2_S_LT_1</p>	<p>sacox2 space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p style="text-align: center;">Example of merged features Less Than 1.0 um rule (...LT_1)</p>

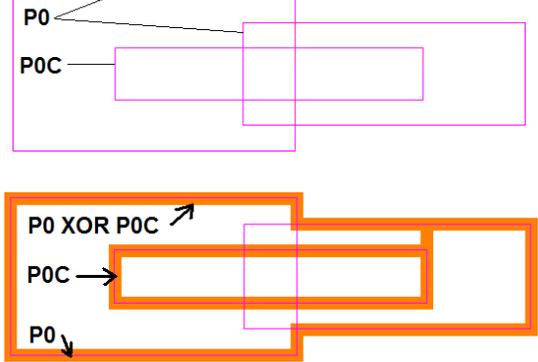
<p>ERR_X2_W_LT_1</p>	<p>sacox2 width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. Can result in lifting patterns, or no pattern.</p>	 <p>Lifting and Unresolved Features</p>
<p>ERR_X2C_WITHOUT_X2</p>	<p>sacox2_cut without sacox2</p>	<p>Unintended geometry. SacOx2_Cut will be interpreted as SacOx2 by the mask conversion process if there is no SacOx2 enclosing it.</p>	 <p>Design Example</p>
<p>ERR_X3C_S_LT_1</p>	<p>sacox3_cut space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p>Example of merged features Less Than 1.0 um rule (...LT_1)</p>

<p>ERR_X3C_W_LT_1</p>	<p>sacox3_cut width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer. Can result in lifting patterns, or no pattern.</p>	 <p>Lifting and Unresolved Features</p>
<p>ERR_X3C_WITHOUT_P2P1</p>	<p>sacox3_cut without full height mmpoly2</p>	<p>Sacox3_Cut typically is used to create an anchor cut for Poly3 to Poly2/Poly1. If the Poly2/Poly1 is not present or less than full height, the connection will not be created or could fail. Sacox3_cut layer assumes there is a Poly2/Poly1 landing material. The etch process includes a substantial over etch with high Oxide to polysilicon selectivity. The MMPoly3 feature will extend below the lower level Poly2/Poly1 layer surface and can cause interference or unintentional locking of moving parts.</p>	 <p>Design Examples</p>

<p>ERR_X4C_S_LT_1</p>	<p>sacox4_cut space less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p>Example of merged features Less Than 1.0 um rule (...LT_1)</p>
<p>ERR_X4C_W_LT_1</p>	<p>sacox4_cut width less than 1µm</p>	<p>1.0 µm is the design rule limit for features on the same layer. Photolithography step may not resolve feature as intended. Results will vary over surface of wafer.</p>	 <p>Lifting and Unresolved Features</p>

ERR_X4C_WITHOUT_P3	sacox4_cut without mmpoly3	<p>Sacox4_Cut typically is used to create an anchor cut for Poly4 to Poly3. If the Poly3 is not present, no connection will be created. Sacox4_cut layer assumes there is a poly3 landing material. The etch process includes a substantial over etch with high Oxide to polysilicon selectivity. The MMPoly4 feature will extend below the lower level polysilicon layer surface and can cause interference or unintentional locking of moving parts.</p> <p>If P3 is down in a X3 Cut, the Poly4 level will not anchor. This error is not flagged by the DRC.</p>	 <p style="text-align: center;">Design Examples</p>
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INFO Descriptions – to be used for viewing only (limited to the first 1000 objects per layer).

INF_POLY0	INF_POLY0	Information layer depicting P0 and P0C polygons are XORed together onto layer INF_POLY0.	
INF_POLY1	INF_POLY1	Information layer depicting P1C and P1 polygons are XORed together onto layer INF_POLY1. Also any P1 created by X2 will be shown based on rules discussed in the design guide.	See INF_POLY0 example above.
INF_POLY2	INF_POLY2	Information layer depicting P2 and P2C polygons are XORed together onto layer INF_POLY2.	See INF_POLY0 example above.

INF_POLY3	INF_POLY3	Information layer depicting P3 and P3C polygons are XORed together onto layer INF_POLY3.	See INF_POLY0 example above.
INF_POLY4	INF_POLY4	Information layer depicting P4 and P4C polygons are XORed together onto layer INF_POLY4.	See INF_POLY0 example above.
INF_SACOX1_CUT	INF_SACOX1_CUT	Information layer depicting X1C polygons are ORed together onto layer INF_SACOX1_CUT.	
INF_SACOX2	INF_SACOX2	Information layer depicting X2 and X2C polygons XORed together onto layer INF_SACOX2.	See INF_POLY0 example above.
INF_SACOX3_CUT	INF_SACOX3_CUT	Information layer depicting X3C polygons ORed together onto layer INF_SACOX3_CUT.	See INF_SACOX1_CUT example above.
INF_SACOX4_CUT	INF_SACOX4_CUT	Information layer depicting X4C polygons ORed together onto layer INF_SACOX4_CUT.	See INF_SACOX1_CUT example above.
-1	Unexpected ICgraph error.	This message indicates that the DRC engine has failed to handle the geometry:. Please report this to drt@sandia.gov .	