Radiation-Hardened Point-of-Load Power Conversion

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Problem

Powering Digital Systems in High-rad Environments

Increased Computing Performance

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Higher Clock Frequency, Smaller Feature Sizes

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Low Voltage, High Current

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Efficient RH Distributed Power System

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Efficient RH Point-of-Load Converters

RH Power FETs | RH Controller IC

Objective - Develop radiation-hardened power MOSFET and HVCMOS technologies that enable an order-of-magnitude improvement in the size and efficiency of point-of-load converters for processor applications high radiation environments.

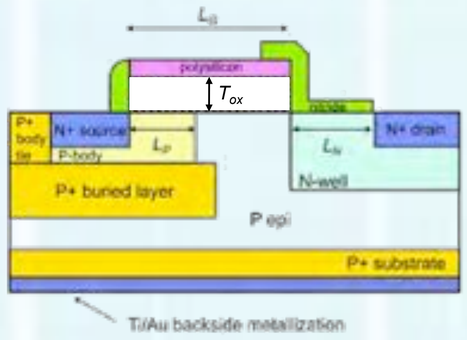
Primary Requirements

- Total dose tolerant to > 100 KRad
- Latch-up Immune
- No SEE to LET > 80 MeV-cm²/mg
- Switching frequency > 300 kHz
- Target efficiency > 90%

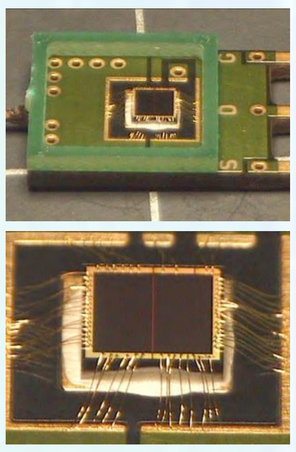
Approach

Rad-Hard Power FET

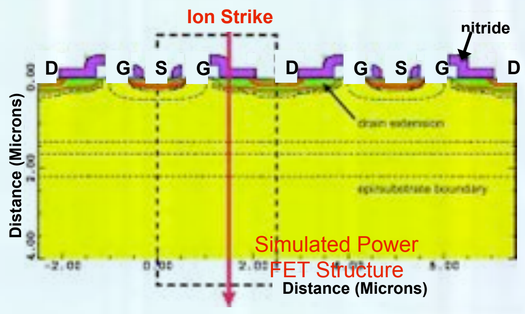
3rd Iteration design with improved body tie

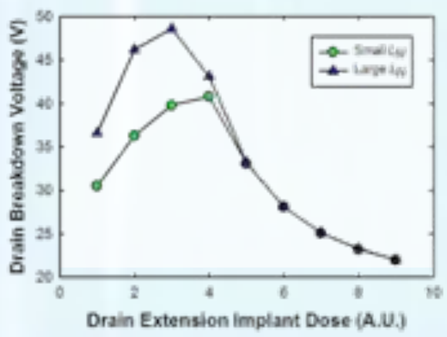


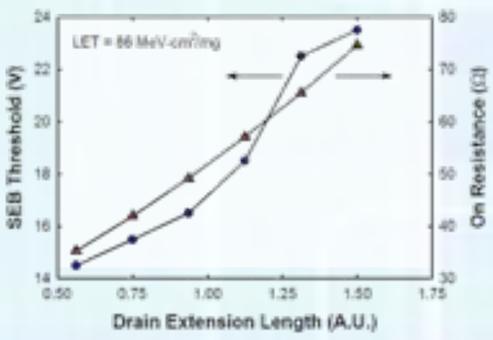
Chip-on-board mounting for radiation and electrical testing



Simulations were used to optimize drain extension process and design parameters

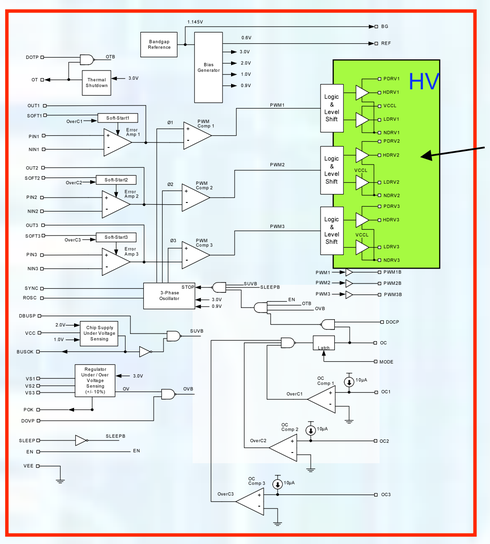






Approach (cont.)

Rad-Hard HVCMOS Controller IC

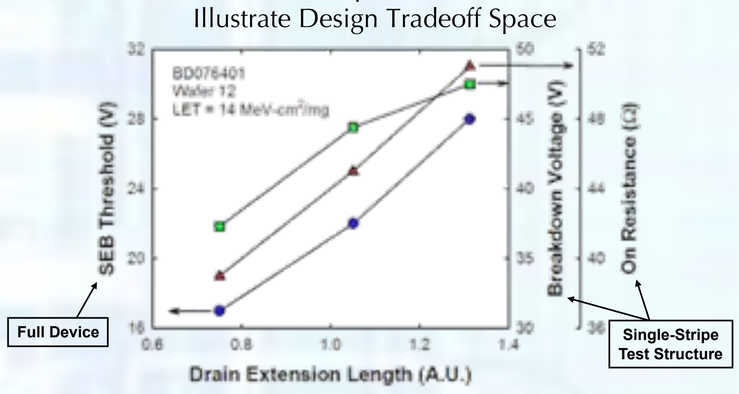


Primary goals are to develop devices with 20+ volt breakdown and dual gate technology within the CMOS7 platform

Results

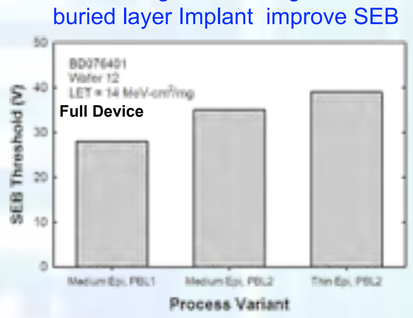
Rad-Hard Power FET

New Devices Show Improved SEB Threshold and Illustrate Design Tradeoff Space

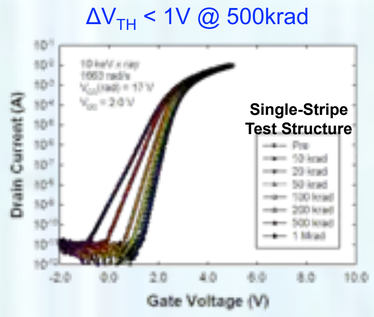


SEB threshold in original devices for an LET of 14 MeV-cm²/mg was only ~12 V.

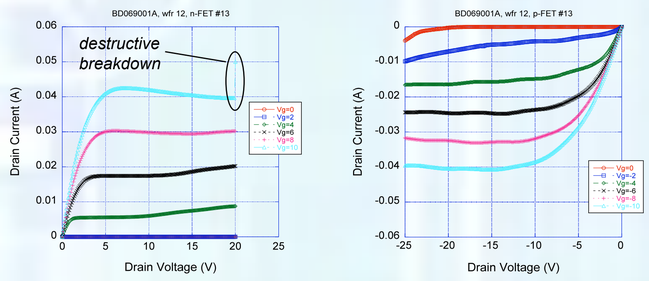
Process changes to starting material and buried layer Implant improve SEB



Total-dose Results: ΔV_{TH} < 1V @ 500krad



High Voltage (HV) CMOS SOI Development



- **Newest N-FETs achieve BV_{DSS} > 40V, newest P-FETs > 30V**
- **Highest breakdown voltage SOI devices ever made at the MDL!**
- **First co-processed SOI HV complementary (N & P) FETs at the MDL!**

Significance

Dramatic increases in computing performance will be required for Sandia's future remote sensing work. Distributed power and point-of-load power conversion will be essential to meet the requirements of the improved highly integrated, low-voltage digital processing components.

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