

MEMS-based Arrays of Micro Ion Traps for Quantum Simulation Scaling



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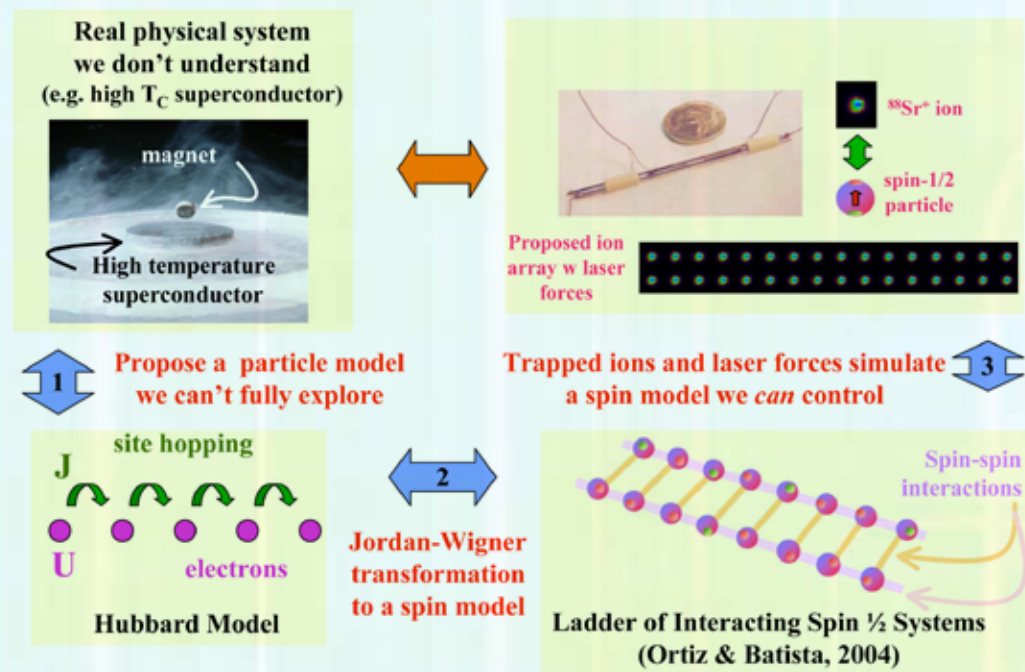
Goal:

Complete fabrication and custom packaging of 2-dimensional linear ion traps and test the trap in LANLs quantum simulation experimental apparatus.

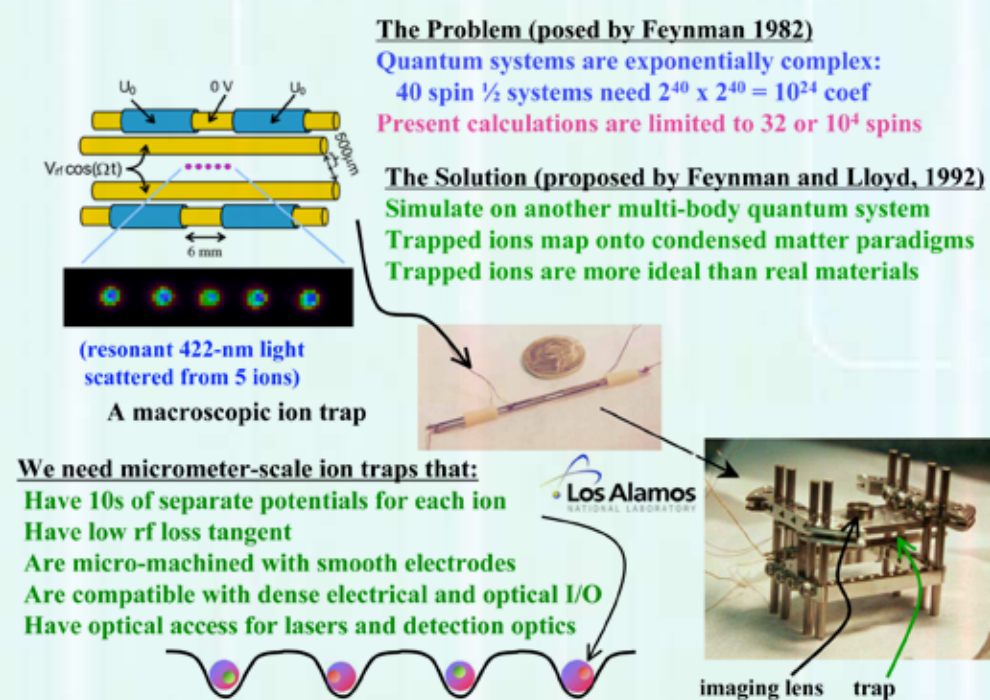
Milestone:

Layout masks; fabricate 2-D ion trap design; perform custom packaging and device release of traps; demonstrate ion trapping

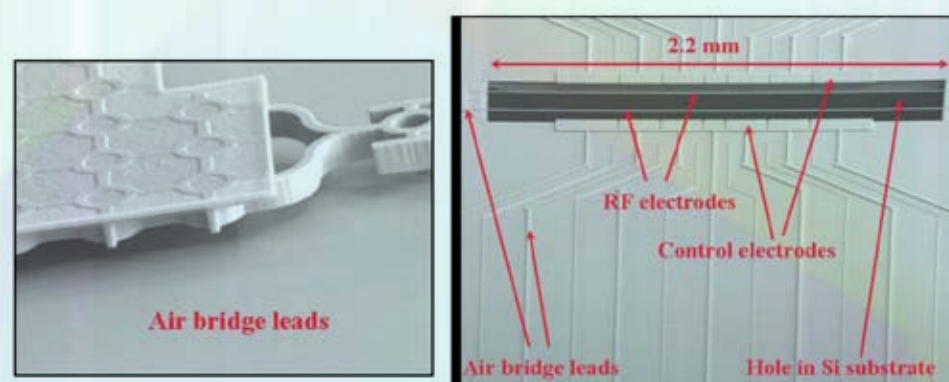
WHAT IS A QUANTUM SIMULATOR?



TRAPPED IONS FOR QUANTUM SIMULATION

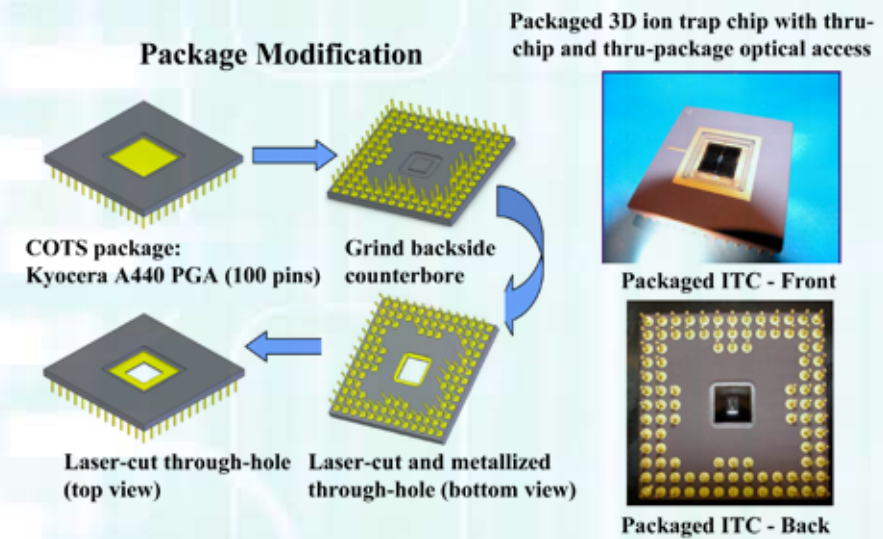


SANDIA ION TRAP CHIP (ITC) EXAMPLE



Sandia National Laboratories linear ion trap chips are micro-fabricated with a metal MEMS process. Planar metallic trap electrodes (W over coated with Au) and a hole through the Si substrate define the trapping region and allow 3D optical access for lasers to ions trapped between RF leads stretched lengthwise over the hole. Control electrodes at the hole edges define seven trapping segments. Air bridged metal leads reduce capacitance and RF dissipation to the substrate. Trapped ion images are from the ITC shown above.

KEY ACCOMPLISHMENT FOR MEMS ION TRAP CHIPS: DEVELOPING A COMMON PACKAGING PLATFORM



ANALYSIS OF PACKAGING MATERIALS PROPERTIES

Assembly of die, die attach and PGA used in FEA analyses.

		CTE ppm/C	Young's Modulus (GPa)	Yield Strength (MPa)	Thermal Conductivity (W/mK)
Kyocera A440 (Al_2O_3) ceramic	PGA package bulk	7.1	310	300	14
Elemental silicon (Si)	Die	2.49	112.4	120	124
Gallium Arsenide (GaAs)	Die	5.4	82.7	unk	50
Gold-Germanium (88Au12Ge) solder	Die attach	13	72.7	185	43.9
Saurisen cement	Die attach	4.68	300	1.7	1.6
JM7000 cyanate ester	Die attach	33	0.01	17.2	1.1
6061-T6 Aluminum	comparison	23.6	69	276	167
Mild steel	comparison	11.7	200	250	60.5

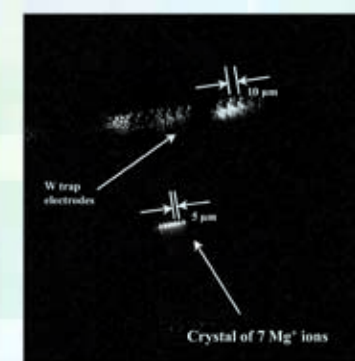
- Hard solders (Au-Si, 80Au20Sn and 88Au12Ge) are not flexible enough to accommodate large die.
- Epoxies were developed and readily used to mitigate the stress between die and package due to CTE mismatch.
- JM7000 was tested and successfully performs at 10^{-11} Torr after 300°C bake-out

SCIENCE BASED ENGINEERING OF A TRAP PACKAGING PLATFORM

FEA Results of Stress as a Function of Die Attach

- Non-linear analysis models the stresses in a bake-out operation from 20C to 300C.
- Results indicate that if the system were to achieve the bake temp, the max stress would be 1.66GPa (far exceeds the yield strengths of 1.7 MPa for Saurisen, 300 MPa for Al2O3 and 120 MPa of Si).
- The die or cement would break long before 300C was achieved.
- Non-linear analysis models the stresses in a die attach operation from 360C to 20C.
- Results indicate that if the system were to cool to room temp the max stress would be 405 MPa, exceeding the yield strength of AuGe (185 MPa), Si (120 MPa), and Al2O3 (300 MPa).
- The die would break or at least delaminate from package long before room temperature was achieved.
- Non-linear analysis models the stresses in a bake out operation from 20C to 300C (zero stress temp is 150C).
- Results indicate that if the system were to heat to 300C the max stress would be 107MPa occurring in the PGA (less than the 300 MPa yield strength of the Al2O3 and the 120 MPa yield strength of Si).

ION TRAPPING DEMONSTRATED IN SNL ION TRAP CHIP



Significance: This activity has addressed some critical questions by the intelligence community regarding the scalability of devices for quantum information processing (QIP).

QIP may address fundamental national security and intelligence problems and NW mission related materials, computation and information science problems.

Current/Potential Sponsors

- DOE
- DTO
- NIST
- DARPA
- LPS
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