



All-SiC Power Module for Grid-tied Energy Storage

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GeneSiC Semiconductor Inc.

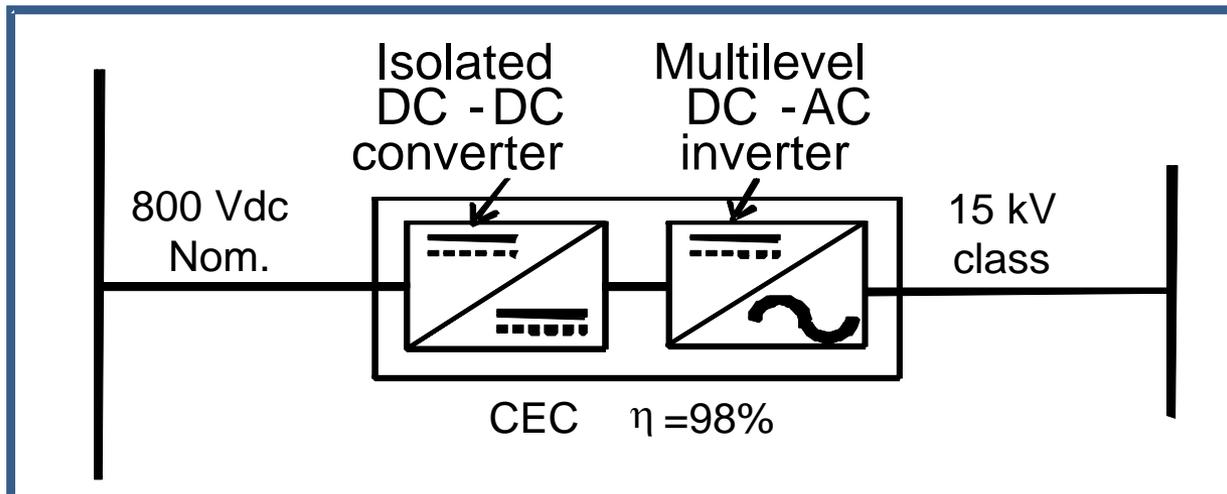
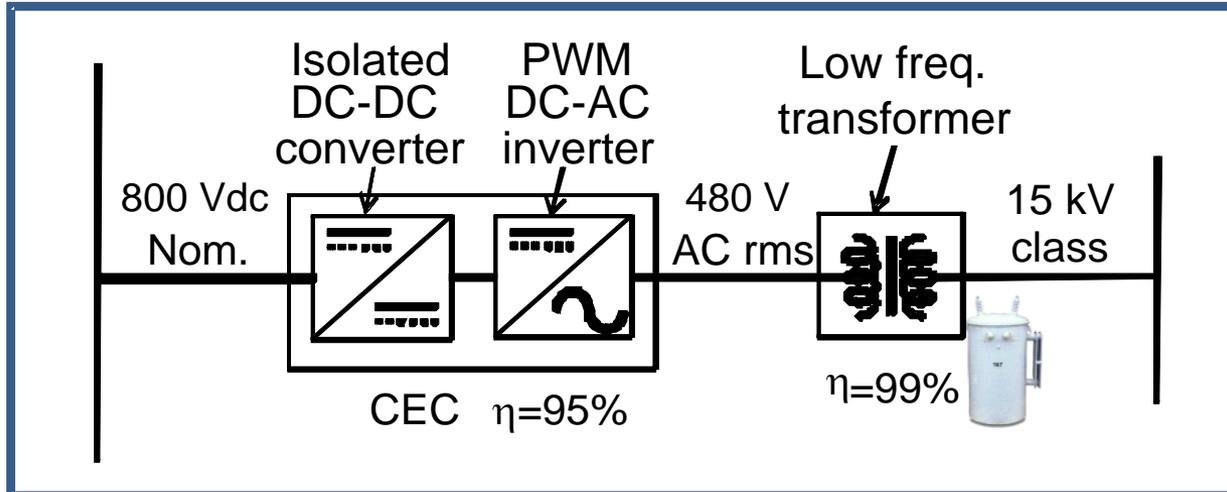
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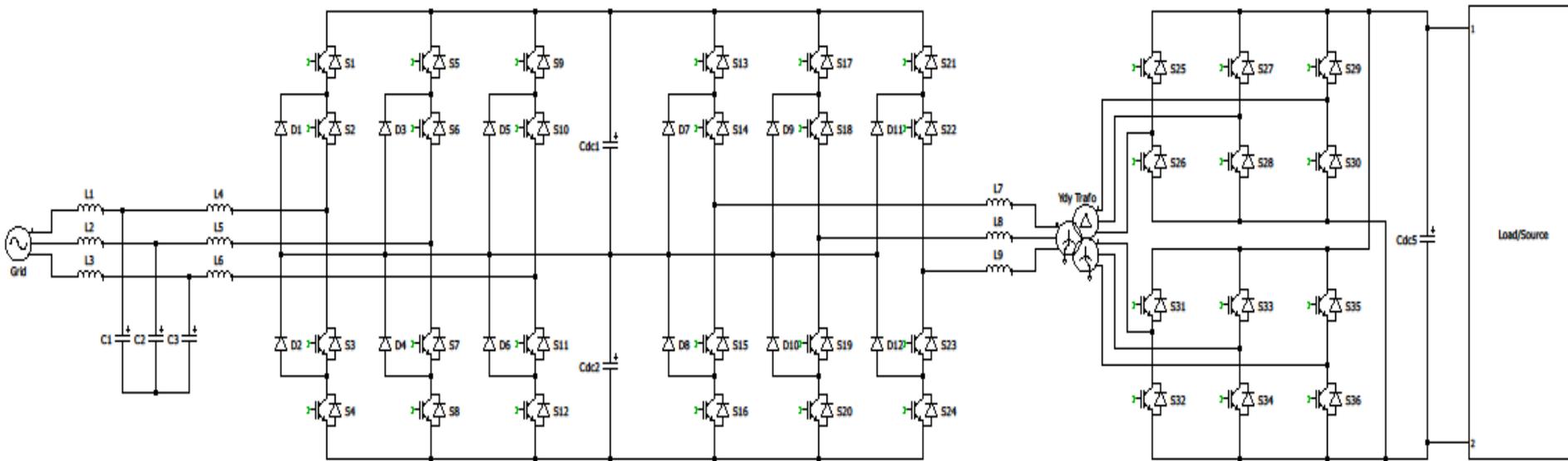
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Battery Energy Storage Power Electronics Architectures



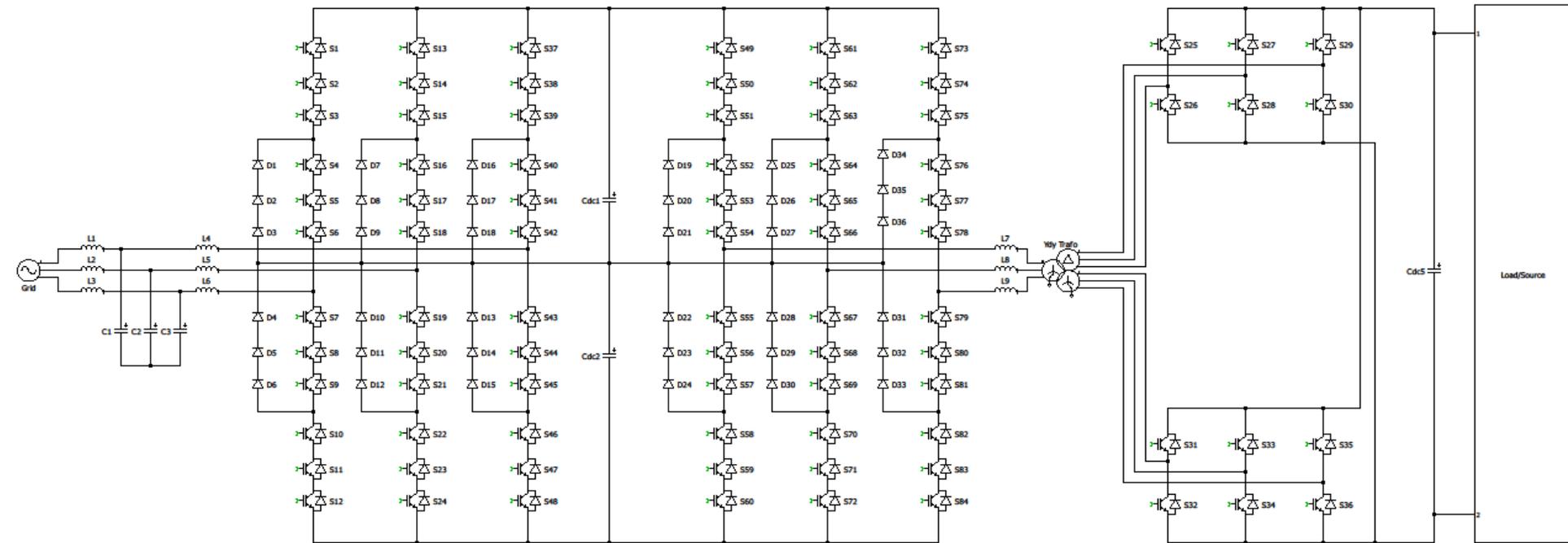
- Bidirectional, isolated DC-AC Power Conversion systems needed
- High Efficiencies are needed due to two-way power flow
- Compact systems help in wider deployments
- Low Frequency Transformer occupies space

Multi-level Converters using High Frequency commodity SiC Transistors



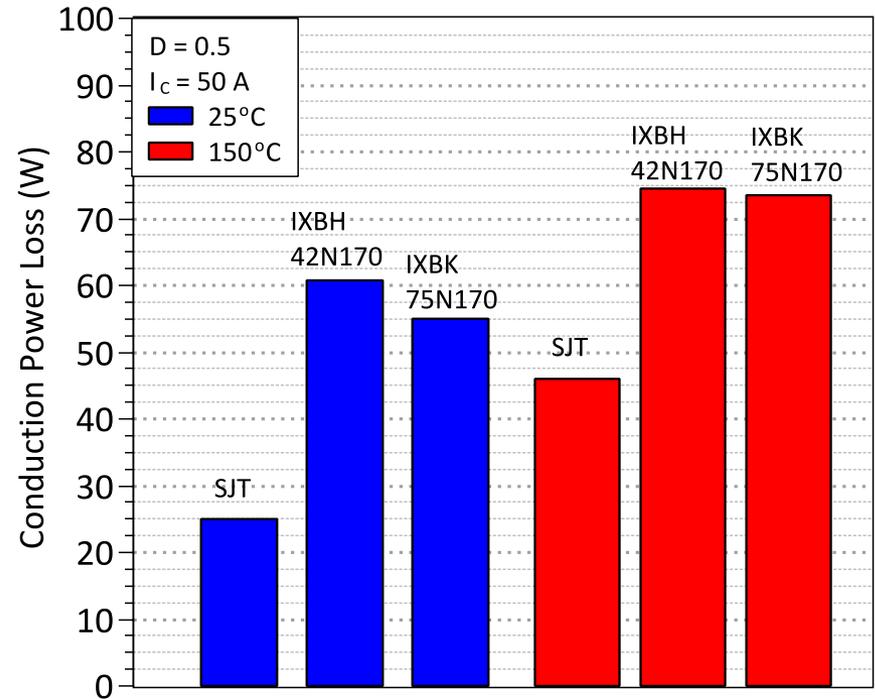
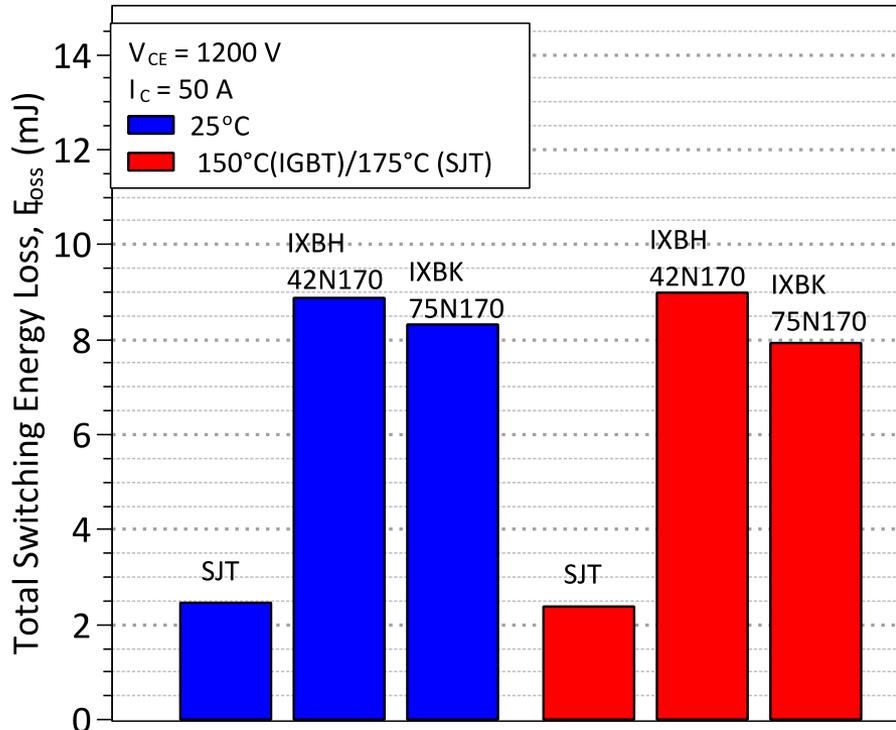
- Bidirectional 800 V grid-scale battery connections on secondary side
- 1700 V and 1200 V SiC devices required for high frequency secondary side connection

Compact, High Efficient Architecture enabled by High Voltage Devices



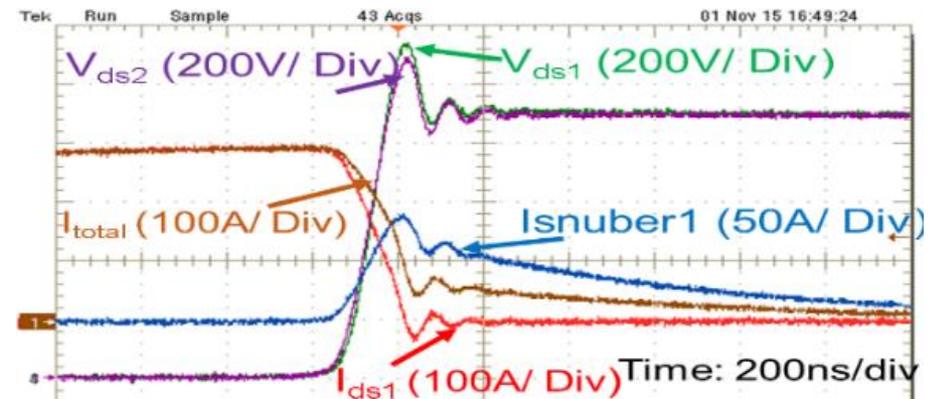
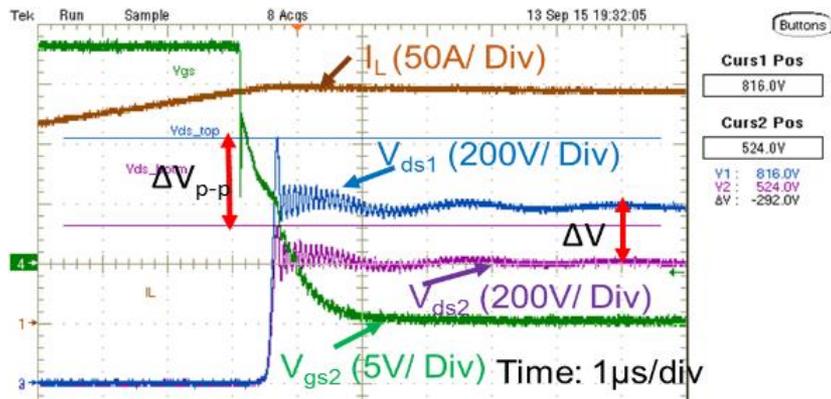
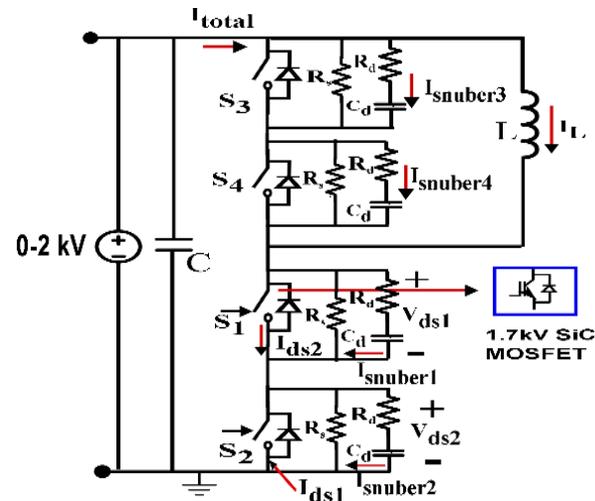
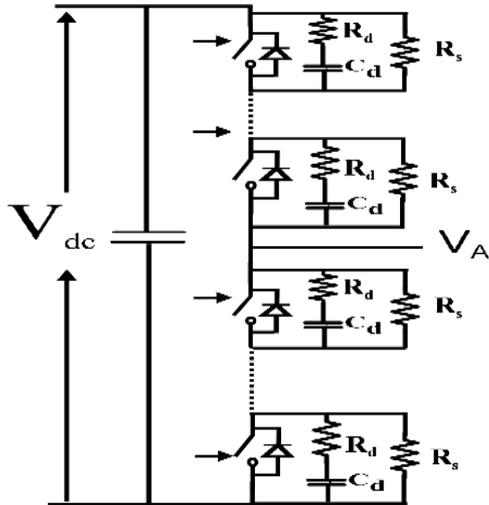
- SiC affords 1-3% increase in conversion efficiencies
- Higher Operating frequencies (5-10 kHz) results in compact systems
- Commodity, 1700 V SiC Transistors can be put in series to achieve low cost for 4160 V AC and 12.47 A AC systems

Results in Phase I of study

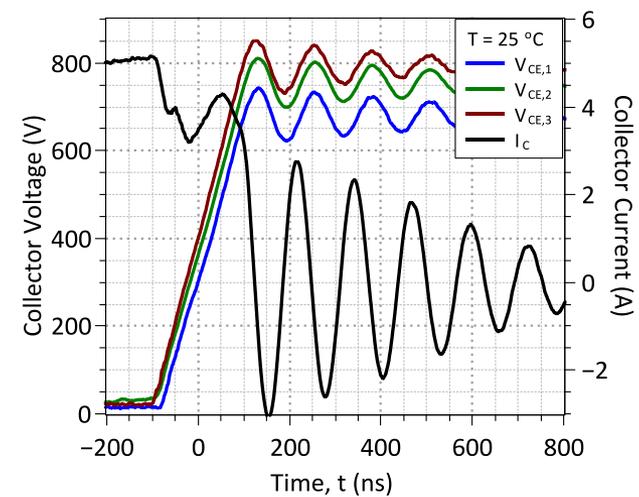
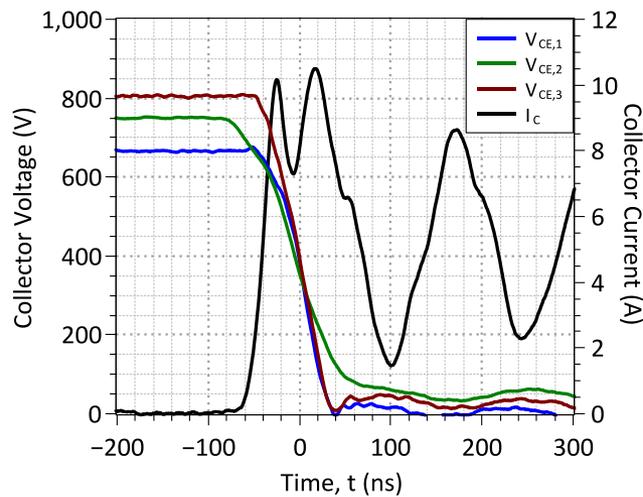
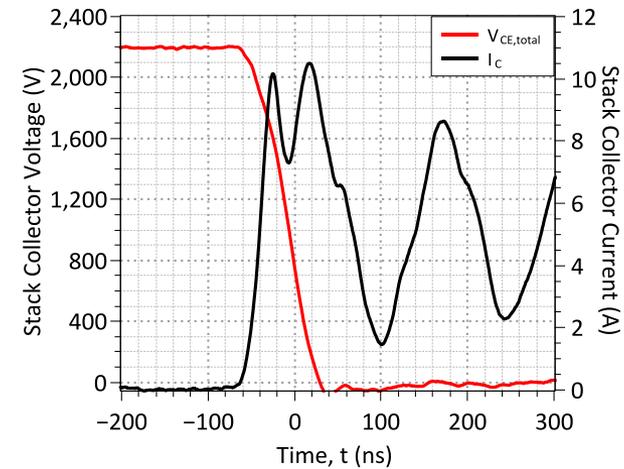
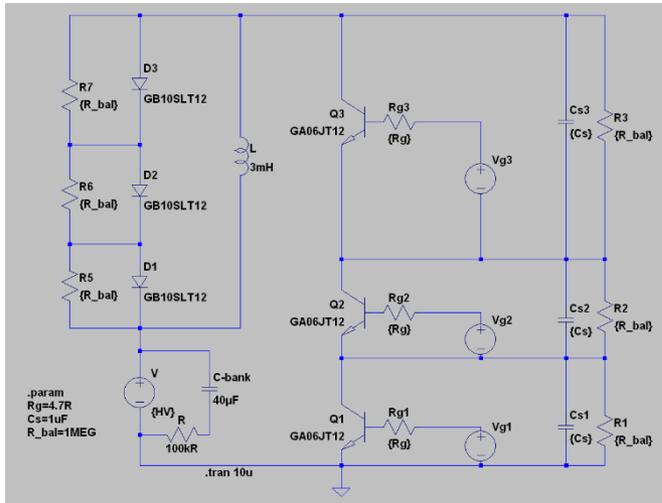


- At 1200 V bus voltages, SiC Transistors offer lower switching as well as conduction losses as compared to the fastest state-of-the-art Si IGBTs

Series Connected Device Architecture



Series Connection of SJTs proven with simulations and measurements



Calculated Loss Comparisons at 1 MVA

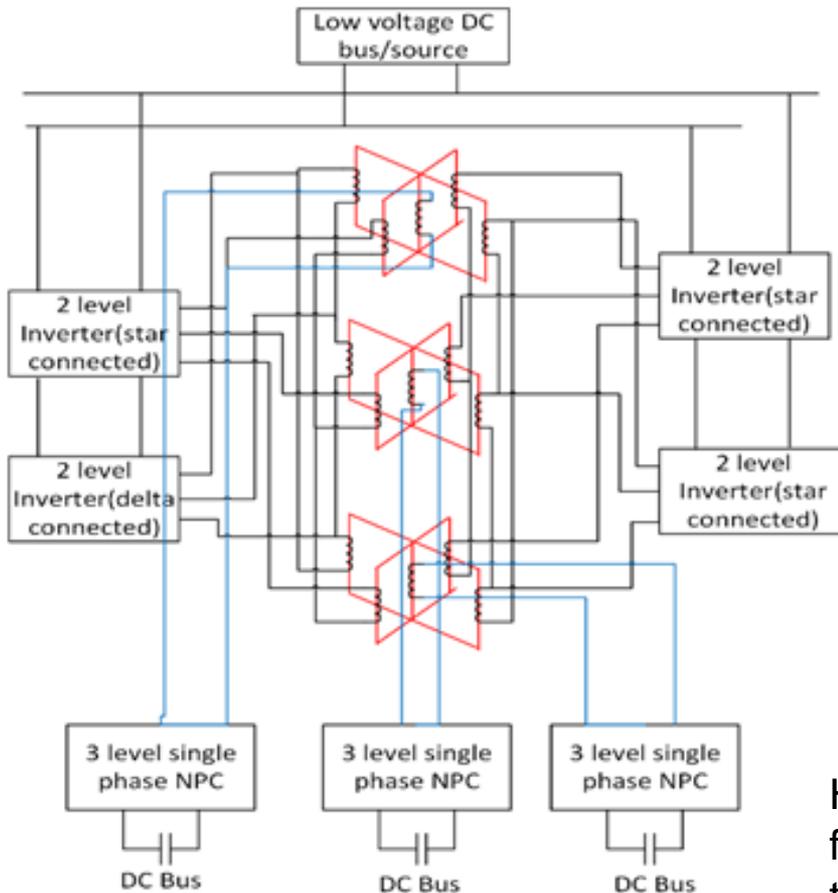
Table 1: Medium Voltage/Low Current Side loss even at 1 MVA operation.

Active Power (MW)	Reactive Power (MVAR)	Loss (W)
1	0	3064
0.8	0.6	4175
0.6	0.8	5330

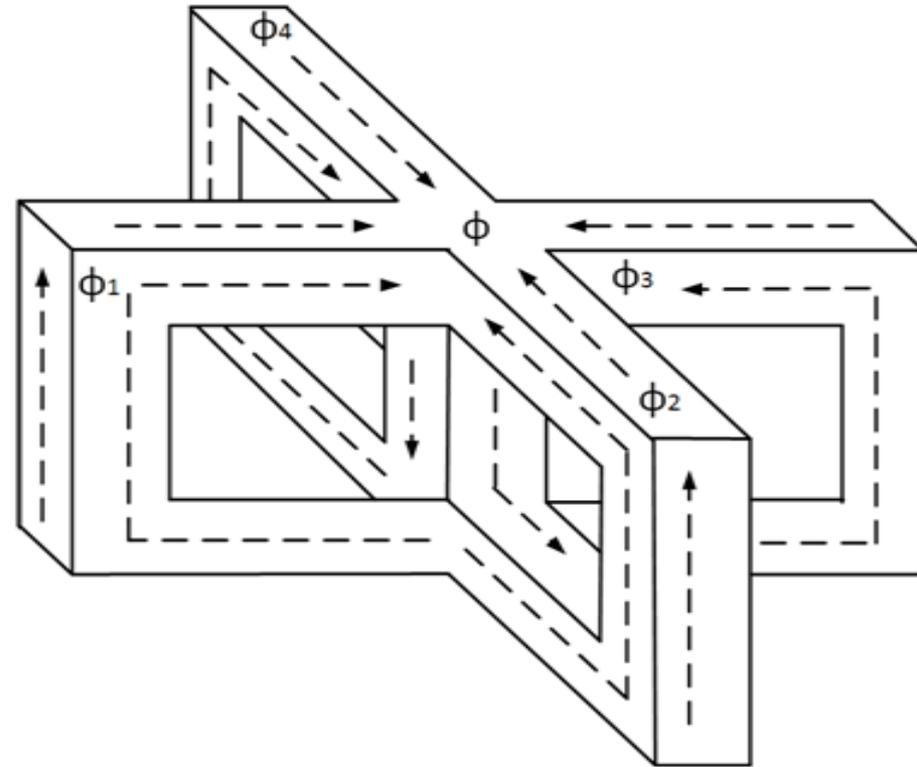
Table 2: Low Voltage/ High Current Side Loss

Active Power (MW)	Reactive Power (MVAR)	Loss (kW)
1	0	32
0.8	0.6	27
0.6	0.8	23

High Frequency 3 Phase Transformer Configuration



Three phase star delta DAB with higher power density



High-frequency (10 kHz) transformer configuration for the DC-DC DAB stage. The four limbs of the three transformers are connected in star and delta fashion to produce a stepped waveform at the middle limb of the transformer.

Status and Future Efforts

- **Current Status**
 - Phase I Project July 2015 – March 2016
 - Phase II Project started Aug 1, 2016
 - Modeling of Circuit Losses completed
 - Series connected devices being scaled up to higher power
- **Future Efforts in Phase I**
 - Complete SPICE Modeling of Devices to be used for 4160 V AC, and then 12.47 kV AC
 - Quantify the impact of All-SiC based power electronics on grid-tied energy storage systems
 - Work with commercialization partners by making a 400 kW demonstration at

Grant Details

- Principal Investigator: Dr. Ranbir Singh and Prof. Subhashish Bhattacharya
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