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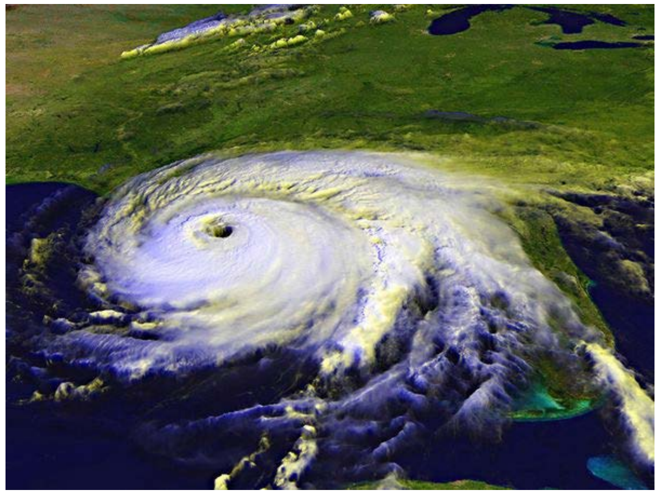


Elimination of Fast Interface States Using Phosphorus Passivation in 4H-SiC MOS Capacitors for Improved Power MOSFET Performance and Reliability

D. R. Hughart, W. C. Kao, M. Goryll, C. Jiao, S. Dhar, J. A. Cooper, D. K. Schroder, S. Atcitty, J. D. Flicker, M. J. Marinella, and R. J. Kaplar

U.S. DEPARTMENT OF ENERGY
NNSA National Nuclear Security Administration

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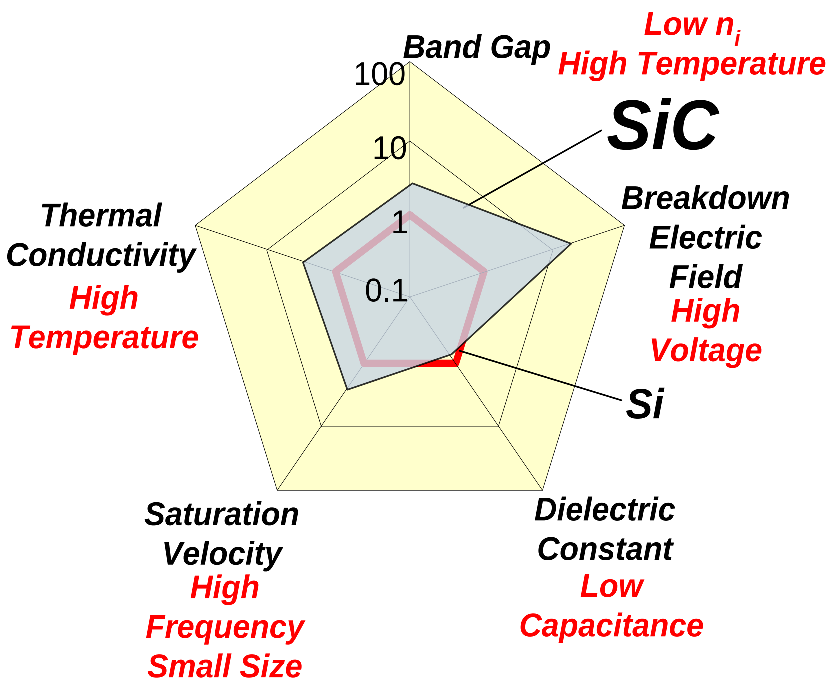
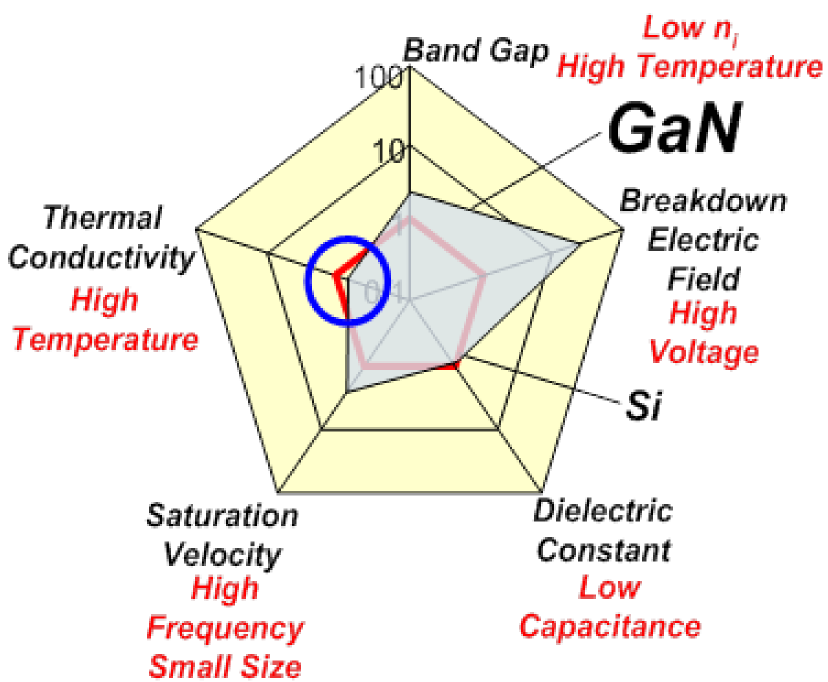
Acknowledgements

We would like to thank the DOE's **Office of Electricity** and **Dr. Imre Gyuk, Program Manager of the Energy Storage Program**, for their support and funding of the Energy Storage Program.

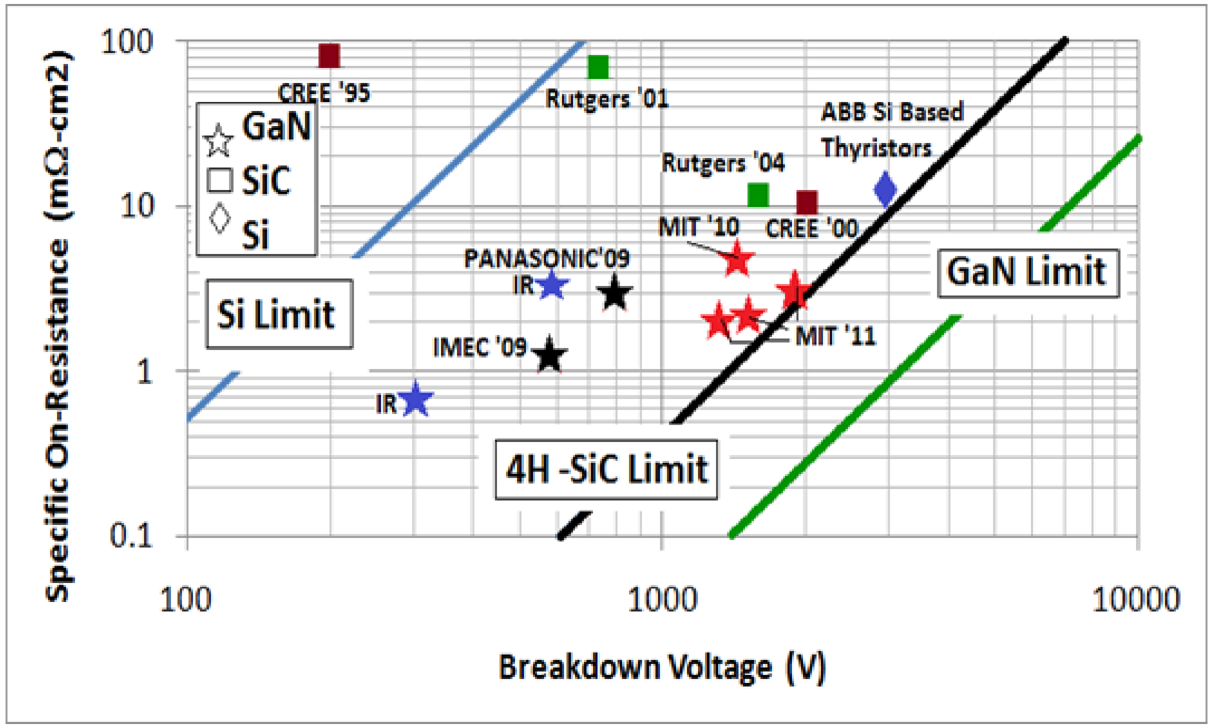
Superior Properties of Wide-Bandgap Materials





Figures courtesy of Prof. D. K. Schroder, ASU

- **Superior properties of post-silicon materials translate to better power electronics performance**
  - **Lower switching and conduction losses (higher efficiency)**
  - **Higher voltage operation (fewer power stages)**
  - **Higher temperature and thermal conductivity (reduced thermal management)**



WBG Impacts Power Conversion Systems

- **WBG semiconductors can have a strong impact on system size and weight due to higher switching frequency and reduced thermal management requirements**
  - **SiC 10 kV Modules are 9% Weight and 12% Volume of IGBT 13.5 kV Module**
- ***But their reliability is far less mature than traditional Si devices!***

Si IGBT Module
13.5 kV, 100 A

SiC MOSFET Module
10 kV, 120 A

M. K. Das et al., ICSCRM 2011

Project Overview

- ***Wide-bandgap semiconductors have material properties that make them theoretically superior to Silicon for power device applications***
  - Lower power loss and reduced cooling requirements would increase the efficiency and reduce the size and complexity of power conversion systems linking energy storage to the grid, *thus reducing overall system cost*
  - However, wide-bandgap materials and devices are far less mature than their Si counterparts; many questions remain regarding their reliability, *limiting their implementation in systems*

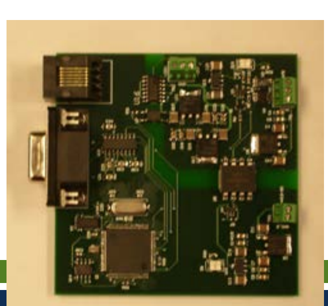
- ***Goal: Understand the reliability physics of wide-bandgap power switches and how it impacts circuit- and system-level performance***

Project Highlights

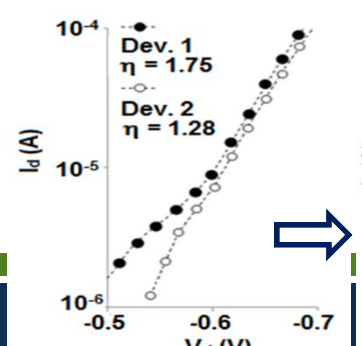
Over 25 Papers and Presentations

2009 → 2015

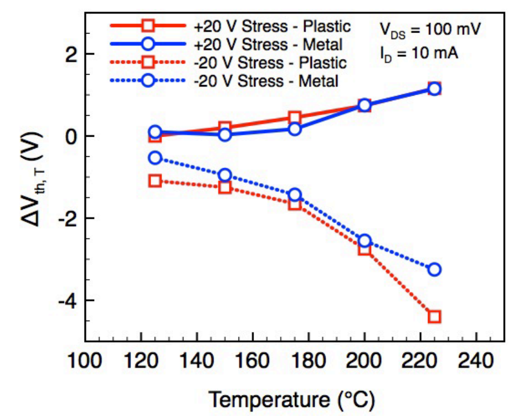
Reliability improvements suggested for components, software, and operation of Silicon Power Corporation's Solid-State Current Limiter.

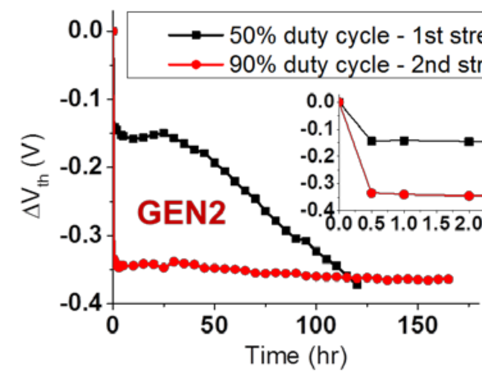


Sandia developed and documented a general process for analyzing the reliability of any power electronics system.

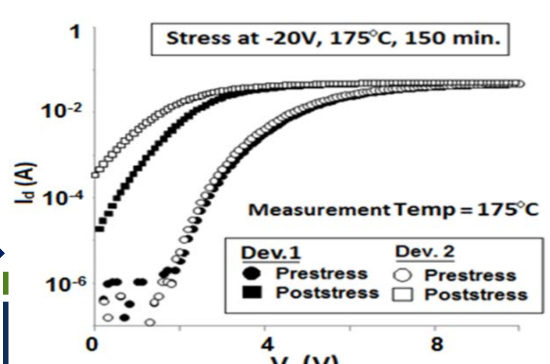


Commercial SiC MOSFETs characterized and evaluated. Investigated the impacts of bias, temperature, packaging and AC gate stress on reliability.

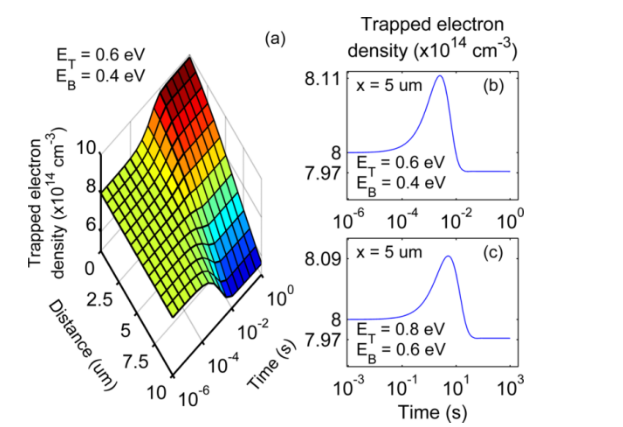




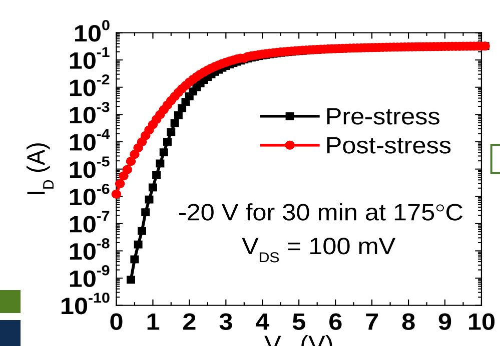
Developed models for SiC threshold voltage instability. Identified the free-wheeling ideality factor as a potential screening metric for threshold voltage shifts.

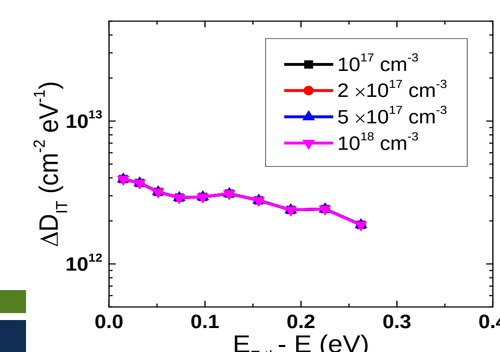


Created a physics-based model for GaN HEMTs linking defect properties to device design.



Developed an easy to use method that can be used by circuit designers to evaluate the reliability of commercial SiC MOSFETs.





Current Year Overview

While much progress has been made, reliability issues with the SiC/SiO_2 interface remain. This year we demonstrate that using phosphorus passivation reduces the concentration of 'fast interface states,' which are likely responsible for reductions in channel mobility

- Phosphorus passivation has been proposed for improving channel mobility compared to nitrogen passivation
- We tested SiC MOS capacitors fabricated using nitrogen and phosphorus passivation techniques and characterized them with conductance and high-low CV measurements
- Tests across a range of temperatures indicate that devices with phosphorus passivation showed fewer 'fast interface states'
- 'Fast interface states' are likely responsible for the lower channel mobility seen in samples that undergo nitrogen passivation

Our work this year evaluates various SiC/SiO_2 passivation techniques, their effects on interface trap densities, and how they are correlated with channel mobility. By understanding the device physics, system level performance can be improved.

Gate Oxide Reliability Has Limited the Adoption of SiC MOSFETs

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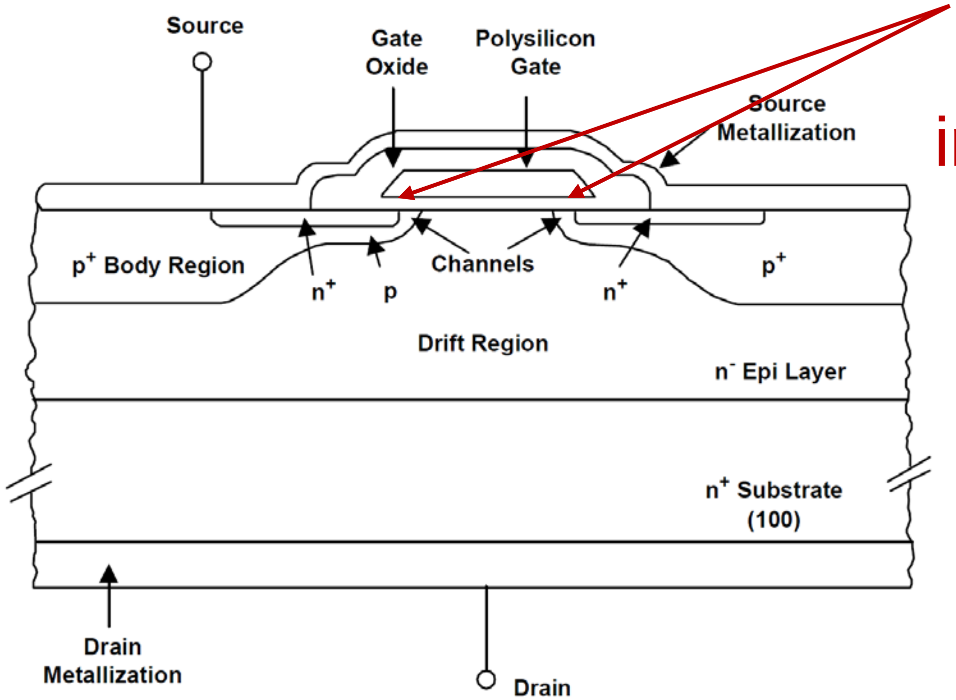
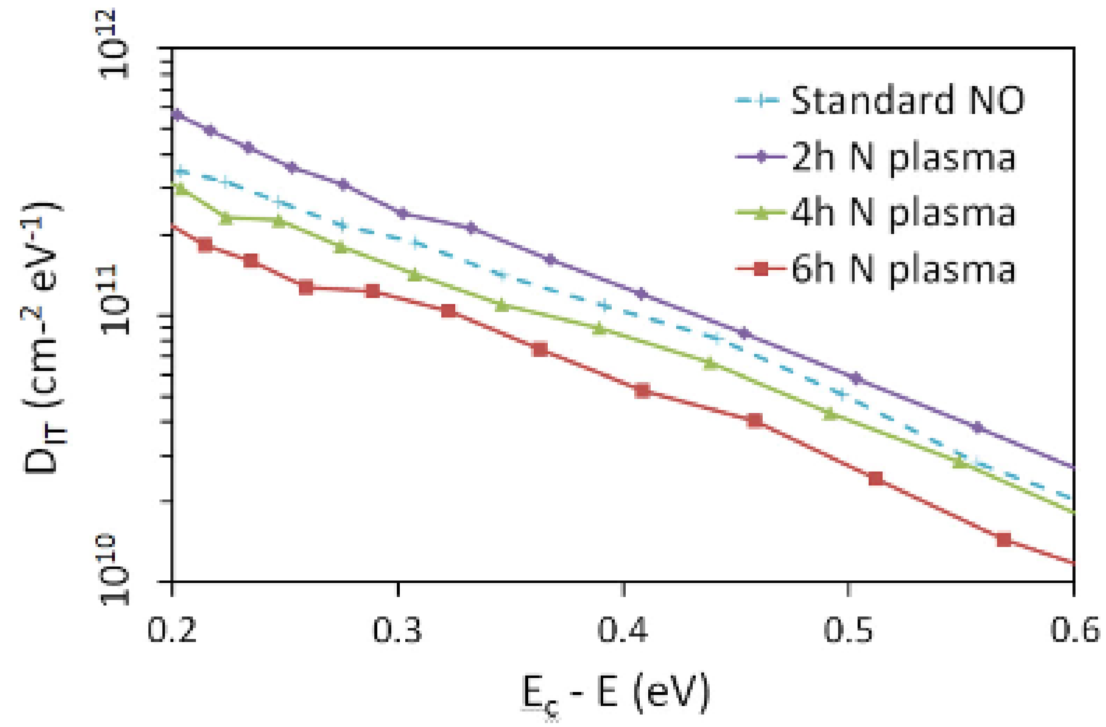
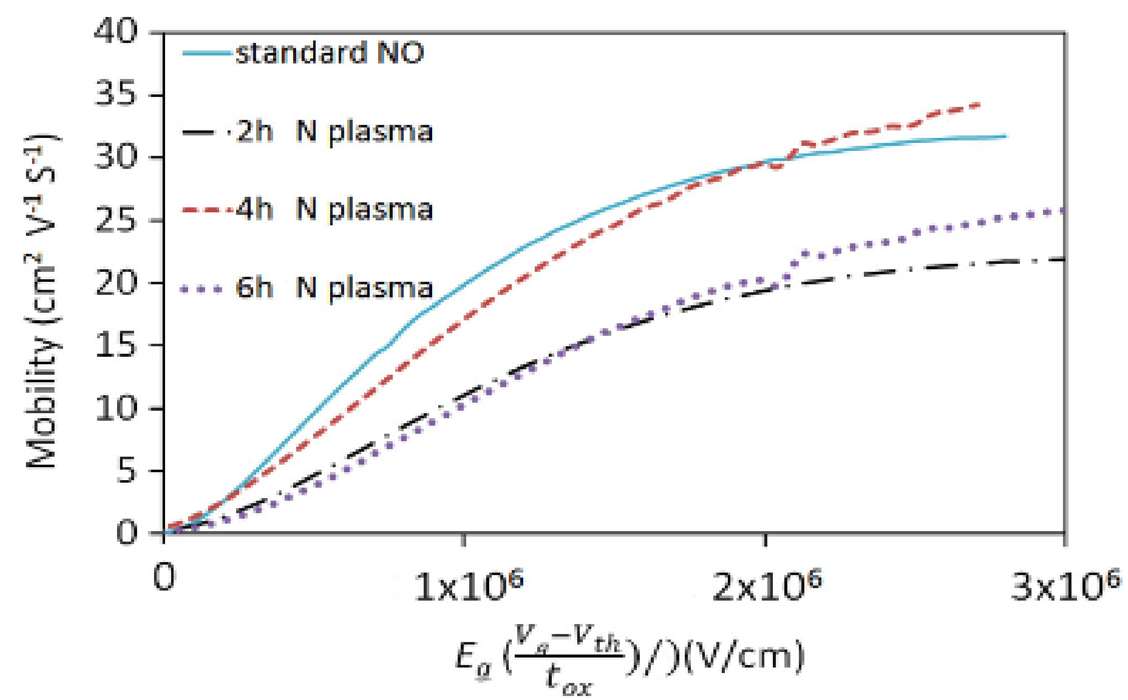
Critical gate oxide interfacial region



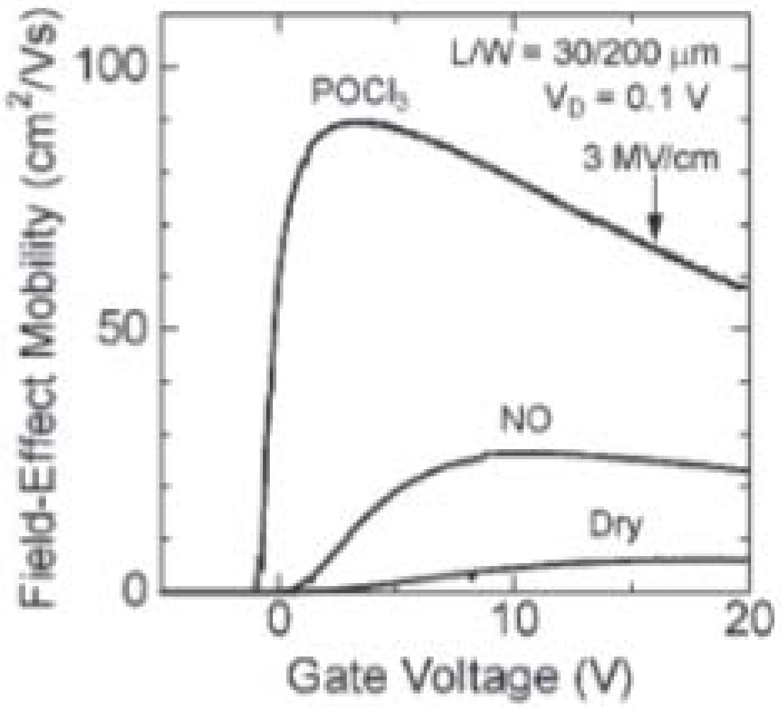


- **Large interface trap densities near the conduction band edge affect channel mobility; currently mitigated by nitrogen passivation**
- **However, passivation treatments to reduce interface traps don’t always result in improvements to channel mobility**



Phosphorus Passivation

- Using a phosphorus doped gate oxide has been proposed as an alternative to nitrogen passivation
  - Higher channel mobilities observed

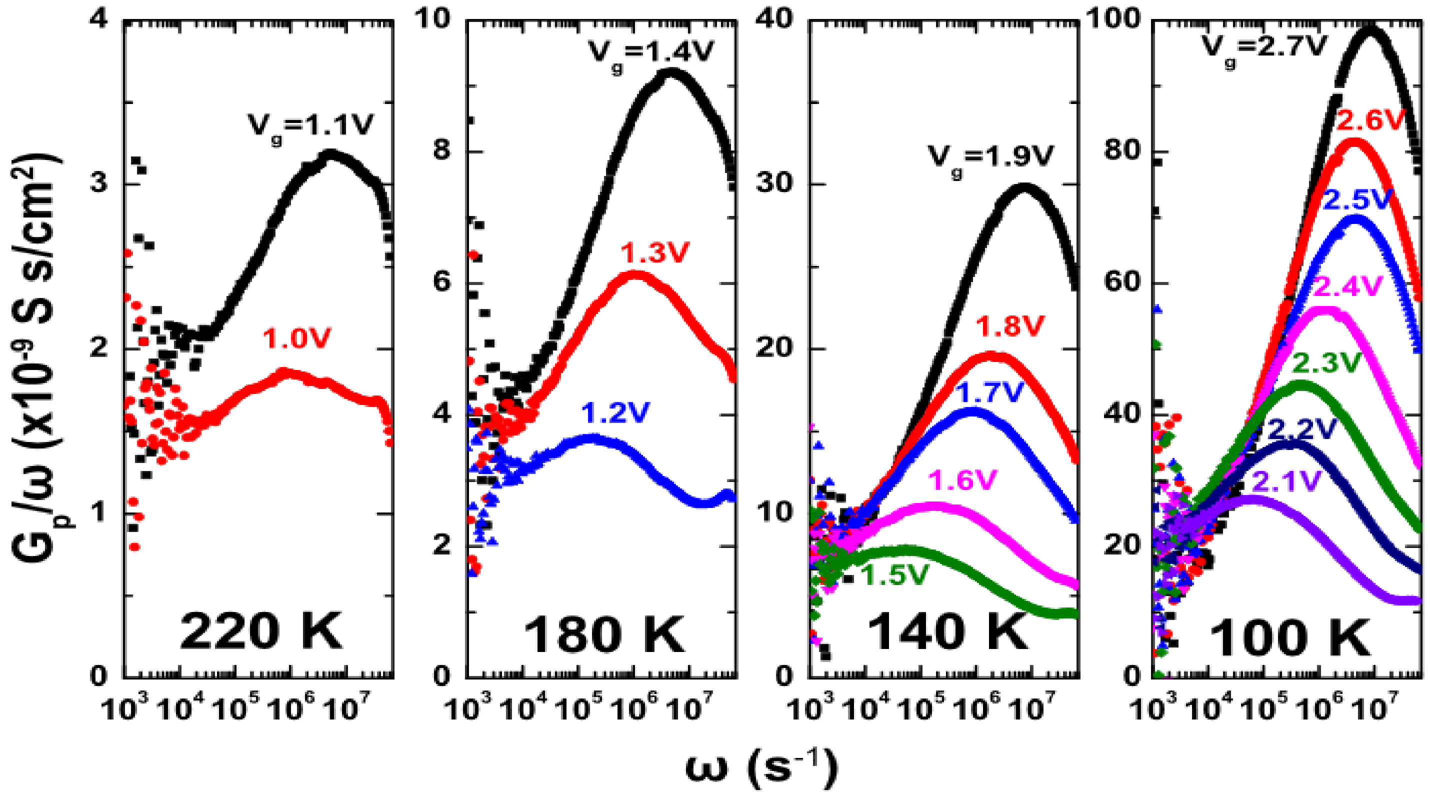


D Okamoto et al., *IEEE Electron Device Lett.* 31 710-2 (2010)

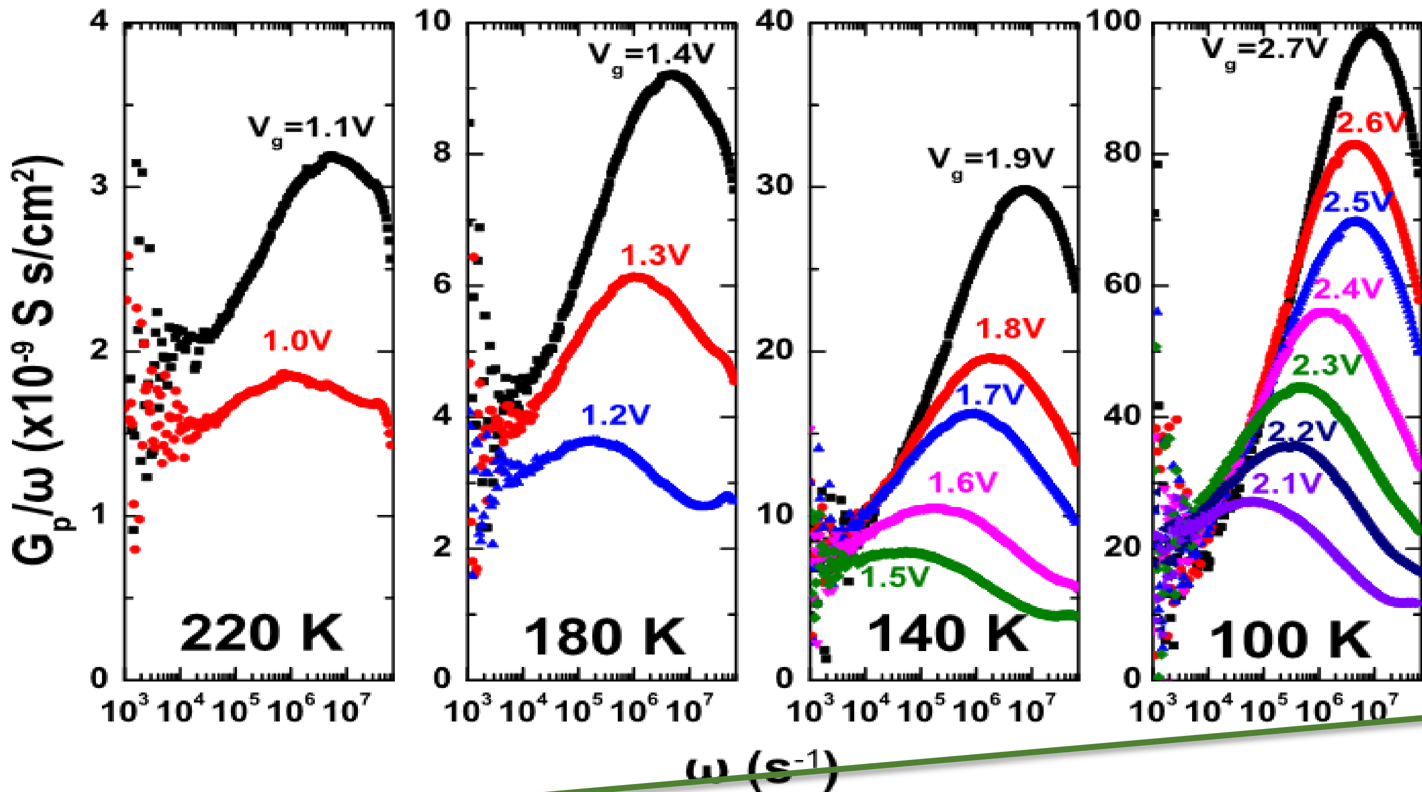
- Fabricated MOS capacitors to study the effects of three different passivation methods
  - NO annealing (industry standard)
  - N plasma
  - Phosphosilicate glass (PSG) treatment
- MOS capacitors are useful for characterizing interface quality

Detecting 'Fast Interface States'

- Interface states with fast time constants (< 1 μs) are difficult to detect with conventional characterization techniques
- Lowering the temperature during measurement increases the time constant and shifts the fast states into a detectable range
  - More distinct peaks and larger signal
  - Conductance and high-low frequency C-V measurements

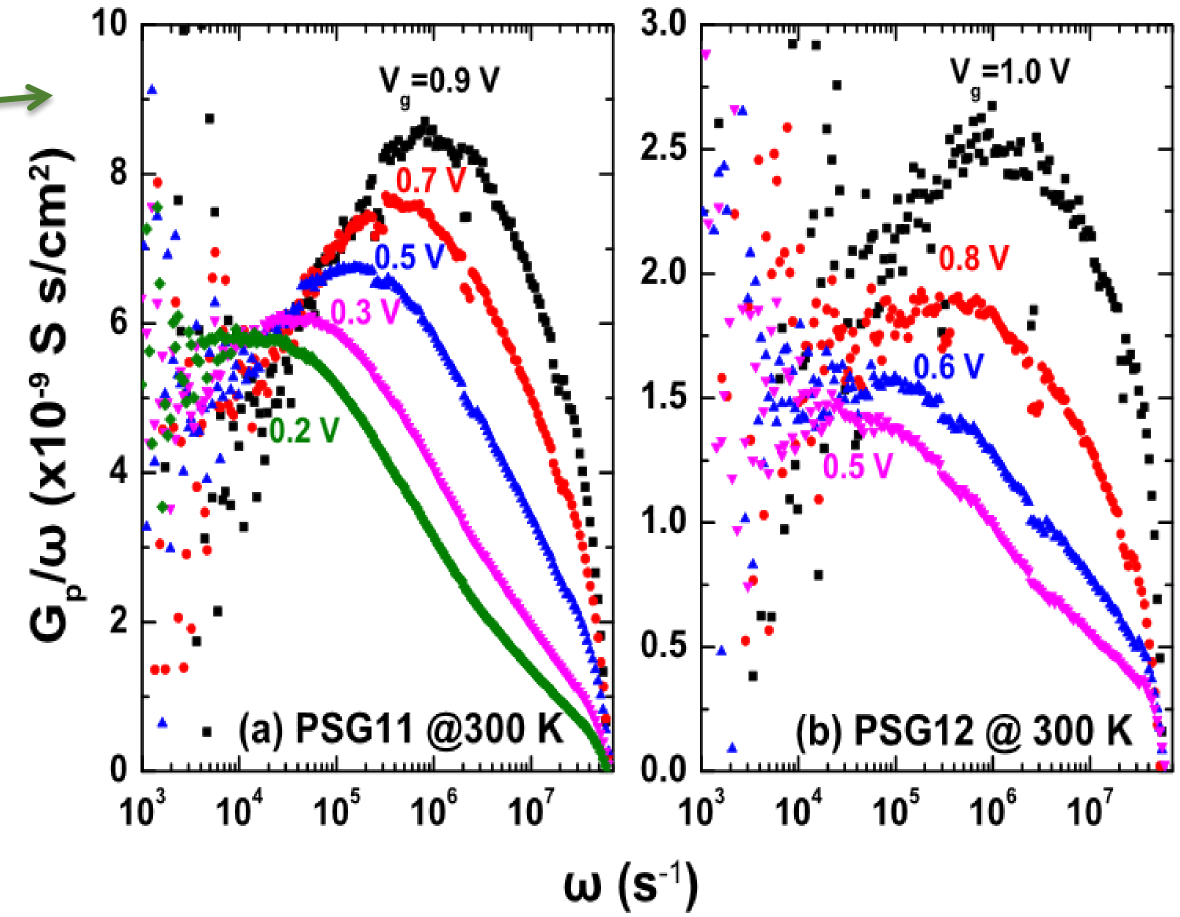


Conductance Measurements



- **N-plasma** passivated samples show larger and more distinct peaks as the temperature is reduced
  - NO samples similar

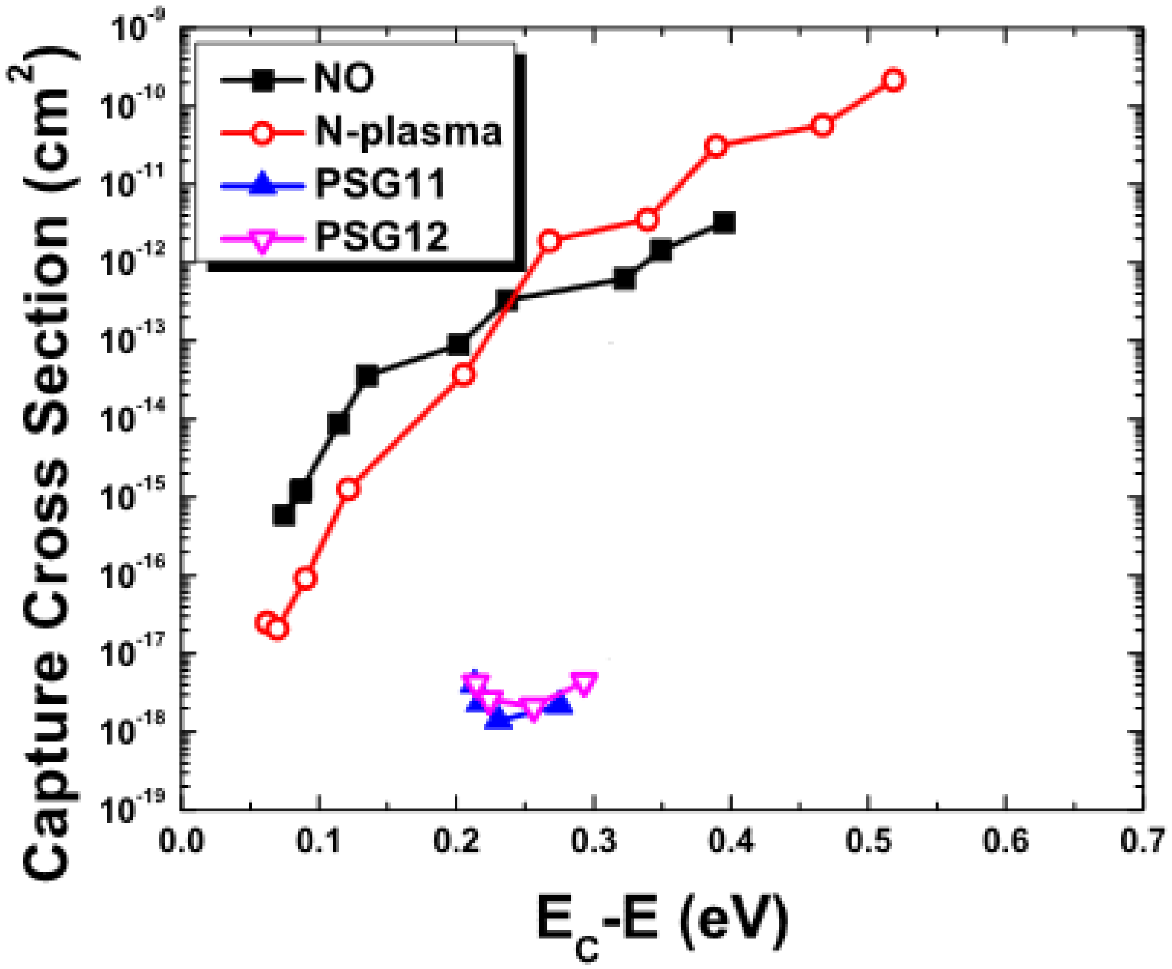
- **PSG** samples showed distinct peaks at room temperature, but not at lower temperatures
  - Lower peak magnitude indicates lower interface trap density



PSG samples show lower concentrations of traps with fast time constants

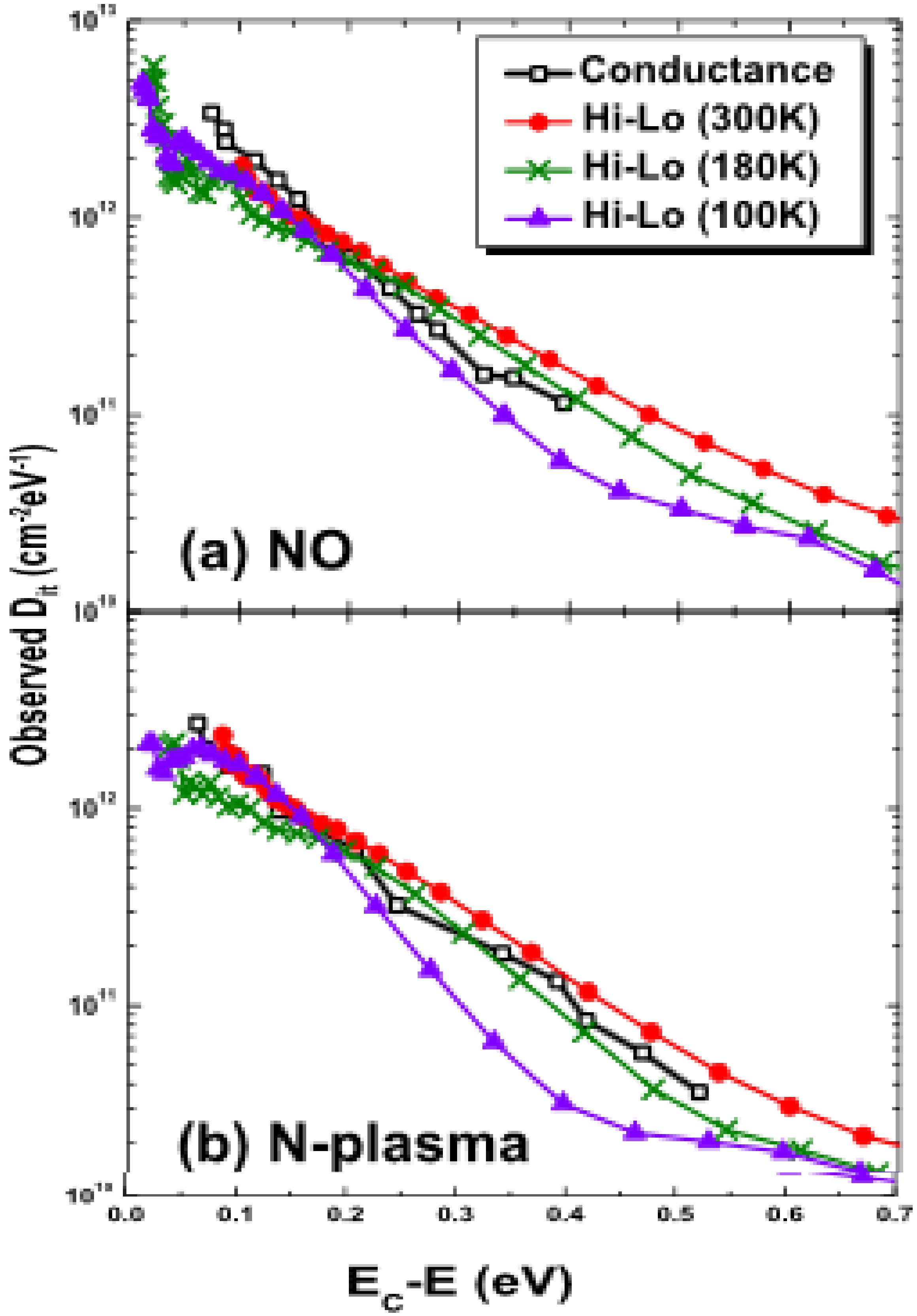
Further Differentiation of Traps

- Capture cross sections extracted from the conductance measurements show significantly different values for traps in nitrogen passivated samples vs. phosphorus passivated samples
  - Different magnitude and energy dependence
- Likely different physical origin of traps for different passivations



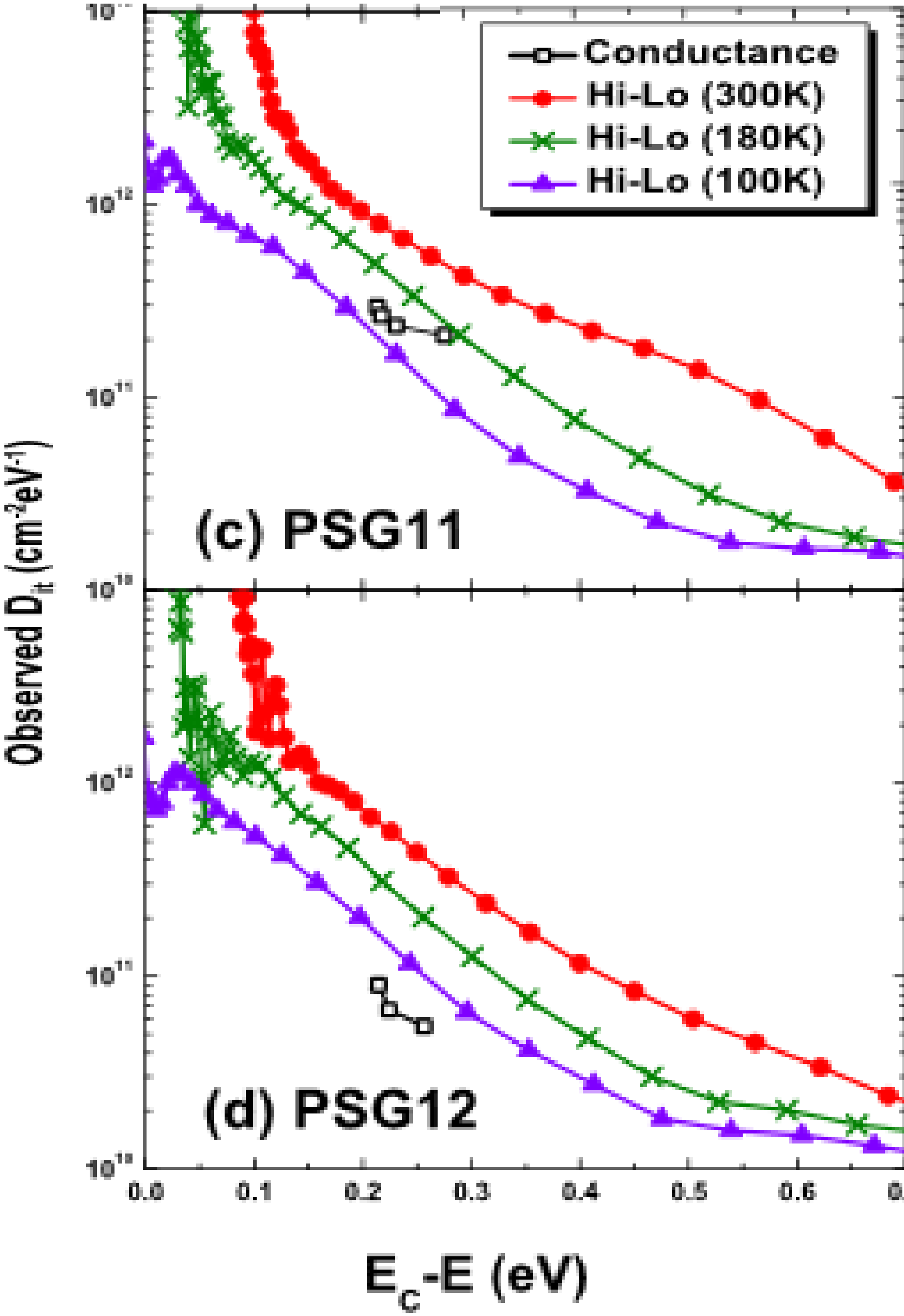
High-Low Frequency C-V

- Interface state density can also be characterized with C-V
  - Good agreement with conductance method
- Samples with nitrogen passivation show decreasing D_{IT} as temperature decreases
- At lower temperatures traps with slow time constants become too slow to be measured and traps with fast time constants become measurable



High-Low Frequency C-V

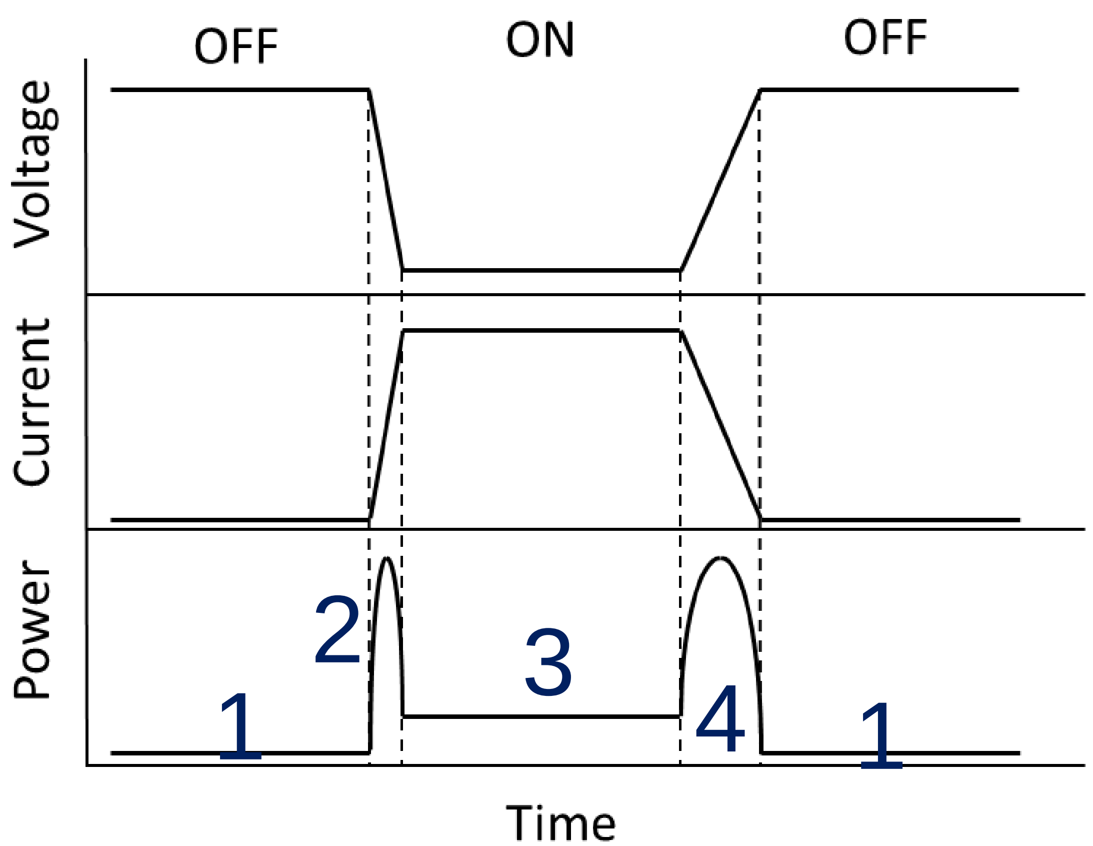
- C-V measurements made on samples with PSG passivation show sharper decreases in D_{IT} as temperature decreases
- PSG samples have lower concentration of interface traps with fast time constants than samples passivated with nitrogen



Summary/Conclusions

- Conductance and high-low frequency C-V measurements show lower densities of 'fast interface states' in SiC MOS capacitors with PSG passivation compared to nitrogen passivation techniques
  - Characterizing D_{IT} over a range of temperatures is an important consideration
- The use of a PSG passivation reduces the density of 'fast interface states'
  - Correlation with higher channel mobilities
- Improvements in mobility have implications at the system level as larger current densities enable devices to further shrink, reducing the footprint of power systems

Future Work: High Power Switching Characterization



Switch power loss mechanisms:

1. **Leakage**
2. Turn-on
3. **Conduction (R_{ON})**
4. Turn-off

High power clamped inductive load switching circuit allows realistic characterization of power losses due to switching as a function of parameters like frequency and duty cycle