**Introduction**

Cryogenic operation of CMOS electronics will be necessary for future electrically controlled solid-state qubit implementations. Understanding local heating within circuits is critical for cryogenic circuit design due to the temperature dependence of transistor and noise behavior. Additionally, cooling circuits becomes harder at cryogenic temperatures due to decreased phonon scattering and thermal conductivity, leading to increased thermal noise and degraded circuit performance. To overcome these detrimental effects we need to understand self-heating of CMOS at cryogenic temperatures and learn circuit layout techniques that reduce self-heating.

We have investigated local heating effects of a CMOS ring oscillator and current comparator at T = 4.2 K. In two cases, the temperature near the circuit was measured with an integrated thermometer. A lumped element equivalent electrical circuit SPICE model that accounts for the strongly temperature dependent thermal conductivities and special 4.2 K heat sinking considerations was developed. The temperature dependence on power is solved numerically with a SPICE package, and the results are within 20% of the measured values for local heating ranging from less than 1 K to over 100 K.

**CMOS7**

Our circuits are fabricated with Sandia's CMOS7 SOI foundry process. CMOS7 is a 0.35mm, 3.3V, five metal layer, shallow trench isolated process with 7nm gate oxide. A passivation layer consisting of 1µm of SiO2 and 0.8µm of SiN coats the top of CMOS7 devices.

**Modeling Approach**

We develop equivalent electrical circuit thermal models. In these models temperature is analogous to voltage, heat to current, and layout of the fabricated circuits.

**Temperature Controlled Thermal Conductivity**

Thermal conductivity is temperature dependent, so we need voltage controlled resistors (VCRs) for our thermal models. SPICE does not have a VCR component, so we model VCRs with a pair of voltage controlled voltage sources. The thermal conductivities are approximated with cubic-spline fits to experimental data.

**Ring Oscillator**

We built a circuit containing two 201-stage ring oscillators with diode thermometers offset the oscillators.

Using a simplified circuit layout and the CMOS7 cross-section, we create a thermal model that includes the primary cooling and heat flow paths. There is no substantial cooling path through the top of the die because of the SiN passivation layer, and no cooling path underneath because the die was mounted to an insulating printed circuit board.

We experimentally characterized our diode thermometers from 4-300K in a probe station by measuring I-V curves. For each temperature we find the voltage shift of the curve from a baseline curve measured at 4.2K. There is no substantial cooling path through the top of the die because of the SiN passivation layer, and no cooling path underneath because the die was mounted to an insulating printed circuit board.

**Current Comparator**

We also measured and self-heating of a current comparator circuit. In this design, a MOSFET's resistance is calibrated for use as a thermometer.

**Circuit Design and Layout for Cryogenic Operation**

We have successfully modeled self-heating in two CMOS circuits operating at 4.2K ambient temperature for power dissipations ranging over several orders of magnitude. The technique is generally applicable to CMOS circuits and can be incorporated in future cryogenic CMOS designs. It can also suggest design a layout techniques for improving thermal performance.

Decreasing power consumption through low-power design techniques and reducing supply voltages will reduce self-heating proportionally. Since thermal resistance, Rth-LA, increases with length and decreases with cross-sectional area, decreasing the length and increasing the width of metal traces also decreases self-heating.

Simulations with the ring oscillator suggest that increasing pad dimensions may substantially decrease self-heating by providing a more efficient transfer of cooling power from the cryogenic environment.

The SiN passivation layer is a thermal insulator, while SiO2 is thermally conductive at low temperature, so removing the SiN to allow cooling through the top of the die is helpful; placing a metal island above the circuit may be even better.