



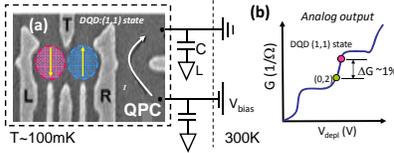
Cryogenic CMOS circuits for single charge digital readout

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Introduction

Local probing of a solid-state qubit can be achieved via electrostatic charge sensing. Combining sensitivity with fast readout with such electrometers is quite challenging due to RC time constants.

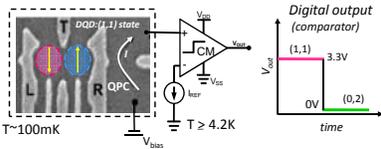


(a) Schematic diagram of a DQD acting as a qubit and a QPC capacitively coupled as a charge sensor. (b) Readout of the qubit is accomplished by measuring the change in the conductance of the QPC.

Typical values of current changes from charge sensors have presently ranged from 10pA – 350pA^{2,3}. We investigate whether CMOS circuitry residing at cryogenic temperature will provide a simple, fast and sensitive measurement scheme.

Digital Readout

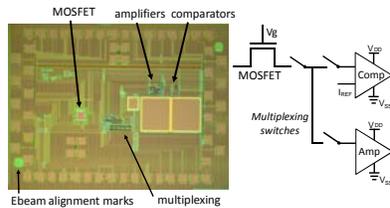
The 1st generation readout scheme is based on a current comparator which takes advantage of the changes in the conductance of the QPC by sensing variations in the current and converting it to digital signal⁴.



Setting the reference current in the comparator between the two states of the qubit allows small changes in the current of the QPC to trigger a digital signal.

CMOS circuits were fabricated through Sandia's CMOS7 foundry process through the multi-project wafer program. Cryogenic characterization of the circuit was performed via immersion in liquid helium. Two circuits investigated:

1. Current Comparator
2. Current Amplifier



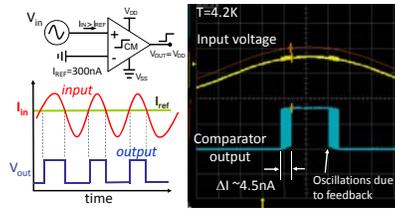
Top view of the first generation ASIC (3mm x 2mm) containing the CMOS circuits for digital readout. The ASIC contains multiplexing switches which allows several test permutations between a MOSFET, amplifiers and comparators.

Current Comparator

Sensitivity

The current sensitivity of the comparator is determined by the voltage difference needed between a stable high and a stable low state and dividing by the input impedance of the comparator (~M Ω):

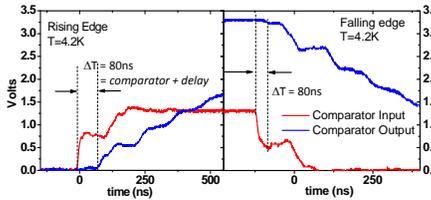
- ~4.5nA at T=300K & 4.2K



Speed

The speed of the comparator was measured to be:

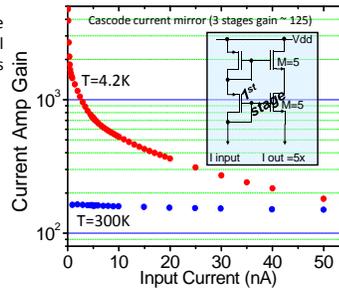
- 62ns at T=300K and 4.2K
- where a delay of 18ns is due to wiring of the setup.



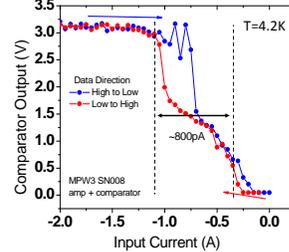
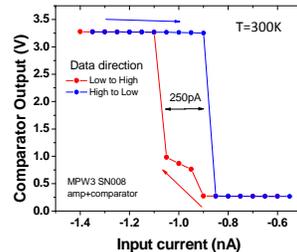
Current Amplifier & Comparator

We investigated a current amplifier on the same ASIC in hopes to increase the signal before the comparator. The observed traits were:

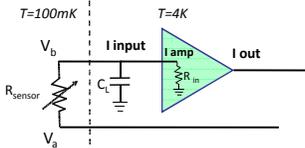
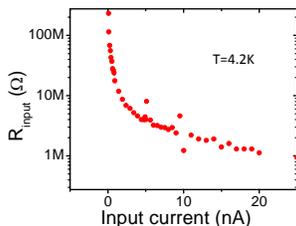
- **Bandwidth** > 100kHz
- **Gain:** 150 at 300K, 200 - 5000 at 4.2K
- **Nonlinear gain: FETs in sub-threshold regime.**
- **Spectral Noise** is due to thermal & 1/f



Comparator Sensitivity with Amp



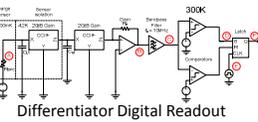
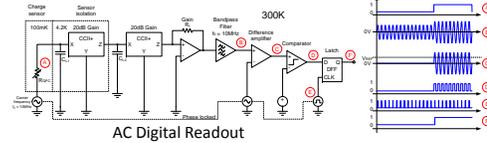
Amplifier Input impedance



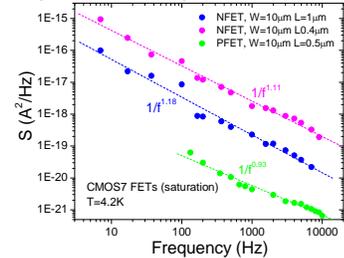
- Large R_{input} hinder ΔI sensitivity
- Does not allow to control the voltage

Future Work

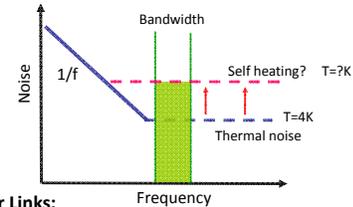
Second generation circuits are being fabricated which will allow the low noise readout to be done at high frequency, above the 1/f noise which will lead to enhanced sensitivity. Schematic diagrams of the circuits are shown below:



Noise characterization of individual FETs from CMOS7 are underway. In order to optimize the bandwidth of the circuits an optimum operating frequency must be determined in which to give the lowest integrated noise.



Optimization of circuits will involve a self consistent simulation of a multitude of circuit properties: spice modeling, noise characterization, and thermal modeling. All of this would then have feedback from actual measurements.



Poster Links:

- Low Temperature Analog CMOS Electronics, Steve Lyon
- Thermal Modeling of Circuits with Temperature Dependent Thermal Conductivities for Cryogenic CMOS, Jason Hamlet
- Charge Sensing in Laterally Coupled Doubled-Top-Gated MOS Structures using Capacitance Modeling and simulation, Harold Stafford

References

1. J. R. Petta, et al., "Coherent Manipulation of Coupled Electron Spins in Semiconductor Quantum Dots", Science, vol.309 pp.2180, 2005
2. C.B. Simmons, et al., "Charge Sensing and controllable tunnel coupling in a Si/SiGe double quantum dot", Nano Lett. 9, pp 3234-3238, 2009
3. C. Barthel, et al., "Fast sensing of double-dot charge arrangement and spin state with an rf sensor quantum dot", cond-mat: arXiv:1001.3585
4. T.M. Gurrieri, et al., "CMOS Integrated Single Electron Transistor Electrometry (CMOS-SET) Circuit Design for Nanosecond Quantum-Bit Read-out", IEEE Conference on Nanotechnology 2008, pp 609-612, 2008