Charge Sensing in Laterally Coupled Doubled-Top-Gated MOS Structures using Capacitance Modeling and Simulation

H. Stalford[1,3], R. Young[1], E. P. Nordberg[1,2], C. Borrás Pinilla[3,4], T. Gurrieri[1], J. Levy[1] and M. S. Carroll[1]

[1] Sandia National Laboratories, Albuquerque, NM; [2] University of Wisconsin-Madison, Madison, WI;
[3] University of Oklahoma, Norman, OK, [4] Universidad Industrial de Santander-Colombia, Bucaramanga, Colombia

Introduction

We investigate the effect of device geometry on charge sensing in laterally coupled doubled-top-gated MOS structures using a combination of semi-classical TCAD simulation and capacitance modeling. The model accurately renders the complex topography of the MOS double top gated structure. The simulation results agree well with experimental results. The uncertainty in the simulated projections due to variation from nominal device dimensions is estimated to be within 10%. The simulated capacitive matrix is used to make projections of charge sensing coupling strengths for future designs; we find that significant increases in coupling, by a factor of 2 to 3, could be achieved with smaller geometries. SPICE modeling combined with this capacitance network model is used to discuss circuit feedback in the quantum dot from external sensing circuitry.

3D CFD-ACE Simulation

A 19 by 19 capacitive matrix, Table 1, is simulated for the device shown in Figs. 1a,b and treated in E. P. Nordberg, et al., "Charge sensing in enhancement mode double-top-gated metal-oxide-semiconductor quantum dots," APL 95, 2010102 (2009). A 2D view of the 2DEG and poly gate conductors is shown in Fig. 2a with the SiO_2 layer removed for viewing; the simulated 19 conductor 3D meshed model is shown in Fig. 2b. The island dots C1 & C2 as shown in Fig. 2 were sized and shaped in the CFD-ACE simulation approach until the simulated capacitances A-E poly gates-to-dot C1 matched the measurements, Fig. 3. The capacitive matrix, Table 1, resulted from the that construction. The measured capacitance 0.09 aF for the charge sensor was taken after capacitive matrix in Table 1 had already been simulated. In this case, the measured capacitance for the charge sensor matched the simulated value 0.09 aF surprisingly well.

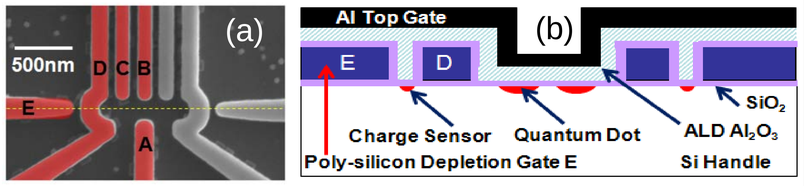


Fig. 1 (a) SEM image. (b) Cross-sectional schematic of ***Sandia's nMOS gate stack*** *(0.35 µm CMOS), SiO_2 gate oxide(35nm),* poly-Si(200nm), ALD Al_2O_3(60nm).

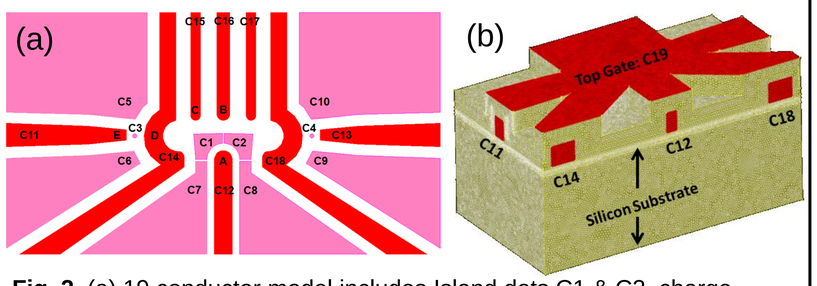


Fig. 2. (a) 19 conductor model includes Island dots C1 & C2, charge sensor dots C3 & C4, 2DEG C5-C10, & poly gates C11-C18. (b) 3D mesh model with Al top gate C19.

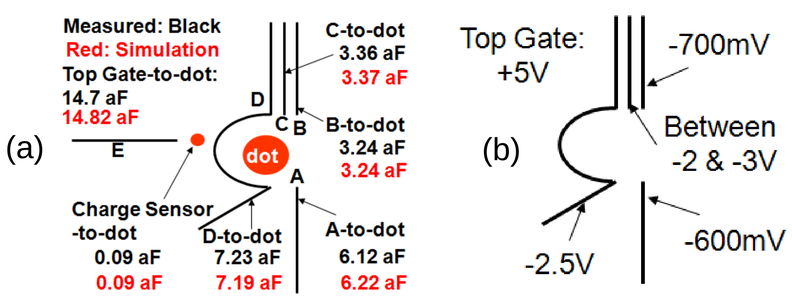


Fig. 3. (a) Simulated capacitances match measurements. (b) Voltages applied to poly gates A-E in measurements.

Table 1. Simulated capacitive 19 by 19 matrix, model of Fig. 2.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1	73.50	-11.49	-0.09	-0.03	-2.81	-1.56	-14.71	-2.70	-0.80	-1.60	-0.30	-6.22	-0.15	-7.19	-3.37	-3.24	-1.05	-1.39	-14.82
2	-11.49	73.42	-0.03	-0.09	-1.61	-0.80	-2.70	-14.47	-1.57	-2.82	-0.15	-6.21	-0.30	-1.39	-1.05	-3.26	-3.38	-7.20	-14.88
3	-0.09	-0.03	7.87	0.00	-1.65	-1.43	-0.29	-0.08	-0.04	-0.08	-1.30	-0.02	-0.01	-2.01	-0.08	-0.05	-0.03	-0.05	-0.63
4	-0.03	-0.09	0.00	7.92	-0.08	-0.04	-0.08	-0.29	-1.43	-1.66	-0.01	-0.02	-1.32	-0.05	-0.03	-0.05	-0.08	-2.03	-0.64
5	-2.81	-1.61	-1.65	-0.08	475.20	-34.80	-10.97	-4.92	-3.30	-7.94	-40.34	-1.14	-0.65	-45.04	-8.52	-5.48	-2.93	-4.03	-298.98
6	-1.56	-0.80	-1.43	-0.04	-34.80	319.26	-22.66	-6.51	-1.81	-3.30	-37.38	-0.93	-0.32	-56.83	-1.48	-1.31	-0.87	-1.76	-148.42
7	-14.71	-2.70	-0.29	-0.08	-10.97	-22.66	290.72	-19.23	-3.51	-4.92	-1.95	-32.10	-0.56	-49.10	-1.66	-1.68	-1.20	-3.45	-120.04
8	-2.70	-14.47	-0.08	-0.29	-4.92	-3.51	-19.23	290.59	-22.63	-10.98	-0.56	-32.15	-1.95	-3.46	-1.20	-1.68	-1.66	-49.17	-119.96
9	-0.80	-1.57	-0.04	-1.43	-3.30	-1.81	-3.51	-22.63	319.12	-34.87	-0.32	-0.93	-37.42	-1.76	-0.87	-1.31	-1.48	-56.72	-148.28
10	-1.60	-2.82	-0.08	-1.66	-7.94	-3.30	-4.92	-10.98	-34.87	475.44	-0.65	-1.14	-40.40	-4.03	-2.93	-5.48	-8.51	-45.12	-299.03
11	-0.30	-0.15	-1.30	-0.01	-40.34	-37.38	-1.95	-0.56	-0.32	-0.65	569.45	-0.14	-0.06	-9.17	-0.36	-0.30	-0.19	-0.33	-475.96
12	-6.22	-6.21	-0.02	-0.02	-1.14	-0.93	-32.10	-32.15	-0.93	-1.14	-0.14	503.06	-0.14	-1.47	-0.36	-0.55	-0.35	-1.46	-417.67
13	-0.15	-0.30	-0.01	-1.32	-0.65	-0.32	-0.56	-1.95	-37.42	-40.40	-0.06	-0.14	569.01	-0.33	-0.19	-0.30	-0.36	-9.15	-475.45
14	-7.19	-1.39	-2.01	-0.05	-45.04	-56.83	-49.10	-3.46	-1.76	-4.03	-9.17	-1.47	-0.33	1350.50	-110.37	-4.91	-1.98	-2.40	-1049.08
15	-3.37	-1.05	-0.08	-0.03	-8.52	-1.48	-1.66	-1.20	-0.87	-2.93	-0.36	-0.36	-0.19	-110.37	365.77	-94.51	-2.78	-1.98	-134.15
16	-3.24	-3.26	-0.05	-0.05	-5.48	-1.31	-1.68	-1.68	-1.31	-5.48	-0.30	-0.55	-0.30	-4.91	-94.51	381.87	-94.48	-4.91	-168.45
17	-1.05	-3.38	-0.03	-0.08	-2.93	-0.87	-1.20	-1.66	-1.48	-8.51	-0.19	-0.35	-0.36	-1.98	-2.78	-94.48	365.30	-110.40	-133.62
18	-1.39	-7.20	-0.05	-2.03	-4.03	-1.76	-3.45	-49.17	-56.72	-45.12	-0.33	-1.46	-9.15	-2.40	-1.98	-4.91	-110.40	1351.94	-1050.35
19	-14.82	-14.88	-0.63	-0.64	-298.98	-148.42	-120.04	-119.96	-148.28	-299.03	-475.96	-417.67	-475.45	-1049.08	-134.15	-168.45	-133.62	-1050.35	5060.41

Sandia National Laboratories

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.
SAND2011-0054P

National Nuclear Security Administration

The size and shape of the QD islands C1 was also constructed via TCAD analysis based on the MIT condition **1.5E11/cm²** electron density. From Fig. 4. we see that TCAD and CFD-ACE simulations both construct QD island dots C1 with similar size and shape, Fig. 4. The two approaches arrived at a similar size and shape. The TCAD approach used the applied voltages, Fig. 3b, whereas the CFD-ACE approach used the measured capacitances ,Fig. 3a.

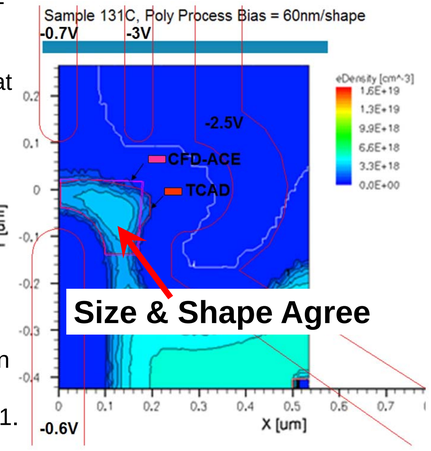
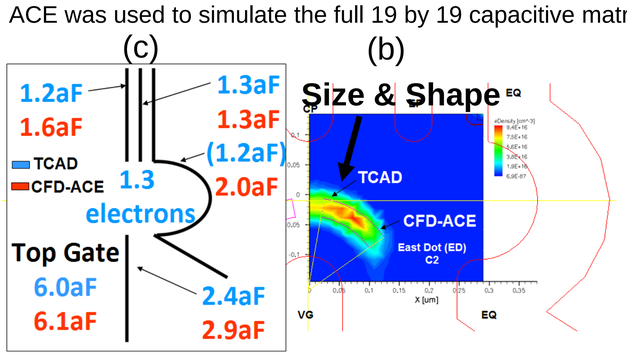


Fig. 4. TCAD analysis uses MIT condition **1.5E11/cm²** electron density to estimate the size & shape of QD island C1.

Single Electron Dot Modeling

TCAD analysis utilized applied voltages Fig. 5a to construct the size and shape of island dot C1 containing only one electron, Fig. 5b and to estimate associated capacitances, Fig. 5c. TCAD's estimated size and shape together with its estimates of gate capacitances to the one electron island dots, C1 & C2 were used in constructing CFD-ACE dots C1 & C2 as shown in Fig. 5d. CFD-ACE was used to simulate the full 19 by 19 capacitive matrix, Table 2.



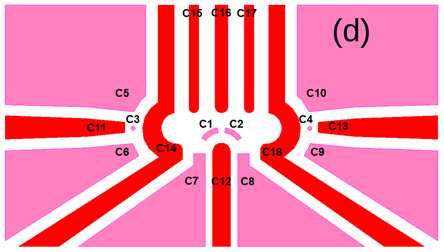


Fig. 5. (a) Applied voltages utilized to generate 1 electron dot C1, (b) TCAD simulates size & shape for one electron dot (maximum charge density of dot is 9.4e16/**cm³** or, equivalently, 0.375e11/**cm²**). (c) Comparison of capacitances: TCAD & CFD-ACE. (d) CFD-ACD Model for C1 & C2 dots

Table 2. Capacitive matrix for 1 electron dot, model of Fig. 5d

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	C18	C19
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
C1	1	24.7629	-2.3407	-0.0312	-0.0143	-1.0488	-0.5524	-3.0576	-1.3623	-0.3587	-0.7193	-0.1021	-2.8399	-0.0656	-1.5605	-1.2499	-1.6106	-0.5596	-0.7270	-6.1546
C2	2	-2.3407	24.7889	-0.0144	-0.0309	-0.7265	-0.3618	-1.3711	-3.0589	-0.5590	-1.0547	-0.0663	-2.8636	-0.1028	-0.7281	-0.5561	-1.6045	-1.2494	-1.9604	-6.1387
C3	3	-0.0312	-0.0144	8.3060	-0.0011	-1.7736	-1.5290	-0.3212	-0.0875	-0.0432	-0.0877	-1.3400	-0.0303	-0.0078	-2.1264	-0.0877	-0.0577	-0.0316	-0.0509	-0.6847
C4	4	-0.0143	-0.0309	-0.0011	8.2914	-0.0078	-0.0432	-0.0880	-0.3220	-1.5298	-1.7731	-0.0078	-0.0307	-1.3405	-0.0509	-0.0314	-0.0576	-0.0880	-2.1092	-0.6765
C5	5	-1.0488	-0.7265	-1.7736	-0.0078	478.3840	-35.6610	-11.6145	-5.2884	-3.4157	-8.1757	-40.6544	-1.3316	-0.6436	-45.6819	-8.6954	-5.6586	-3.0543	-4.1964	-300.6452
C6	6	-0.5524	-0.3618	-1.5290	-0.0432	-35.6610	322.0050	-23.4156	-3.7853	-1.8694	-3.3979	-37.7330	-1.0300	-0.3238	-57.7684	-1.5584	-1.3931	-0.9230	-1.8359	-148.8991
C7	7	-3.0576	-1.3711	-0.3212	-0.0880	-11.6145	-23.4156	288.1292	-20.5683	-3.7446	-5.2937	-1.9829	-33.5807	-0.5884	-50.9187	-2.0780	-2.0291	-1.4038	-3.8232	-122.2919
C8	8	-1.3623	-3.0589	-0.0875	-0.3220	-5.2884	-3.7853	-20.5683	298.2053	-23.4247	-11.5988	-0.5877	-33.5560	-1.5977	-3.8216	-1.4000	-2.0291	-2.0254	-51.0488	-122.2843
C9	9	-0.3587	-0.5590	-0.0432	-1.5298	-3.4157	-1.8694	-3.7446	-23.4247	321.5701	-35.6333	-0.3257	-1.0373	-37.7272	-1.8463	-0.9252	-1.3994	-1.5682	-57.6018	-148.9561
C10	10	-0.7193	-1.0547	-0.0877	-1.7731	-8.1757	-3.3979	-5.2937	-11.5988	-35.6333	477.8529	-0.6584	-1.3326	-40.6506	-4.2000	-3.0529	-5.6777	-8.7348	-45.6270	-300.1686
C11	11	-0.1021	-0.0663	-1.3400	-0.0078	-40.6544	-37.7330	-1.9829	-0.5877	-0.3257	-0.6584	555.7935	-0.1572	-0.0584	-8.9613	-0.3648	-0.3042	-0.1921	-0.3409	-462.1124
C12	12	-2.8399	-2.8636	-0.0303	-0.0307	-1.3316	-1.0300	-33.5807	-33.5560	-1.0373	-1.3326	-0.1572	488.4920	-0.1577	-1.8256	-0.5119	-0.7758	-0.5149	-1.0361	-404.8181
C13	13	-0.0656	-0.1028	-0.0078	-1.3405	-0.6436	-0.3238	-0.5884	-1.5977	-37.7272	-40.6506	-0.0584	-0.1577	555.3281	-0.3386	-0.1901	-0.3018	-0.3530	-8.9664	-461.6569
C14	14	-1.5605	-0.7281	-2.1264	-0.0509	-45.6819	-57.7684	-50.9187	-3.8216	-1.8463	-4.2000	-8.9613	-1.8256	-0.3386	1323.7220	-108.8644	-5.1121	-2.0867	-2.5592	-1024.9070
C15	15	-1.2499	-0.5561	-0.0877	-0.0314	-5.6954	-1.5584	-2.0780	-1.4000	-0.9252	-3.0529	-0.3648	-0.5119	-0.1901	-108.8644	360.0217	-93.4219	-2.8565	-2.0880	-133.0687
C16	16	-1.6106	-1.6045	-0.0577	-0.0576	-5.6586	-1.3931	-2.0291	-2.0291	-1.3994	-5.6777	-0.3042	-0.7758	-0.3018	-5.1121	-93.4219	374.3480	-92.7485	-5.1332	-154.7677
C17	17	-0.5596	-1.2494	-0.0316	-0.0880	-3.0543	-0.9230	-1.4038	-2.0254	-1.5682	-8.7348	-0.1921	-0.5149	-0.3630	-2.0867	-2.8565	-92.7485	355.7641	-108.5257	-128.5228
C18	18	-0.7270	-1.9604	-0.0509	-2.1092	-4.1964	-1.8359	-3.8232	-51.0488	-57.6018	-45.6270	-0.3409	-1.0361	-8.9664	-2.5592	-2.0880	-5.1332	-108.5257	1326.6590	-1028.9650
C19	19	-6.1546	-6.1387	-0.6847	-0.6765	-300.6452	-148.8991	-122.2919	-122.2843	-148.9561	-300.1686	-462.1124	-404.8181	-461.6569	-1024.9070	-133.0687	-154.7677	-128.5228	-1028.9650	4955.7184

Electrometry & Charge Sensing

Spin to charge conversion through a quantum point contact (QPC) or single electron transistor (SET) is one of the enabling technologies to perform measurements of double quantum dot (DQD) states. Detection of a small charge variation requires sufficiently sensitive analog electronics. The QPC can be biased in such a way to cause discrete conductance to appear across the QPC, Fig. 6. Using classical electronics, the QPC can be viewed as a classical variable resistor, i.e., CMOS comparator.

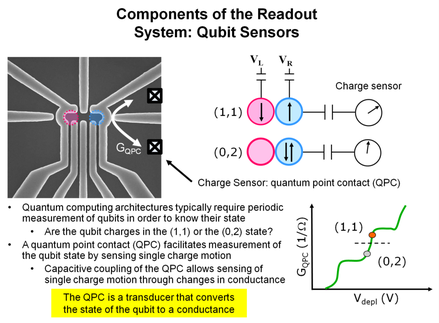


Fig. 6: The state of the DQD is indicated by the magnitude of the conductance across the quantum point contact.

During the read-out process, CMOS comparator converts the resistive variability to corresponding variations in voltage or current. Fig. 7 depicts this for both the voltage and current mode approaches .

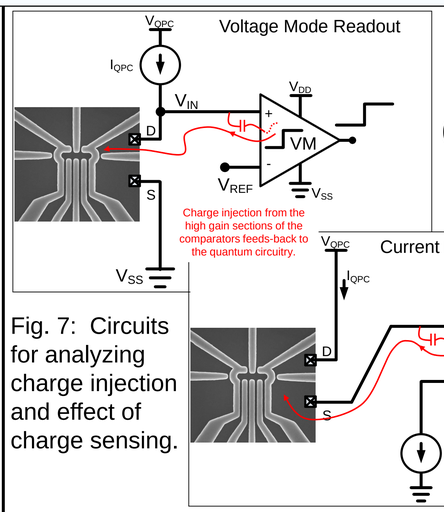


Fig. 7: Circuits for analyzing charge injection and effect of charge sensing.

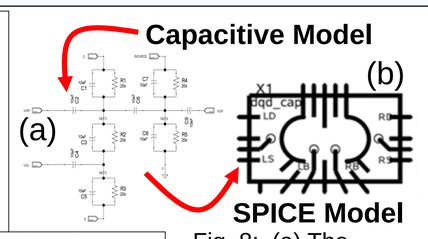


Fig. 8: (a) The capacitive model is utilized to create a small signal circuit model, (b) which is then converted to standard electronics simulation tools such as SPICE.

In the voltage mode, the QPC conductance is converted to a voltage, V_{QPC}, by applying an independent bias current, I_{QPC}, through the QPC. The result is a voltage, V_{IN}, on the drain of the QPC equal to the product of I_{QPC} and R_{QPC}, where $R_{QPC} = 1/G_{QPC}$. The DQD state is reflected on the output of the comparator as a digital high or low by comparing the resulting QPC voltage to a reference voltage. In the current mode, the QPC conductance is converted to a current by applying an independent bias voltage, V_{QPC}, across the QPC. The result is a current, I_{QPC}, through the QPC equal to V_{QPC}/R_{QPC}. Again, the DQD state is reflected on the output of the comparator as a digital high or low by comparing the resulting QPC current to an adequate reference current.

In order to study the effects of the comparator charge feedback, the capacitive model is utilized to create a small signal circuit model, Fig. 8a, for use in standard electronics simulation tools such as SPICE, Fig. 8b. In this way, the small signal model is used to do the following: (a) evaluate effect of classical electronics on DQD, (b) perform noise analysis including charge injection, feedback, and cross-talk and their effect on gate rotations, (c) correlate voltage pulses on gates to exchange energy at quantum dots, and (d) guide classical electronics to more robust and accurate designs with fewer circuit iterations.

The charge sensing feedback analysis results are shown in Figure 9 for the voltage mode comparator interfaced to the capacitive network model of the DQD, and Figure 10 for the current mode comparator interfaced to the capacitance network model. The graphs of Figure 9 show (from top to bottom) the comparator clock, which is the signal that turns on the comparator; next is the change in voltage on the comparator input node (V_{IN}) due to the charge injection; and the bottom three plots are the resulting effect on the island of the QPC which is connected to the input node of the voltage mode comparator, the right dot, the left dot, and finally the adjacent left QPC island on the opposite side of the DQD (similarly, for that in Fig. 10).

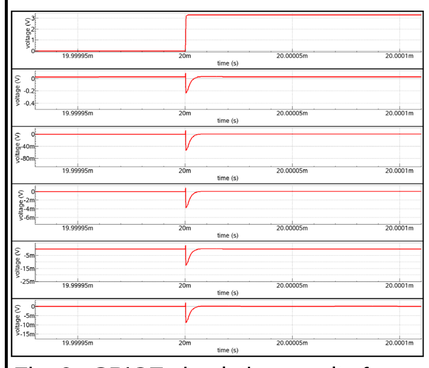


Fig. 9: SPICE simulation results for voltage mode comparator approach.

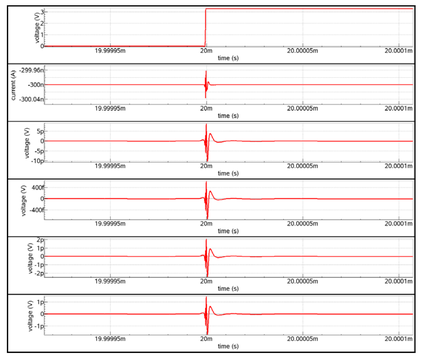


Fig. 10: SPICE simulation results for current mode comparator charge case.

The simulated capacitive matrices in Tables 1(large dot with many electrons) & 2(small dot with one electron) provide insight into making projections of charge sensing coupling strengths for future designs. SPICE modeling based on these and other capacitive models indicate that significant increases in charge sensing coupling, by a factor of 2 to 3, could be achieved with smaller geometries.

Summary

1. Simulated capacitances compare well (better than 10%) with those extracted from measurements.
2. Capacitive modeling estimates size and shape of complex quantum dots.
3. SPICE modeling results indicate that significant increases in charge sensing coupling, by a factor of 2 to 3, could be achieved with smaller geometries.